PERKIN-ELMER

MODELS 3210 AND 3210A PROCESSORS

Installation and Maintenance Manual

47-022R22

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PREFACE

This manual provides the necessary information for a technician to install and maintain the Perkin-Elmer Model 3210 and Model 3210/A Digital Systems.

While the Model 3210 is a complete system, the Model 3210/A is completely unbundled to allow the OEM user to use as much or as little hardware needed to develop his product.

Chapter 1 is the installation guide that covers unpacking, staging hardware and cabling, initial power-up checkout, and online testing information. Chapter 2 provides unpacking procedures and general configurations for the Perkin-Elmer Model 3210. Chapter 3 contains descriptions and figures of mechanical components, cooling facilities, and electrical plugs and receptacles required for the Perkin-Elmer Model 3210. It also provides a breakdown of all the subassemblies available in the Model 3210/A. Chapter 4 contains general information for the Model 3210 Power Subsystem. Chapter 5 provides installation and operation procedures for the system control panel. The remaining chapters include processor and memory board installation, block diagram analyses, and a microword description. Also described are the functions of the CPU-A, CPU-B, CPU-C, CPU-D, local bank controller (LBC), and storage module (STM) boards. Adjusting and troubleshooting procedures, test aid data, high speed data handling, hardware documentation, microcode and bootloader listings are included.

Revision 22 includes revisions 18, 19, 20, 21, and 22 and provides the following changes:

- Signal cable has been lengthened to avoid possible short against rear flange of chassis.
- The 35-813F01 and 35-813F02 terminators have been superseded by 35-813F01M01 and 35-813F02M01.
- Information drawing 01-196D12 has been revised to reflect the IDC.
- Drawing 17-597 has been revised to correct cable length table.
- Drawing 11-296M01D03 has been added to reflect the stabilizer legs as an integral part of the base welding assembly.

The following publications can be used in conjunction with this manual:

MANUAL	PUBLICATION NUMBER
Loader Storage Unit (LSU) Programming Manual	29-450
Mass Storage Module (MSM) Maintenance Manual	29-518
Removable Media Mass Storage Module (MSM) Maintenance Manual	29-644
2-Line and 8-Line Communications Multiplexor Maintenance Manual	29-650
Sub-Channel Controller Installation and Maintenance Manual	29-678
Model 550 Video Display Unit (VDU) Maintenance Manual	29-690
Model 550 Video Display Unit (VDU) Installation and Maintenance Manual	29-691
Perkin-Elmer 3220 High Performance Floating-Point Processor (HPFPP) Installation and Maintenance Manual	29-705
8KB Loader Storage Unit (LSU) Installation and Maintenance Manual	47-019
Model 3210 Power Subsystem Installation and Maintenance Manual	47-020

For information on the contents of all Perkin-Elmer 32-bit manuals, see the 32-Bit Systems User Documentation Summary, Publication Number 50-003.

CHAPTER 1
PROCESSOR INSTALLATION GUIDE

1.1 STAGING NEW HARDWARE

1. Unpack equipment and inspect for damage.

2. The Basic Processor is housed in a modified "low boy" rack which contains a processor chassis, a fan cooling system, an AC power distribution system, and a DC power system (battery backup).

3. Refer to the Model 3210 Power Subsystem Installation and Maintenance Manual, Publication Number 47-020, for AC power connection and requirements.

4. Install the processor rack in the space allocated and connect the power cable with the AC circuit breaker off.

5. Adjust the permanent leveling legs to the rack to prevent rack rollers from moving the rack. The cabling between the processor and I/O peripherals are interfaced between the cable convenience panel and the applicable I/O device.

1.2 MODEL 550 VDU STAGING AND CABLING

1. Carefully check the VDU for mechanical shipping damage.

2. Install the VDU in the space provided.

3. Install the signal cable, 17-272F01, from the VDU to the cable convenience panel.

4. With the power switch in the OFF position, install the power cord into the customer's power receptacle.

1.3 INITIAL POWER-UP

1. Prior to initial power-up of the processor, ensure that all printed circuit boards are securely seated and all cables are securely fastened.

2. Turn on the AC distribution panel circuit breaker and power up the processor. Check the voltages for proper settings on all chassis.

1.4 FINAL ON-LINE TESTING

To test the system's on-line capabilities, run the following multimedia diagnostics that apply to the configuration:

06-230R01 Perkin-Elmer Series 3200 Basic Confidence Test
06-228R02 Perkin-Elmer Series 3200 Processor Test Part 1
06-229R02 Perkin-Elmer Series 3200 Processor Test Part 2
06-236R02 S3200 19-221 MOS Memory Test Program
06-238R00 Perkin-Elmer Series 3200 Commercial Instruction Set Test
06-235R02 Perkin-Elmer Series 3200 Memory Address Translator/CACHE (MAT/CACHE) Test
06-243R01 Model 550 Video Display Unit (VDU) Test
06-127R09 Common RS-232 Interface Off-Line Test
06-159R07 Perkin-Elmer 32-Bit System Exerciser
06-133R09 Common Universal Clock Module Test
06-246R01 3200 Error Logger/Correction Diagnostic Test
06-161R06 Perkin-Elmer 32-Bit Selector Channel Test

NOTE

Test programs must be at revision level indicated or higher.

Refer to the appropriate maintenance manuals if problems are encountered.

1.5 TEST EQUIPMENT

C.E. tool kit
Extender board (15")
Extender board (17")
Oscilloscope
Extender board ribbon cables (shielded)
Model 3220 Test Aid

SYSTEM INSTALLATION
CHECKLIST

Customer_____ Date Started_____

	INITIAL
Staging Hardware and Cabling	_____
Initial Power-up Checkout	_____
Final Testing W/MMD	_____
Customer OS Running	_____

NOTES:

Date Completed_____

Installation C.E._____

Figure 1-1 System Installation Checklist

CHAPTER 2
INTRODUCTION

2.1 GENERAL INFORMATION

The Model 3210 Processor features a highly modular structure that permits configuration to the user's exact processing requirements. The system can be configured for convenient expansion as the user's requirements grow. Circuit descriptions are provided in the appropriate maintenance or instruction manuals. A front view of the Model 3210 system is shown in Figure 2-1.

2.2 UNPACKING

The system is shipped with all mounting hardware, cables, plugs, etc., necessary for complete installation.

Read the following procedures before starting an installation:

1. Carefully remove each component from its carton or crate. Observe any special unpacking instructions included with the component.

2. Inspect all components for physical damage. Consult your local Perkin-Elmer office in the event of damage.

3. If any components are shipped from the factory already mounted, ensure that all terminals and connectors are secured properly.

2.3 GENERAL CONFIGURATION AND EXPANSIONS

This section provides a general configuration for the Model 3210 System. Cables, memory expansion, power supplies, and mechanical components are discussed in detail in later chapters.

The basic Model 3210 system consists of:

1 Model 3210 Processor with 512 kb of MOS Memory
1 Loader Storage Unit
1 Consolette Panel
1 2-line Communications Multiplexor
1 Model 550 VDU
1 Universal Clock
1 Perkin-Elmer 3200 SELCH
1 75 A Power Supply with battery backup
1 I/O Chassis
1 Removable cartridge disk system

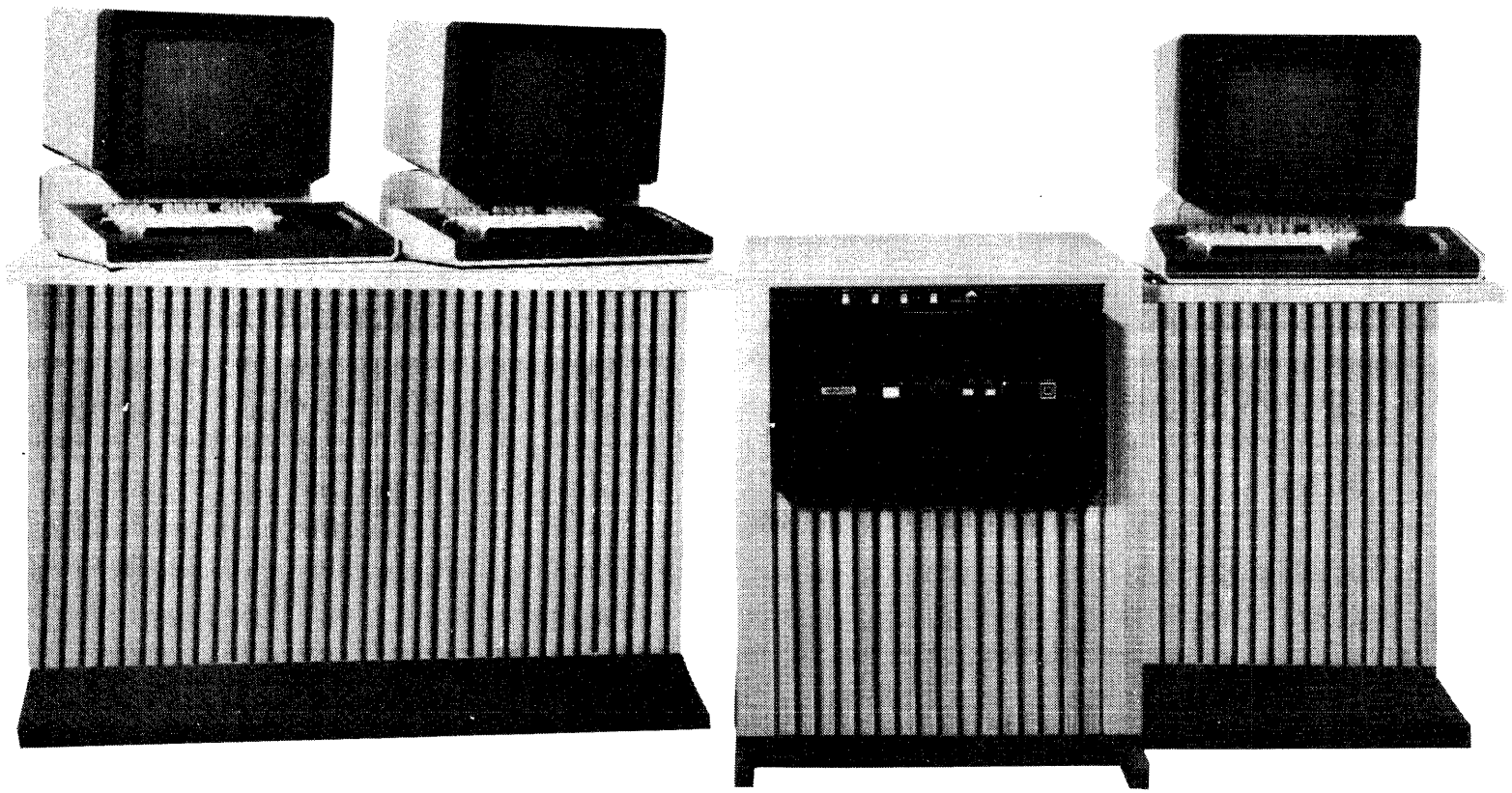


Figure 2-1 Front View of A Model 3210 System

CHAPTER 3
MECHANICAL CONFIGURATION

3.1 INTRODUCTION

This chapter describes the mechanical components and subassemblies of the Perkin-Elmer Model 3210 and Model 3210/A Digital Systems. While the Model 3210 is a complete system, the Model 3210/A provides unbundled subassemblies to allow the OEM to use as much or as little hardware needed to develop his product.

Sections 3.2 through 3.10 describe a typical Perkin-Elmer system and provide general mechanical information for the Model 3210 and Model 3210/A. Figure 3-1 illustrates the basic cabinet structure, outline dimensions, and subassembly mounting information. Figure 3-2 defines a typical component configuration within a basic cabinet.

Section 3.11 begins, in conjunction with the information drawings provided, a complete breakdown of the subassemblies available in the Model 3210/A. A list of these subassemblies is provided in Table 3-1.

3.2 CONTROL PANEL

The control panel is mounted in the top front panel position of the cabinet, fastened to the uprights by two each #4-40 machine screws and lock washers, and connected through a ribbon cable to the processor backpanel at P1. Refer to Chapter 5 for control panel cabling and operation.

3.3 DISK DRIVE

The disk drive is mounted on a slide assembly fastened to front and rear uprights per Disk Information Drawing 16-876C12. Refer to the appropriate disk manual for cabling and operation.

WARNING

PRIOR TO INSTALLING THE DISK DRIVE IN THE CABINET OR PULLING OUT THE DRIVE FOR SERVICE, THE FOUR LEVELLERS ON THE UNDERSIDE OF THE STABILIZER LEGS MUST BE ADJUSTED TO MAKE SECURE CONTACT WITH THE FLOOR. FAILURE TO DO THIS MAY CAUSE THE CABINET TO TIP OVER WHEN THE DISK IS IN AN EXTENDED POSITION.

3.4 CENTRAL PROCESSING UNIT (CPU) CHASSIS

The CPU chassis is fastened to the front uprights with eight #10-32 thread forming screws. The chassis will accommodate up to 5 17-inch boards and 11 15-inch boards as determined by system requirements.

3.4.1 Half-Boards (7-inch)

One or two 7-inch boards (half-boards) can be inserted into a 15-inch chassis slot by using a 16-398 Half-Board Adapter Kit. Refer to Figure 3-3. The kit may hold two active boards or one active and one blank board as required.

3.5 POWER SUBSYSTEM

The power subsystem mounts directly behind the CPU chassis, fastened to rear uprights with six #10-32 thread forming screws. Mounting and cable routing is designed to allow the subsystem to swing out for installation and service. See the Model 3210 Power Subsystem Installation and Maintenance Manual, Publication Number 47-020 for cabling and operation.

2501-1

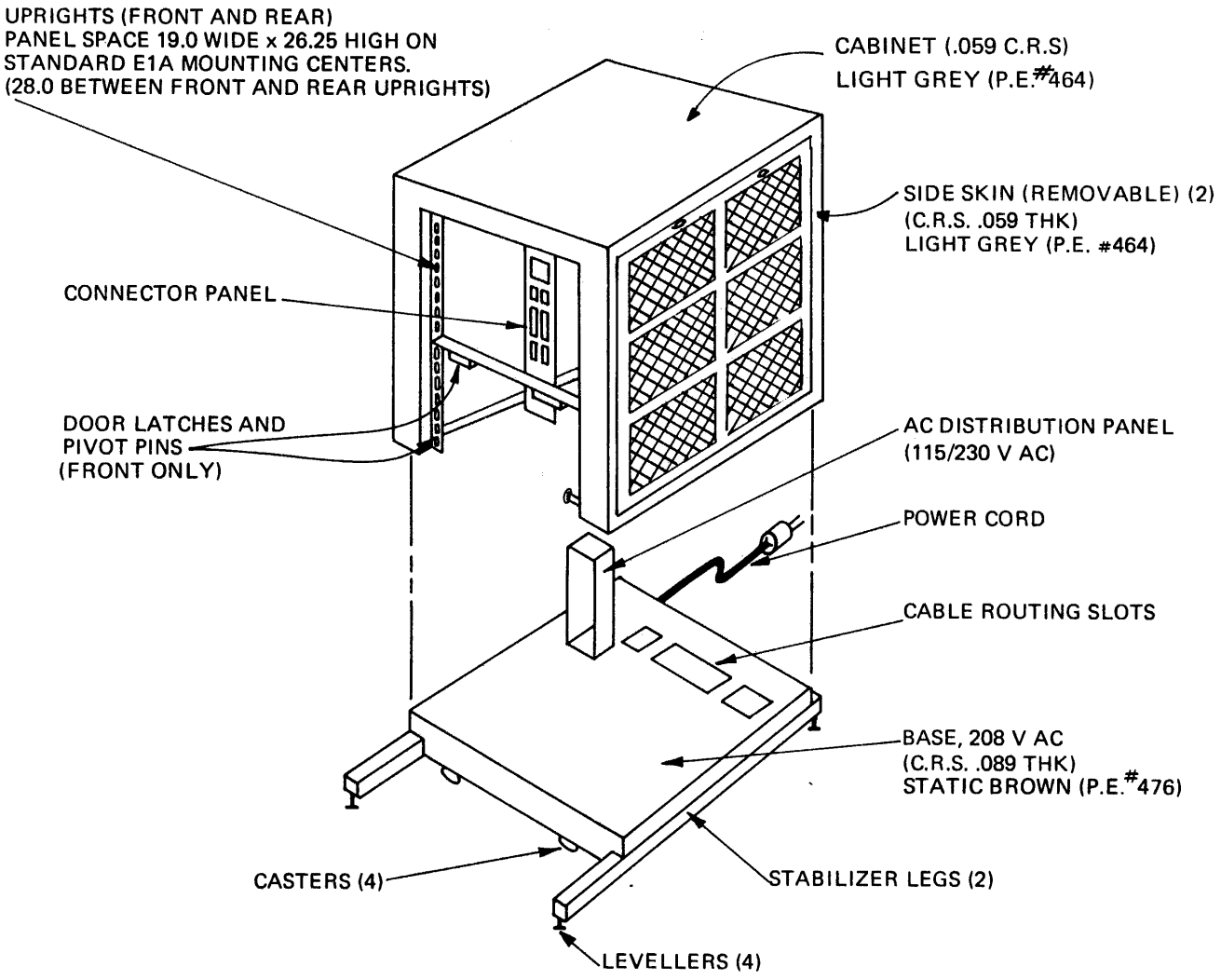


Figure 3-1 Basic Cabinet Structure

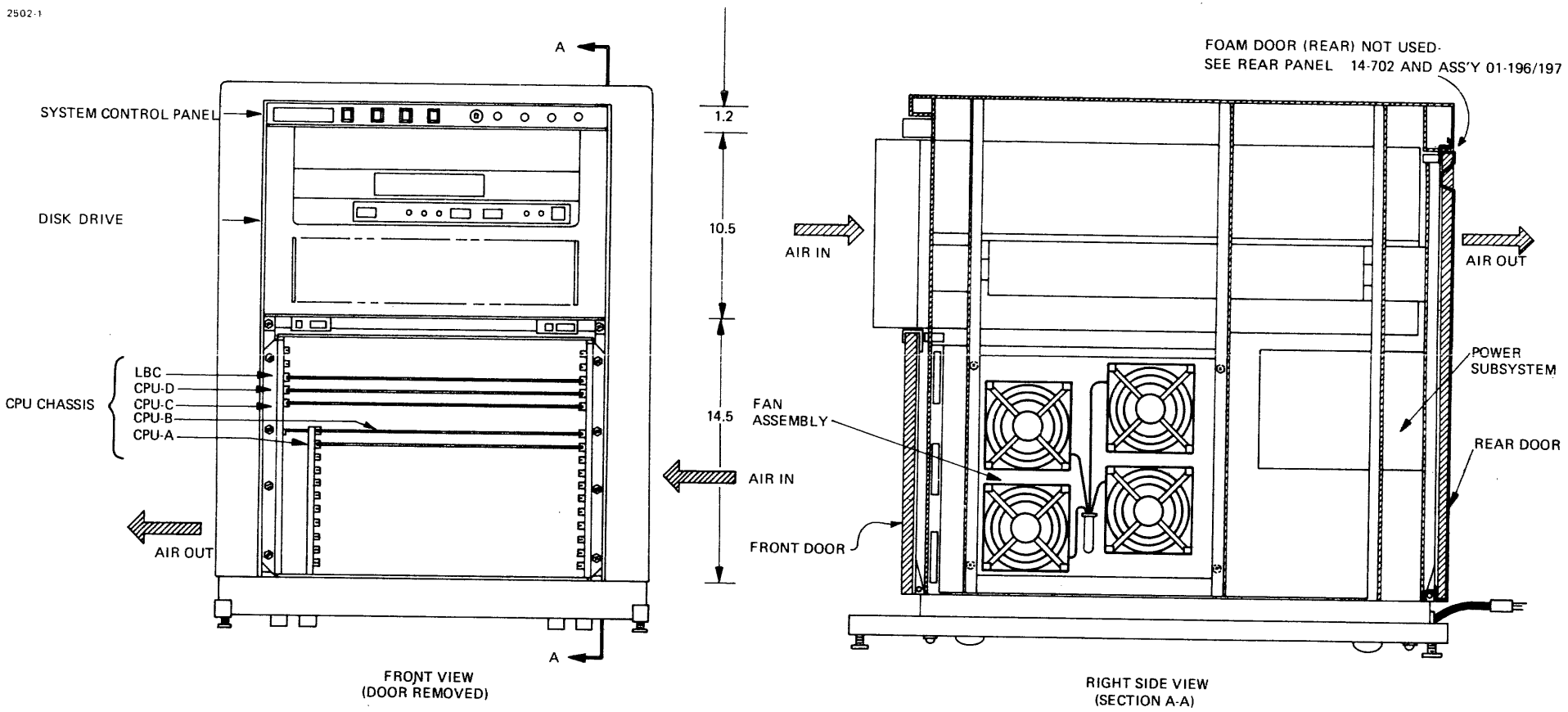


Figure 3-2 System Component Configuration

0110

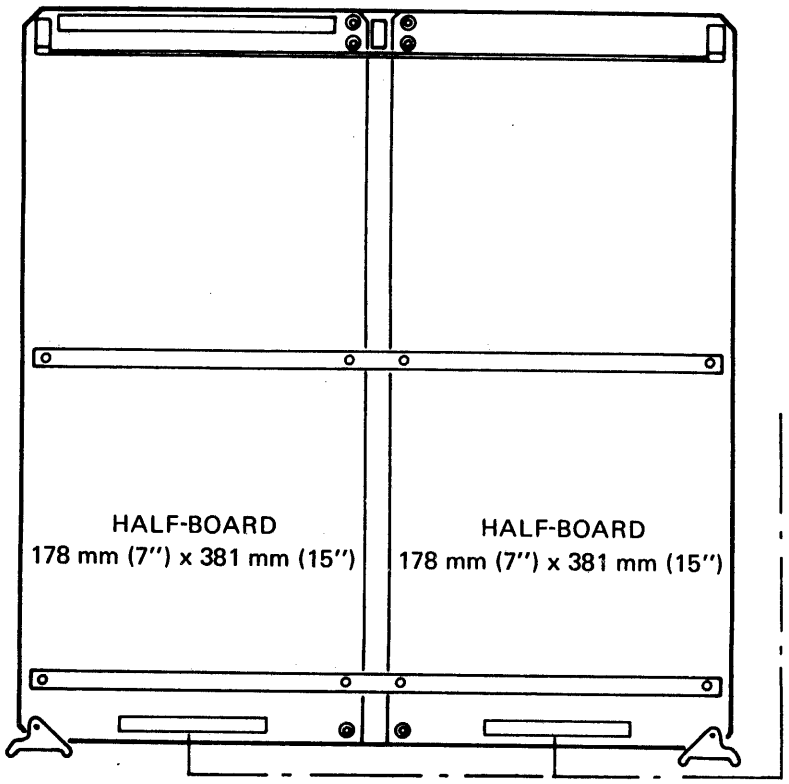


Figure 3-3 16-398 Half-Board Adapter

3.6 COOLING

The cabinet is designed to provide cooling and ventilation, using room ambient air, for three primary heat-generating components:

1. The CPU chassis is cooled by a modular fan assembly mounted to the cabinet structure along the right side of the chassis. Air is forced across the CPU boards from right to left.

2. The power subsystem includes a fan that forces air across the unit from left to right.

3. The disk drive is equipped with a built-in fan assembly that pulls air from front to rear.

NOTE

Air enters and exits the cabinet through perforated side skins and doors. The most sensitive element is the left side of the cabinet where the warm air exits. One foot (1') of clearance is recommended

to allow the warm air to exit. If one foot (1') of clearance is not possible, the cabinet should be moved forward or backward one foot (1') to allow air flow. To insure maximum component life, keep the cabinet clear of any obstructions that might restrict air flow.

3.7 POWER DISTRIBUTION

The system cabinet is powered from a 30 AMP, 208 V service. Filtered AC is distributed within the cabinet through an AC panel attached to the left center upright. The panel, accessible from the rear of the cabinet, provides AC for the power subsystem, disk drive, and two fan modules. In addition, a duplex receptacle is included for an accessory device.

3.8 CABLE ROUTING AND CONNECTIONS

Cables within the cabinet are generally routed along the left side of the enclosure as shown in Information Drawings 01-158D12 and 01-196D12. Connector panels are included along both center uprights to provide a convenient interface for terminations between internal and external cables. Cables that exit the cabinet are routed through one of three slots in the base assembly. Care must be taken to insure that cables are dressed and secured to allow sufficient clearance and slack to accommodate swing-out or slide-mounted subassemblies.

3.9 SYSTEM GROUNDING

For safety and reliability, system Signal Ground (DC Ground) is connected to Chassis Ground (AC Ground) at a single point (Uni-point Ground) in the basic processor cabinet. The Uni-point Ground is maintained throughout all multiple cabinet configurations. Refer to Figure 3-4.

3.10 EXPANSION CABINETS

Cabinets for system expansion can be supplied to accommodate various requirements within the scope of established system parameters. (See your Perkin-Elmer Sales Representative.)

Power requirements, AC distribution, and system grounding in these enclosures are identical to the specification indicated for the base system cabinet.

In general, expansion cabinets are available in two types of enclosures, and their use is limited within the guidelines described in the following paragraphs.

3.10.1 Expansion Cabinet (30") 76.2cm

30" expansion cabinets are available for disk drives and I/O expansions. The disk drive expansion cabinet is capable of housing a single disk drive, two disk drives, or a single disk drive and two I/O chassis. The I/O expansion cabinet is equipped with a single I/O chassis and master power supply and is capable of housing three I/O chassis. I/O may be expanded to only one expansion cabinet. Mountings and accessory hardware for these configurations is illustrated in Figure 3-5.

3.10.2 Expansion Cabinet (56") 142.2cm

The 56" expansion cabinet is supplied only where a magnetic tape expansion is required. Additional I/O chassis and disk drives may be rack-mounted in the available space directly below the tape drive.

- For magnetic tape drives with external formatters, combinations may include one disk drive, two I/O chassis, or one of each.
- For tape drives without external formatters, two disk drives, two I/O chassis, or a combination of both may be used.

These configurations and accessory hardware are illustrated in Information Drawing 02-752D12.

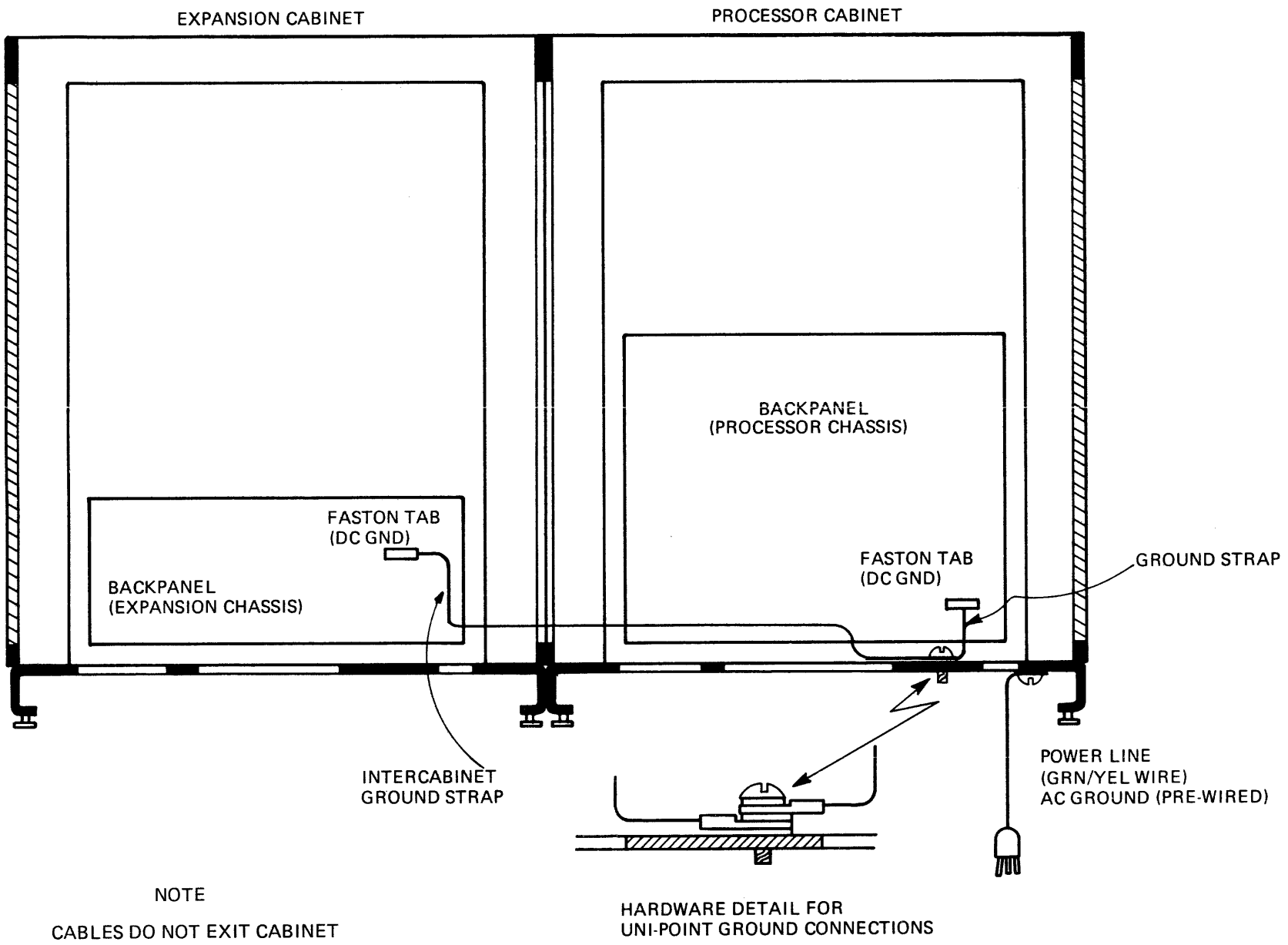
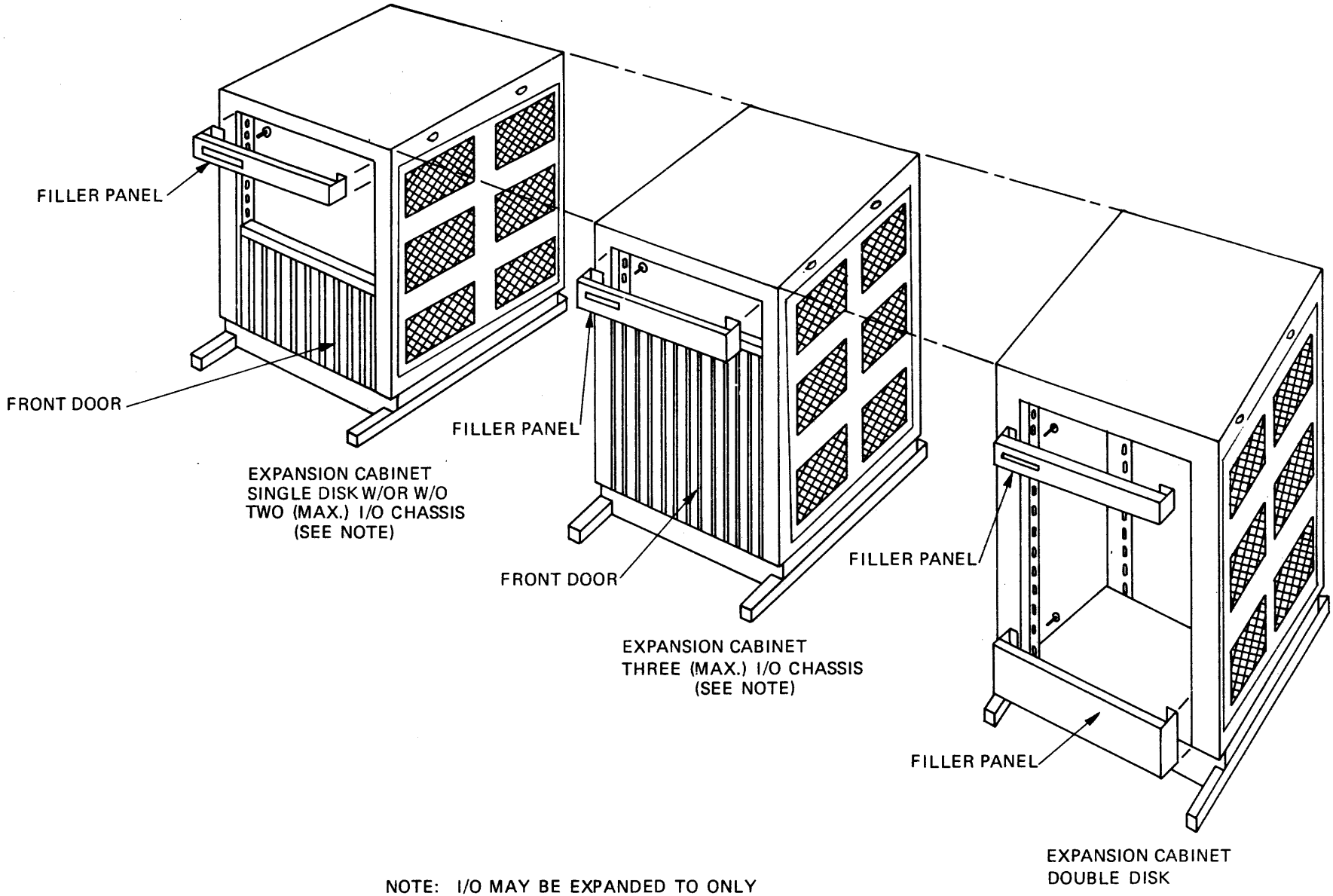


Figure 3-4 System Grounding



NOTE: I/O MAY BE EXPANDED TO ONLY ONE EXPANSION CABINET.

Figure 3-5 Expansion Cabinet Accessory Hardware

3.11 MODEL 3210/A

The following paragraphs describe the options available in the Model 3210/A System. All optional subassemblies are listed in Table 3-1. The information drawings provided must be followed during this discussion.

TABLE 3-1 LIST OF MODEL 3210/A SUBASSEMBLIES

MARKETING NUMBER	PERKIN-ELMER PART NUMBER	DESCRIPTION
M32-525	02-784F01	3210/A CPU chassis with 256 kb of memory. Includes the processor boards, memory controller (LBC), a 256 kb memory module, a 2-line communications multiplexor, a 16-slot CPU chassis with floating-point backpanel, and a control panel for a 30" cabinet.
M32-526	02-784F02	3210/A CPU chassis with 512 kb of memory. Includes the processor boards, memory controller (LBC), a 512 kb memory module, a 2-line communications multiplexor, a 16-slot CPU chassis with floating-point backpanel, and a control panel for a 30" cabinet.
M32-527	02-784F03	3210/A CPU chassis with a 1 MB of memory. Includes the processor boards, memory controller (LBC), a 1 MB memory module, a 2-line communications multiplexor, a 16-slot CPU chassis with floating-point backpanel, and a control panel for a 30" cabinet.
M32-528	02-784F04	3210/A CPU chassis with 2MB of memory. Includes the processor boards, memory controller (LBC), a 2 MB memory module, a 2-line communications multiplexor, a 16-slot CPU chassis with floating-point backpanel and a control panel for a 30" cabinet.

TABLE 3-1 LIST OF MODEL 3210/A SUBASSEMBLIES (Continued)

MARKETING NUMBER	PERKIN-ELMER PART NUMBER	DESCRIPTION
M32-529		This is the substitution of a non-floating-point backpanel on orders for M32-525, M32-526, M32-527, and M32-528. This option is not field installable and must be specified with the processor order.
	02-783F01	M32-529 with 256 kb of memory
	02-783F02	M32-529 with 512 kb of memory
	02-783F03	M32-529 with 1 Mb of memory
	02-783F04	M32-529 with 2 Mb of memory
Not Assigned	35-764F01	256 kb (1/4 Mb) expansion memory module
M32-510	35-764F02	512 kb (1/2 Mb) expansion memory module
M32-511	35-764F03	1 Mb expansion memory module
M32-512	35-764F04	2 Mb expansion memory module
M32-560	02-785	8K Loader Storage Unit (LSU) with bootloader
M32-561	11-295 M01	Cooling Fan Assembly
M32-563	02-663	Test Aid
M32-564	02-745	Battery Backup (for use with M32-540 master power supply)
M32-565	02-788F01	3210/A 30" system cabinet. Does not include front door, cooling, or power supply, 60Hz.
M32-566	02-788F02	3210/A 30" system cabinet. Does not include front door, cooling, or power supply, 50Hz.
M32-567	02-786F02	Front door for a 30" cabinet with a single CDD disk drive cutout.

TABLE 3-1 LIST OF MODEL 3210/A SUBASSEMBLIES (Continued)

MARKETING NUMBER	PERKIN-ELMER PART NUMBER	DESCRIPTION
M32-568	02-786F03	Top and bottom filler panels for a 30" cabinet with dual CDD disk drives.
M32-569	02-786F01	Full front door for a 30" cabinet.
M32-570	09-147F01	3210/A 56" system cabinet including control panel and AC distribution panel. Does not include front door, or cooling, 60Hz.
M32-571	09-147F02	3210/A 56" system cabinet including control panel and AC distribution panel. Does not include front door, or cooling, 50Hz.
M32-572	02-787	I/O interface panel for 56" cabinet.
M32-540	02-743F01	Master power supply (P5 only)
M32-541	02-744	Slave power supply
M32-513	02-752	I/O chassis for a 30" cabinet
M32-514	02-752F01	I/O chassis for a 56" cabinet
M32-509	02-665	Floating-point processor

3.11.1 Model 3210/A CPU Chassis With Floating-Point Backpanel (M32-525, M32-526, M32-527, M32-528)

Refer to sheet 1 of Information Drawing 02-784D12. This is the minimum package available and includes the processor boards, memory controller board (LBC), a 2-line communications multiplexor, a 16-slot CPU chassis with floating-point backpanel, and a system control panel for a 30" cabinet. It also includes one memory module (STM) of either 1/4 Mb, 1/2 Mb, 1 Mb, or 2 Mb size as described in Table 3-1.

The CPU chassis comes with all boards installed. The 09-140 system control panel is included, along with its related cabling and mounting hardware. All chassis mounting hardware is included.

Outline and mounting dimensions are shown for the chassis and system control panel. In the event that an OEM desires to provide his own cooling, a cooling specification chart for individual PC boards is shown at the bottom of the sheet.

NOTE

> The direction of airflow through the processor chassis is from right to left (viewing it from the front). When the Perkin-Elmer cooling fan assembly is used, the clearance instructions shown on Sheet 1 of Information Drawing 02-784D12 must be adhered to.

This drawing also shows the slot locations for the processor boards, the High Performance Floating-Point Processor (HPFPP), and other optional boards.

Refer to Sheet 2 of Information Drawing 02-784D12. A Functional Schematic, 09-140B08 is provided for the 30" cabinet system control panel. When the OEM prefers to use his own power source, a PC Assembly Power Requirements chart is provided at the top left corner. This chart shows the individual printed circuit board power requirements for P5. The P5U (uninterruptible) requirements for the memory boards are also shown.

The chassis power requirements chart at the lower left locates and describes various sense points for test purposes. This chart also describes other power requirements necessary for proper chassis operation.

At the bottom center of the sheet, a connector pin assignment chart is provided to aid the OEM in interfacing his own power supply to the chassis. A description of each connectors's function is given.

The backpanel is provided with a P5/P5U jumper depending on whether or not battery backup is used. See Detail B for instructions.

3.11.2 Model 3210/A CPU Chassis Without Floating-Point Backpanel (M32-529)

This is the substitution of a non-floating-point backpanel on the M32-525, M32-526, M32-527, and M32-528 CPUs. This is not field installable and must be specified with the processor order. The 1/4 Mb, 1/2 Mb, 1 Mb, and 2 Mb memory modules are available under this option as shown in Table 3-1. This option is described in Information Drawing 02-783D12.

3.11.3 Expansion Memory Modules

Four expansion memory modules are available with both the Model 3210 and Model 3210/A. The memory sizes are 256 kb (35-764F01), 512 kb (35-764F02), 1 Mb (35-764F03), and 2 Mb (35-764F04). These memory boards are described in detail in Chapter 14 of this manual.

3.11.4 8 kb Loader Storage Unit (LSU) With Bootloader (M32-560, 02-785)

The primary function of the 8 kb LSU is to automatically load, upon initialization, a program stored in nonvolatile programmable read-only memories (PROM) located on the 35-805 8 kb LSU printed circuit board. The standard program loaded is the Perkin-Elmer 3200 Series 8 kb LSU Bootloader Program (03-337). The first part of this program is a basic confidence test. The remainder of the program allows the user to load an OS/32 from a disk or magnetic tape. A user can load a unique program by following the procedures described in the Loader Storage Units (2 kb LSU and 8 kb LSU) Programming Manual, Publication Number 29-450 (R01 or higher). Also, refer to the 8 kb LSU Installation and Maintenance Manual, Publication Number 47-019.

3.11.5 Cooling Fan Assembly (M32-561)

Refer to Information Drawing 11-295M01C12. This drawing provides the outline and mounting dimensions for the cooling fan assembly. Airflow direction, necessary clearances with regard to the CPU chassis, and power requirements are also provided. Fan specifications and performance curves are provided in the tables at the bottom of the sheet. All mounting hardware is included in this package.

3.11.6 02-663 Test Aid (M32-563)

The 02-663 Test Aid is a compact, durable, and simple to use test fixture. It provides the necessary control to display the B, S, and ROM DATA (RD) buses of the processor, as well as the control store address (CSA), four processor flags, instruction register (IR), and I/O attention lines (INT). Complete details on the operation, installation, and maintenance of the test aid are provided in Chapter 16 of this manual.

3.11.7 Battery Backup (M32-564)

The battery backup option is intended for use with the M32-540 master power supply. The battery backup provides up to 15 minutes of backup to memory in case of power failures or brownouts.

Refer to Information Drawing 02-745C12. This drawing provides the information necessary to install the battery and P5U board into the master power supply. More detail on the battery backup and P5U board is provided in the Model 3210 Power Subsystem Installation and Maintenance Manual, Publication Number 47-020.

3.11.8 3210/A 30" System Cabinet

This option is available in 50Hz (M32-566, 02-788F02) and 60Hz (M32-565, 02-788F01). This option does not include front door, cooling, or power supplies.

Refer to Information Drawing 02-788D12. This drawing shows the 30" system cabinet without the front door and filler panels. Wiring is shown for both international and domestic usage. Cabinet outline and chassis mounting dimensions are provided to aid installation. Receptacle and plug configurations and recommended usage for both domestic and international applications are shown in Details A, B, C, and D.

A.C Distribution panel for fan power connectors, and fuse information is shown in the cabinet rear view.

3.11.9 Front Door, 30" Cabinet (M32-567)

Refer to Information Drawing 02-786D12. The 02-786F02 front door and filler panel is used in a single disk configuration. Disk location and filler panel location are shown on sheet 1. The filler panel (16-875F02) may be interchanged with a system control panel. All mounting hardware is provided.

3.11.10 Top and Bottom Filler Panels For A 30" Cabinet with Double Disk (M32-568)

Refer to Sheet 2 of Information Drawing 02-786D12. The 02-786F03 top and bottom filler panels are used for double disk applications. A front view and partial section locating the installed panels is shown. All mounting hardware is included in this package.

3.11.11 Full Front Door For A 30" Cabinet (M32-569)

Refer to Sheet 1 of Information Drawing 02-786D12. The 02-786F01 full front door is used for CPU and I/O chassis installations. Two filler panels are supplied to provide interchangeability with a system control panel as shown in partial section A-A on Sheet 1. All mounting hardware is included in this package.

3.11.12 56" Cabinet (M32-570, M32-571)

This option is available in either a 50Hz (M32-571) or 60Hz (M32-570) version. This option does not include front door or chassis cooling. It does include, however, an AC distribution panel fo for either international or domestic applications, a top exhaust fan assembly, an adaptor mounting plate for use with Perkin-Elmer cooling fan assembly 11-299M01, and a system control panel for 56 inch cabinets. All mounting hardware is included in this package. Details on this cabinet are provided in Information Drawing 09-147D12. Functional Schematic 09-148B08 is provided for the system control panel.

3.11.13 I/O Interface Panel For A 56" Cabinet (M32-572)

The panel shown in Information Drawing 02-787C12 provides interconnection capability with peripheral devices outside the cabinet. All mounting hardware is provided. Mounting and outline dimensions are provided.

3.11.14 Master Power Supply (M32-540, 02-743F01)

Refer to Information Drawing 02-743D12. Outline and mounting dimensions are provided. Cable lengths and interfacing information are shown at the upper right of the drawing. Input power plug information is given, along with fan power plug information for when the slave power supply is used. CPU chassis interconnection (2 plugs) is shown. All mounting hardware is supplied in this package. More detail on the master power supply is provided in the Model 3210 Power Subsystem Installation and Maintenance Manual, Publication Number 47-020.

3.11.15 Slave Power Supply (M32-541, 02-744)

The slave power supply is shown on Information Drawing 02-744D12. CPU interconnections and master power supply interconnections are shown at the right side of the drawing. The interface signal cable that is connected to the master power supply is shown at the top of the drawing. All mounting hardware is provided in this package. More detail on the slave power supply is provided in the Model 3210 Power Subsystem Installation and Maintenance Manual, Publication Number 47-020.

3.11.16 I/O Chassis (M32-513, M32-514)

The I/O chassis for the 30" cabinet (M32-513, 02-752) and the I/O chassis for the 56" cabinet (M32-514, 02-752F01) are described on sheet 7 of Information Drawing 02-752D12. The basic difference between the chassis (M32-513 and M32-514) is in the mounting hardware. Mounting dimensions, airflow direction, and fan power cables are shown. All mounting hardware is supplied in this package. The hardware includes cables, retainers, distribution

panels, chassis rails, I/O terminators, jumpers, and other hardware necessary to install the chassis as shown on Sheets 1 through 6 of 02-752D12.

To install the chassis into a Perkin-Elmer 30" or 56" cabinet, refer to sheets 1 through 6 of 02-752D12.

3.11.17 Floating-Point Processor (M32-509)

Chassis slots 07 and 08 are dedicated to the floating-point processor A and B boards as shown on 02-784D12. This option cannot be installed in a non-DFU backpanel.

CHAPTER 4
POWER SUBSYSTEM

4.1 INTRODUCTION

The Perkin-Elmer Model 3210 Power Subsystem is a modularly designed power converter system suitable for use with the Perkin-Elmer Model 3210 System. This subsystem provides 5 volt logic power (P5), uninterruptible 5 volt memory power (P5U/Battery Backup), and can be expanded for use with the optional 34-040 slave power supply.

The Perkin-Elmer Model 3210 Power Subsystem and its companion 34-040 slave power supply option are designed to meet Underwriter's Laboratory (UL), Canadian Standard Association (CSA), and Verband Deutscher Electrotechniker (VDE) approval. For detailed information on ratings, installation, and maintenance, refer to the Model 3210 Power Subsystem Installation and Maintenance Manual, Publication Number 47-020.

CHAPTER 5
SYSTEM CONTROL PANEL

5.1 INSTALLATION

The system control panel mounts at the top front panel mounting position of the cabinet, fastened to the vertical uprights with two each #4-40 machine screws and lock washers. Refer to Figure 5-1.

The panel is connected through a ribbon cable (P1), to the processor backpanel (J1). Connector P1 is keyed to ensure correct orientation.

5.2 OPERATION

Function switches and indicators are described in the following sections. Refer to Figure 5-2.

5.2.1 Function Switches

5.2.1.1 Key-Operated Security Lock

This is a 3-position (STANDBY/ON/LOCK) key-operated locking switch that controls the primary power to the system. The key lock performs the following functions:

- STANDBY - Processor 5 volts is OFF. 5 volts STANDBY (P5U) is ON.
- ON - Primary power is ON.
- LOCK - Primary power is ON, and the INITIALIZE HALT/EXE and SINGLE switches on the system control panel are disabled.

5.2.1.2 Initialize (INIT) Switch (Momentary Switch)

This switch causes the system to be initialized. After the initialize operation, all device controllers on the system multiplexor bus are cleared, and certain functions in the processor are reset. This switch is disabled when the key is in the LOCK position.

5.2.1.3 IPL ENABLE/DISABLE Switch

When the IPL ENABLE/DISABLE switch is in the ENABLE position and AC power is restored, if the security lock switch is placed in the ON position from the STANDBY position, or if the INIT switch is depressed, the system is reloaded from the loader storage unit (LSU).

5.2.1.4 HALT/RUN Switch

When depressed, this single action switch causes a running system to halt and enter the processor console service state, or it forces a halted system in the processor console service state to enter the run mode.

5.2.1.5 SINGLE Switch

This switch, when placed in the ON position, puts the processor in the single instruction cycle mode and takes a running program to the processor console service mode. When in the single instruction cycle mode, the processor is returned to the processor console service mode after execution of each user instruction. The location counter displays the address of the next instruction to be executed. The status portion of the PSW reflects the execution of the previous instruction.

5.2.2 Indicators

5.2.2.1 Central Processing Unit (CPU) Power

This indicates that the processor system power (P5) is ON.

5.2.2.2 Memory Power

This indicates that memory system power (P5U) is ON.

5.2.2.3 WAIT

The running program can place the processor into the WAIT state by setting the WAIT bit of the current program status word (PSW). The WAIT indicator is lit to inform the operator of this condition. The indicator is also lit when the processor is in the console service mode.

5.2.2.4 FAULT

This indicator is lit during system initialization and remains lit until microcode power-up test is successfully completed. The indicator remains on if the processor self-test fails.

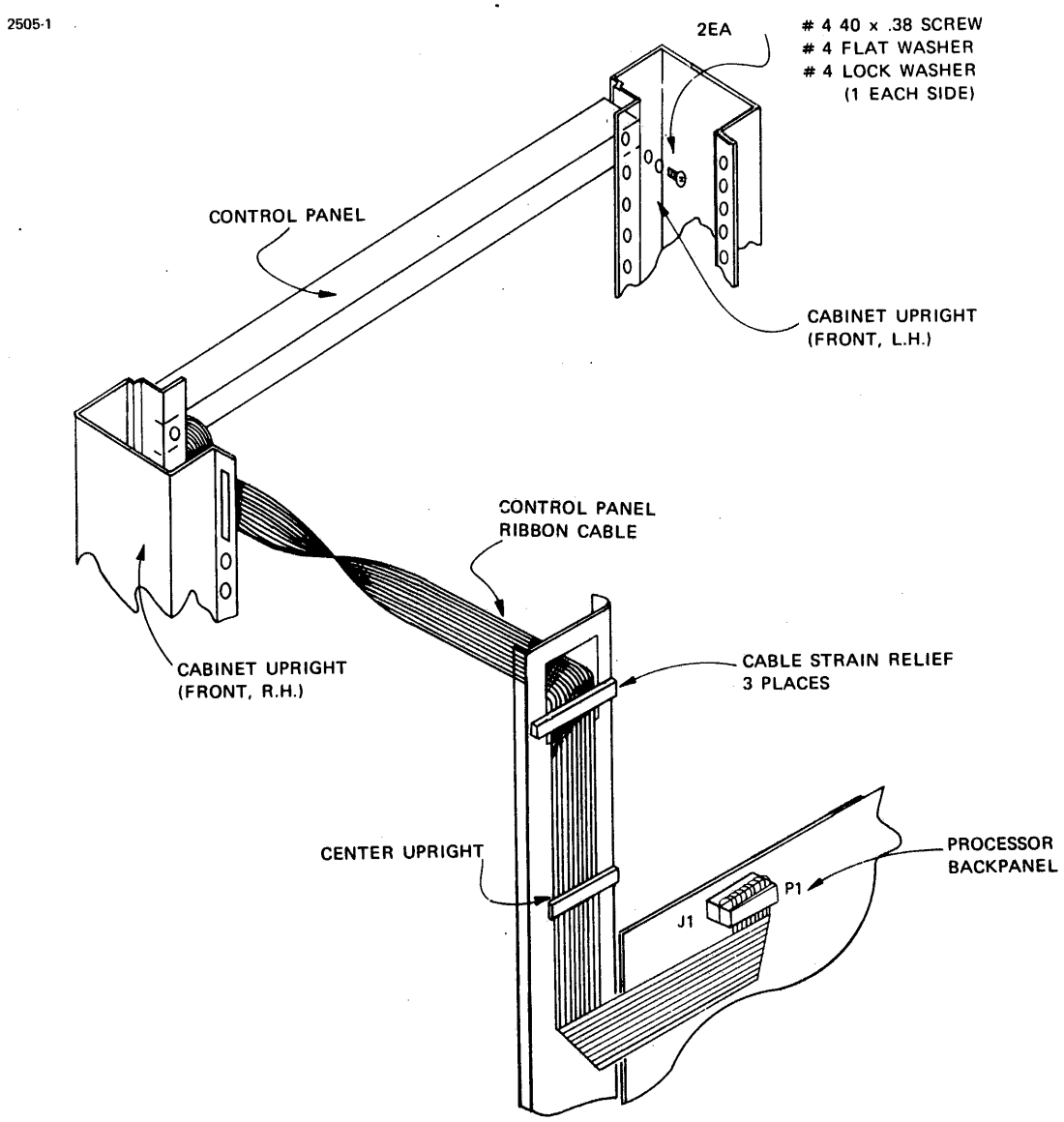


Figure 5-1 System Control Panel Installation (Cabinet Skins Omitted For Clarity)

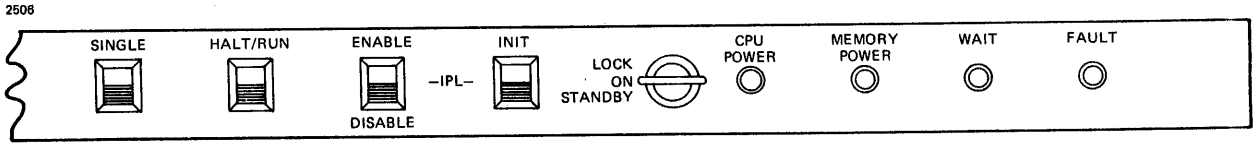


Figure 5-2 Function Switches and Indicators System Control Panel

CHAPTER 6
PROCESSOR AND MEMORY INSTALLATION

6.1 INTRODUCTION

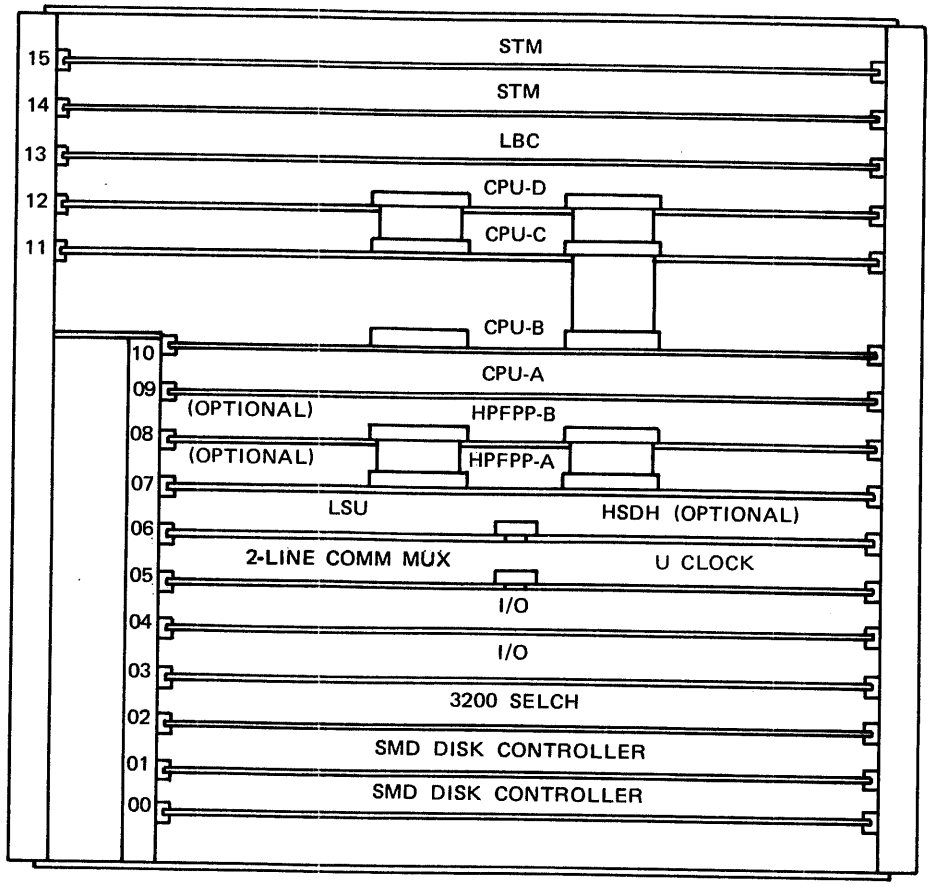
This chapter describes the installation of the Model 3210 Processor and memory. All processor and memory boards occupy slots in one of two basic system chassis, with or without floating-point, as shown in Figures 6-1 and 6-2.

The basic processor and memory consists of:

1 CPU-A board, 35-816 in slot 9
1 CPU-B board, 35-768 in slot 10
1 CPU-C board, 35-769 in slot 11
1 CPU-D board, 35-770 in slot 12
1 CPU-LBC board (4 Mb), 35-771F04 in slot 13
or
1 CPU-LBC board (8 Mb), 35-806F02 in slot 13
1 STM 35-764 in slot 14/15
1 cable 17-234F08 (50 pin)
1 cable 17-234F10 (50 pin, 3 header)

NOTE

Figures 6-1 and 6-2 show two separate chassis. Slots 7 and 8 in the floating-point chassis are dedicated slots and cannot be used for other boards.



NOTE: THESE ARE TWO SEPARATE CHASSIS. SLOTS 7 AND 8 IN THE FLOATING-POINT CHASSIS ARE DEDICATED SLOTS AND CANNOT BE USED FOR OTHER BOARDS.

Figure 6-1 Front View of Chassis With Floating-Point

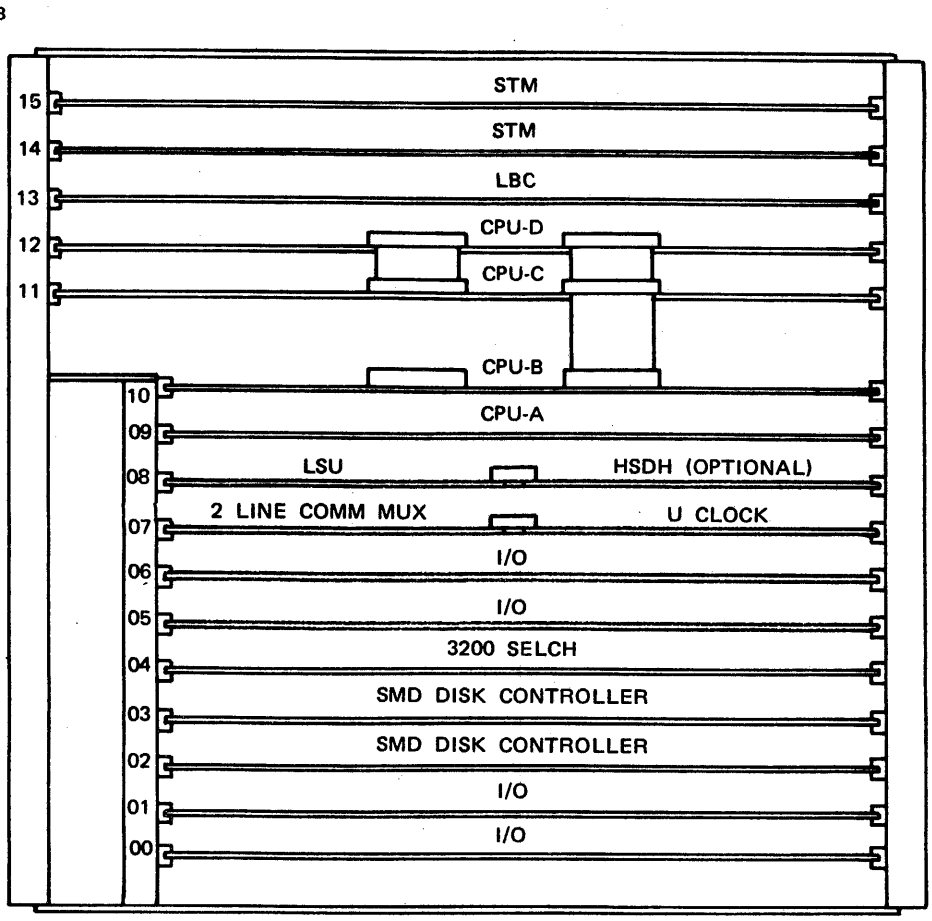


Figure 6-2 Front View of Chassis Without Floating-Point

6.2 CPU-A (35-816)

The CPU-A board must always be installed in slot 9. Before installing this board, ensure that the privileged illegal ROM and option strapping are correct. The privileged illegal read-only memory (ROM) (19-188F25) is in location A39.

The COMM option and the HPFPP option must be disabled by strapping TPA to TPG and TPC to TPG, respectively; the DROMs are enabled by strapping TPE to TP4.

The Test Aid DIP switches in the front of the CPU-A board must be in the OFF (open) position. The CPU-A board can then be installed.

6.3 CPU-B (35-768)

The CPU-B board must always be installed in slot 10. There is no strapping on the CPU-B board.

6.4 CPU-C (35-769)

The CPU-C board must always be installed in slot 11 of the CPU chassis. This board contains the strapping required for allocating segments of memory to shared memory. At the time of manufacture, the board is strapped so that all memory is local. Memory can be allocated as shared memory in 1 Mb increments. Refer to the functional schematic for the CPU-C board, 35-769D02, Sheet 13, for strapping information.

6.5 CPU-D (35-770)

The CPU-D board must be installed in slot 12 of the CPU chassis. No strapping options are contained on this board. Certain straps located on this board are used for factory maintenance purposes. Refer to Chapter 15, Adjustments, for this information.

On the CPU-D board, the DMA system hangs up if the following straps have not been installed:

LOCATION	STRAP	
00A	10 to 72	
02A	09 to 73	
CONN 6	112-6(TPD)	113-6(TPC)

6.6 CPU-LBC (35-771F04 (4 Mb) or 35-806F02 (8 Mb))

The CPU-LBC board is always installed in slot 13. Before installing the LBC, check CONN 5 for the following:

- 215-5 (TP10) connected to 216-5 (TP9)
- 221-5 (TP4) connected to 222-5 (TP3)
- TPA connected to TPB (35-806F02 only)
- No connection between 224-5 (TP1) and 223-5 (TP2)
- No connection between 214-5 (TP11) and 213-5 (TP12)
- No connection between 217-5 (TP8) and 218-5 (TP7)

6.7 STORAGE MODULE (STM)

The STMs must be installed in ascending slots beginning with slot 14. Refer to Chapter 14 for proper setting of the module select switch at location A46 on each STM.

6.8 DISK CONTROLLER

The basic system comes equipped with a 35-811 Disk File Controller and a 35-627 Disk Controller installed in the first two slots immediately below the selector channel (SELCH). Detailed information for these boards is provided in the Removable Media Mass Storage Module (MSM) Maintenance Manual, Publication Number 29-644. A functional schematic and assembly drawing for the 35-811 Disk File Controller are provided at the back of this manual.

The file control board is configured to operate with one of three CMD drives as shown in Table 6-1. All drives connected to the controller must be of the same CMD type.

TABLE 6-1 CMD DRIVE TYPE SELECTION

STRAPPING	CMD DRIVE TYPE 32MB	64MB	96MB
B	B1 - B2	B2 - G B1 - N/C	B2 - G B1 - N/C
C	C2 - G C1 - N/C	C1 - C2	C2 - G C1 - N/C
D	D2 - G D1 - N/C	D2 - G D1 - N/C	D1 - D2

6.9 PROCESSOR CABLING

Install the following cables:

CABLE	FROM	TO	TO
17-234F08 (50 pin)	CPU-D CONN 5	CPU-C CONN 5	NA
17-234F10 (50 pin)	CPU-D CONN 4	CPU-C CONN 4	CPU-B CONN 3

6.10 CPU MULTIPLEXOR BUS EXPANSION

6.10.1 Sub-Channel Controller

The Sub-Channel Controller (SCC) is used to extend the 3210 CPU multiplexor bus to one I/O expansion cabinet. The following is a guide for installing the SCC in the CPU chassis:

BACKPANEL PIN IDENTIFICATION

XX_1X_1 - YYZZ

X = ROW NUMBER
X_1X_1 = PIN NUMBER
YY = SLOT
ZZ = CONNECTOR

The SCC must reside in slot 0 of the CPU chassis. Strap the SCC as follows:

1. Set the switch at location A28 to X'0'.
2. Remove the following straps:

   A to A, C to D, B to B, E to F, 1 to 2

3. Add the following straps:

   1 to 3, C to G

Perform the following CPU backpanel wiring modifications:

1. Remove multiplexor bus wires on slot '0' connector 1, pins 11 through 26, rows 1 and 2.

2. Perform the following RACK0/TACK0 rerouting on the CPU chassis. The twisted pair wire (yellow/black) must be used for long jumpers. See Figure 6-3.

   a. Remove wire jumper between 222-0000 and 122-0801 (3210 without HPFPP) or 122-0601 (3210 with HPFPP).

   b. Remove wire jumper between 122-0000 and 222-0100.

   c. Remove RACK0/TACK0 jumpers on slot 0, both connectors 0 and 1.

   d. Add twisted pair wire between the following pins:

      3210 with HPFPP

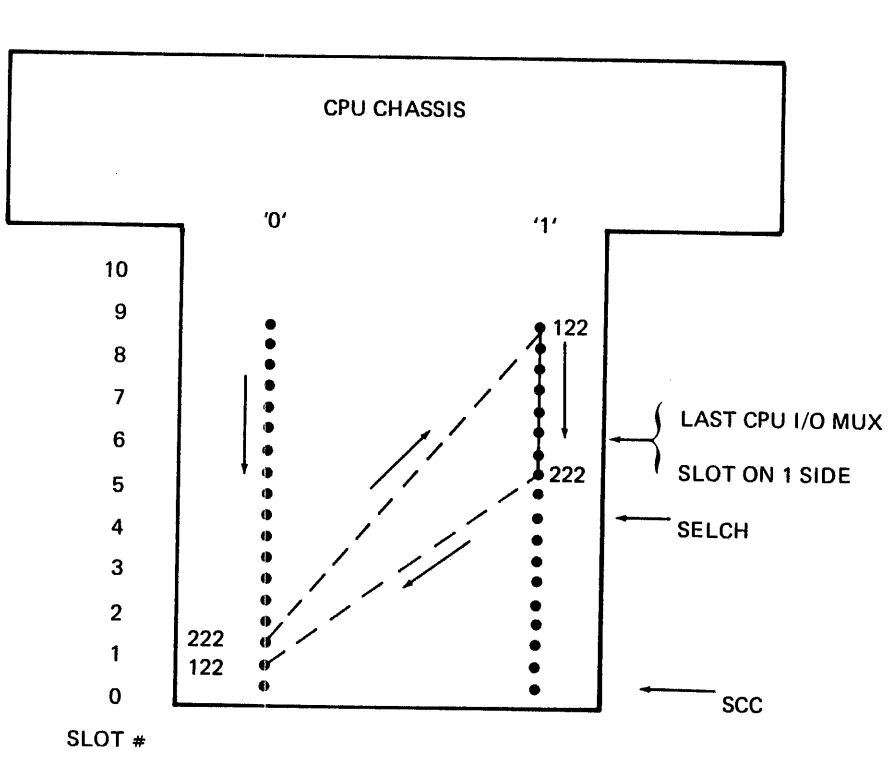
      122-0601 ----> 222-0100 (yellow)
      140-0601 ----> 140-0100 (black)

      3210 without HPFPP

      122-0801 ----> 222-0100 (yellow)
      140-0801 ----> 140-0100 (black)

   e. Add twisted pair wire between the following pins:

      122-0000 ----> 222-YY01 (yellow)
      140-0000 ----> 140-YY01 (last I/O slot on CONN1) (black)



NOTE

---- denotes twisted pair wire.

Figure 6-3 Rear View of CPU Chassis (RACK0/TACK0 Routing)

6.10.2 I/O Expansion Chassis Wiring Instructions For Extended CPU Multiplexor Bus

RACK0/TACK0 rerouting is shown in Figure 6-4. Perform the following steps:

1. On all I/O expansion chassis, remove the following wires:

   134-0700 to 122-0701
   122-0700 to 222-0001

2. On all I/O expansion chassis (except the top most chassis) add the following wire:

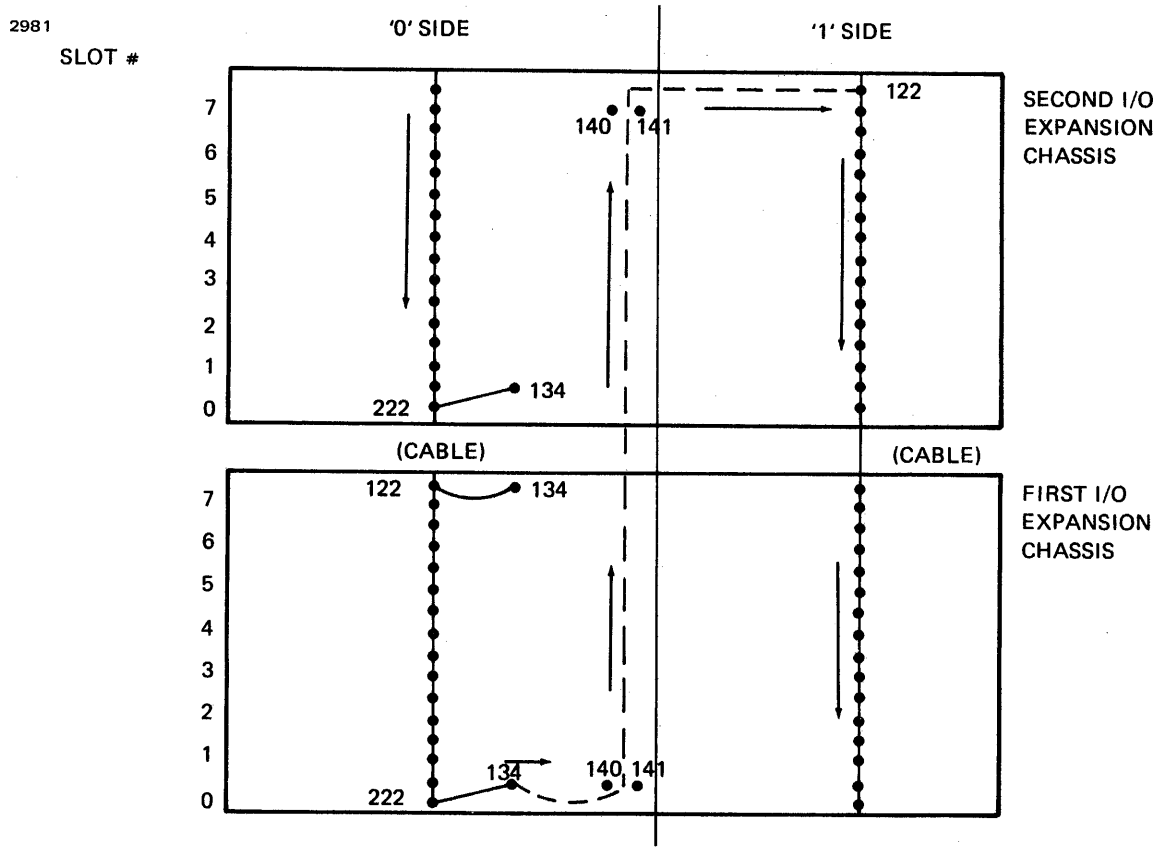
   134-0700 to 122-0700

3. RETACK0 Routing. Twisted pair wire (yellow/black) must be used.

Last I/O slot on Connector 0 to the first I/O slot on Connector 1.

134-0000 to 122-YY01 (yellow)
140-0000 to 140-YY01 (black)

Route wire between pins 140-YY00 and 141-YY00 of all I/O slots.



NOTE

---- denotes twisted pair wire.

Figure 6-4 Rear View of I/O Expansion Chassis Showing RACK0/TACK0 Routing

CHAPTER 7
BLOCK DIAGRAM ANALYSIS

7.1 INTRODUCTION

This chapter provides an overview of the Model 3210 Processor. Refer to Functional Schematic 01-158D08, Sheet 1, for a block diagram. Each board in the Central Processing Unit (CPU) is discussed individually in order to understand how the logic is partitioned within the CPU. This understanding is necessary in order to isolate faults to the board level.

7.2 SYSTEM ORGANIZATION

The CPU is organized between three 32-bit buses: the A, B, and S buses. The A bus presents data to the Arithmetic Logic Unit (ALU). The B bus presents data to the ALU, HPFPP, and Link Register. The S bus transfers the ALU output data to the appropriate destination. The source and destination of the A, B, and S buses and the functions performed by the ALU are controlled by microinstructions contained in the control store.

7.3 CPU-A BOARD

The CPU-A board contains the heart of the microprocessor which is used to emulate the instruction set. This board houses all elements of control store for the machine, the control store addressing, interrupt handling, and power fail/initialize control.

7.3.1 Fixed Control Store (FCS)

Fixed Control Store (FCS) consists of 2 k words, 32 bits each, of Read-Only-Memory (ROM) which is a high-speed, solid-state, nonvolatile memory. Each word in FCS is 32 bits long and represents one microinstruction. Each microinstruction read out of FCS is placed in the 32-bit ROM Data Register (RDR). RDR is the instruction register for the microprocessor and drives the RD bus. Most microinstructions are executed in one machine cycle of 200 nanoseconds. RD bits are decoded to direct the processor through its operations. The meaning of the microinstruction word is explained in Chapter 8.

7.3.2 ROM Data Register (RDR)

The ROM Data Register (RDR) is a 32-bit register which is loaded at the beginning of every machine cycle with microinstructions fetched from control store. The RDR drives the RD bus. This register can also be described as a pipeline register, since it allows for overlapping of ROM access and instruction execution.

7.3.3 Control Store Address Register (CSAR)

Locations in control store are addressed by the 12-bit Control Store Address Register (CSAR). Microinstructions are normally located at sequential addresses in the control store. The CSAR is an up-counter which increments by one as each new microinstruction is read into the RDR. The CSAR, therefore, holds the address of the next sequential microinstruction to be executed. When it becomes necessary to jump out of sequence, the CSAR can be loaded with a new address from the RDR register, the Decoder Read-Only-Memories, the Link Register, or the priority interrupt encoder; or it can be cleared by the hardware to zero for an instruction read or system initialization.

7.3.4 Link Register (LR)

A branch and link capability is provided in this machine by means of the 12-bit Link Register (LR).

When the microprogram specifies Link, the LR is unconditionally loaded with the address of the current microinstruction being executed and is automatically incremented by one prior to the next system clock. When the microprogram executes a Branch/Return, the CSAR is loaded from the LR.

The LR may also be loaded from the B bus in order to nest microsubroutines.

7.3.5 Decoder Read-Only-Memory (DROM) and Privileged Illegal ROM (PILROM)

The DROMs are constructed using three 512x4-bit ROMs which are addressed by the 8-bit op-code field of the Instruction Register. They contain the D1 and D2 vector addresses which are entry points for instruction emulation routines. The microprogram interrogates the D1 address at instruction read time and the D2 vector during instruction emulation. The 12 bits of the resulting readout are jammed into the CSAR, resulting in an automatic transfer to an address which is related to the user's operation code.

The Privileged/Illegal ROM (PILROM) is also addressed by the 8-bit op-code field and is interrogated at D1 time to supply privileged instruction and illegal instruction.

7.3.6 Priority Interrupt Encoder (PIE)

The priority interrupt encoder provides high-speed interrupt handling to the microprogram. It monitors 14 interrupt lines, sets their priorities, and when interrogated by the microprogram, provides a vectored branch into the interrupt service table in the microcode.

7.3.7 Initialize Logic

System initialization is controlled on the CPU-A board by the initialize logic. This logic interfaces to the power system and, together, they monitor and control the DC power required in the system. Early Power Fail (EPF) and Primary Power Fail (PPF) interrupts are also generated by this logic.

7.3.8 Console Support Logic

The console support logic monitors the EXECUTE/HALT switch and the single switch from the System Control Panel and creates console attention interrupts to the microprogram.

7.3.9 Test Aid

The CPU-A has a built-in test aid. Sixteen switches in two DIP packages at the front of the CPU-A board provide CSAR match/SYNC, microcode single step, MAT or MPE fault match, and external match capabilities for troubleshooting.

7.4 CPU-B BOARD

The CPU-B board is the processor's arithmetic board. It contains a 32-bit ALU which is fed by the 32-bit A multiplexor and a 32-bit B multiplexor, a 32-bit shift register, the PSW, a flag register, and the A and B register stacks.

7.4.1 Arithmetic Logic Unit (ALU)

The Arithmetic Logic Unit (ALU) is 32 bits wide with full look-ahead carry logic. It is fed by the 32-bit A and B multiplexors and its output generates the S bus.

7.4.2 A Multiplexor

The 32-bit A multiplexor feeds the ALU from either the A bus or the shift register.

7.4.3 B Multiplexor (B Bus Shifter)

The 32-bit B multiplexor feeds the A input to the ALU and is used as the input to the register stacks for divide operations. It also performs all of the ALU shift operations defined in the shifter microcode field.

7.4.4 32-Bit Shift Register

This register can be loaded from the S bus, shifted left or shifted right (one place per processor clock), and can be presented to the B bus or to the ALU via the A multiplexor.

7.4.5 Flag Register (FLR)

The Flag Register (FLR) is a 4-bit register containing the following flags: Carry (C), Overflow (V), Greater than Zero (G), and Less than Zero (L). These flags are modified at the conclusion of arithmetic and logical microoperations to reflect the result of the operation. The FLR is loaded from bits 28:31 of the S bus when either the FLR or the Program Status Word (PSW) is the specified destination register.

7.4.6 Program Status Word (PSW)

The Program Status Word (PSW) is a 24-bit register used to indicate the system status relative to the user program being emulated. Bits 8:27 of the PSW are used as interrupt masks to define the operational status or mode of the user-level processor. Some of the PSW bits have hardware significance, while others are of significance only to the microprogram. Bits 28:31 of the PSW make up the Condition Code (CC) field which reflects the result of the previous user instruction.

The status portion of the PSW is 32 bits long. Only 24 bits, however, are implemented in the hardware of this machine. Bits 0:7 are not used and are forced to zero.

The CC may be updated only from the FLR. When PSW is the specified destination register, bits 8:27 of the S bus are loaded into bits 8:27 of the PSW, and S bus bits 28:31 are captured in the FLR. The CC field remains unchanged until the microprogram causes it to be updated from the FLR when the jam bit is set in the microword. The PSW is unloaded onto the A bus.

7.4.7 A and B Register Stacks

The 32-bit A and B register stacks hold the 4 microregisters, 8 general register sets of 16 registers each, and an alternate register set of 16 registers. These stacks are loaded

simultaneously from the S bus (from the B multiplexor in the case of a divide) and always hold identical data. The A and B register stacks can be unloaded by the A and/or B source field of the microword tc their respective latch registers.

7.4.8 Register Stack Control

The register stack control provides address and timing for the register stacks.

7.5 CPU-C BOARD

The CPU-C board provides an interface between the central processing unit and memory system. All registers associated with memory addressing and memory data are located on this board. This unit also contains the Memory Address Translator (MAT). The MAT provides dynamic address relocation and memory protection.

7.5.1 Location Counter (LOC)

The Location Counter (LOC) is a 24-bit addendum to the PSW which holds the address of the next user instruction to be executed in main memory. The LOC is implemented as an up-counter which increments by two for each halfword of data required to execute an instruction.

7.5.2 Processor Memory Address Logic

The Memory Address Register (MAR) is a 24-bit register which contains the address of main memory to be accessed. The LOC is selected as the address to memory during instruction reads through the Program Address (PA) multiplexor; in all other cases, the PA selects the MAR.

Each time a memory reference is made, including instruction reads, the output of the PA multiplexor is loaded into an auxiliary address register (ZMAR). If a fault is detected in the system, the data in the ZMAR remains unchanged until directed by the microprogram. The first time, after a fault, that MAR is the selected B source, the data contained in the ZMAR is unloaded.

On a processor operation to memory, the 13 most significant bits of the program address are subject to relocation and placed on the LMA bus, while the 11 least significant bits are placed on the bus unchanged.

7.5.3 Memory Address Translator (MAT)

Dynamic memory relocation is provided when enabled by bit 21 of the PSW. This is accomplished by adding the relocation field of the selected segmentation register to bits 16:20 of the program

address which has bits 8:15 forced to zero. This relocated address is then used to access memory.

The segmentation registers also contain the necessary information to provide memory access protection for the selected segment.

7.5.4 Memory Data Register (MDR)

Processor data from/to main memory is contained in the Memory Data Register (MDR). This register is 32 bits wide and is loaded from the S bus before initiating a memory write operation. The data contained in the MDR is gated onto the local memory bus (MDS bus) for writes to local memory.

The data, when it becomes available on a memory read, is loaded into the MDR from the MDS bus or EDMA bus. The microprogram can then access the data by specifying the MDR as the B bus source.

7.6 CPU-D BOARD

The CPU-D board is the machine's control board. The system clocks for the processor, as well as I/O, EDMA, and memory control logic, are all contained on this unit. Refer to Chapter 12 for a detailed analysis of the CPU-D and for all information concerning clocks and control logic.

7.6.1 Instruction Register (IR)

The Instruction Register (IR) is a 16-bit register divided into three fields: operation code (OP), user destination (YD), and user source (YS). The IR is loaded during an instruction fetch, when the data is available from memory.

7.6.2 Input/Output (I/O)

The 16-bit parallel Input/Output (I/O) bus is used to send and receive information to and from device controllers. These operations are achieved by gating S bus data onto the D bus and activating an I/O control line, or by activating a control line and gating D bus data onto the internal B bus.

7.6.3 Extended Direct Memory Access (EDMA) Registers

Data paths for Extended Direct Memory Access (EDMA) operations to memory are contained within the CPU-D board. The local memory address on an EDMA operation is loaded into the EDMA Memory Address Register (EMAR) and sent to the LMA bus. Data on write operations from an EDMA device, e.g., a BSELCH, is loaded into the EDMA Memory Data Register (EMDR) and presented to the local memory bus through the MDS multiplexor. For memory read cycles, data goes from memory to the EMDR and then onto the EDMA bus.

7.7 LOCAL BANK CONTROLLER (LBC)

This board provides an interface between the processor and the storage module (main memory) in the system (refer to Chapters 13 and 18). The major functions of this module are the generation of the necessary timing for the storage modules, error code generation and checking, error logging, and memory refresh control.

Address and data information between the processor and main memory is latched in registers contained on the LBC. Refer to Chapters 13 and 18 for detailed descriptions of the timing and control logic on this board.

7.7.1 Input Data Register (IDR)

At the start of a memory write operation, the data on the MDS bus (MDS000:310) from the processor is latched in the Input Data Register (IDR). This data is then presented to the error correction logic in order to generate the seven parity bits used for error correction. The data, along with the parity bits, is then gated to the local memory bus (LMB000:380).

7.7.2 Output Data Register (ODR)

For memory read operations, good data (data which has been checked and corrected if necessary) is latched in the Output Data Register (ODR). The ODR is constructed using tri-state devices. These outputs are used to form the bidirectional MDS bus.

7.7.3 Good Data Register (GDR)

The Good Data Register (GDR) is used to latch checked/corrected data to be returned to the processor on memory read cycles, or which is to be written into memory. Data is written to memory from the GDR any time a memory read is initiated and an error is detected and corrected, or on a partial word write operation (byte or halfword write) whether or not an error has been detected.

7.7.4 Uncorrected Data Register (UDR)

Data read from memory is stored into the Uncorrected Data Register (UDR). This data is used as an input to the error correction/detection logic along with the parity bits contained in the Uncorrected Parity Register (UPR).

If the data is found to be valid, this good data is loaded into the GDR, unmodified. If a single-bit error is detected, the error correction logic generates correct data and loads it into the GDR where it is then transferred to the applicable destination.

7.7.5 Error Logger

Each time an error is detected on a read from memory, information concerning the type of error (single-bit or multiple-bit) and the chip location for single-bit errors are stored in a random access memory. The data in this memcry can be accessed by the processor by issuing a read error logger command.

CHAPTER 8
MICROWORD DESCRIPTION

8.1 INTRODUCTION

The microword consists of groups of data bits that are fetched from control store as a 32-bit microinstruction word. Groups of ROM Data (RD) bits of the microinstruction control various hardware functions of the microprocessor. The specific function of the data bit groups may be altered by the format of the microinstruction, the operation modifiers, or the specific source or destination register. The following is a breakdown of these data bit groups which are called instruction word fields. Refer to Table 8-1 and Figure 8-1 during this description.

8.2 MEMORY CONTROL FIELD (MC) - RD BITS 0, 1, 2, AND 3

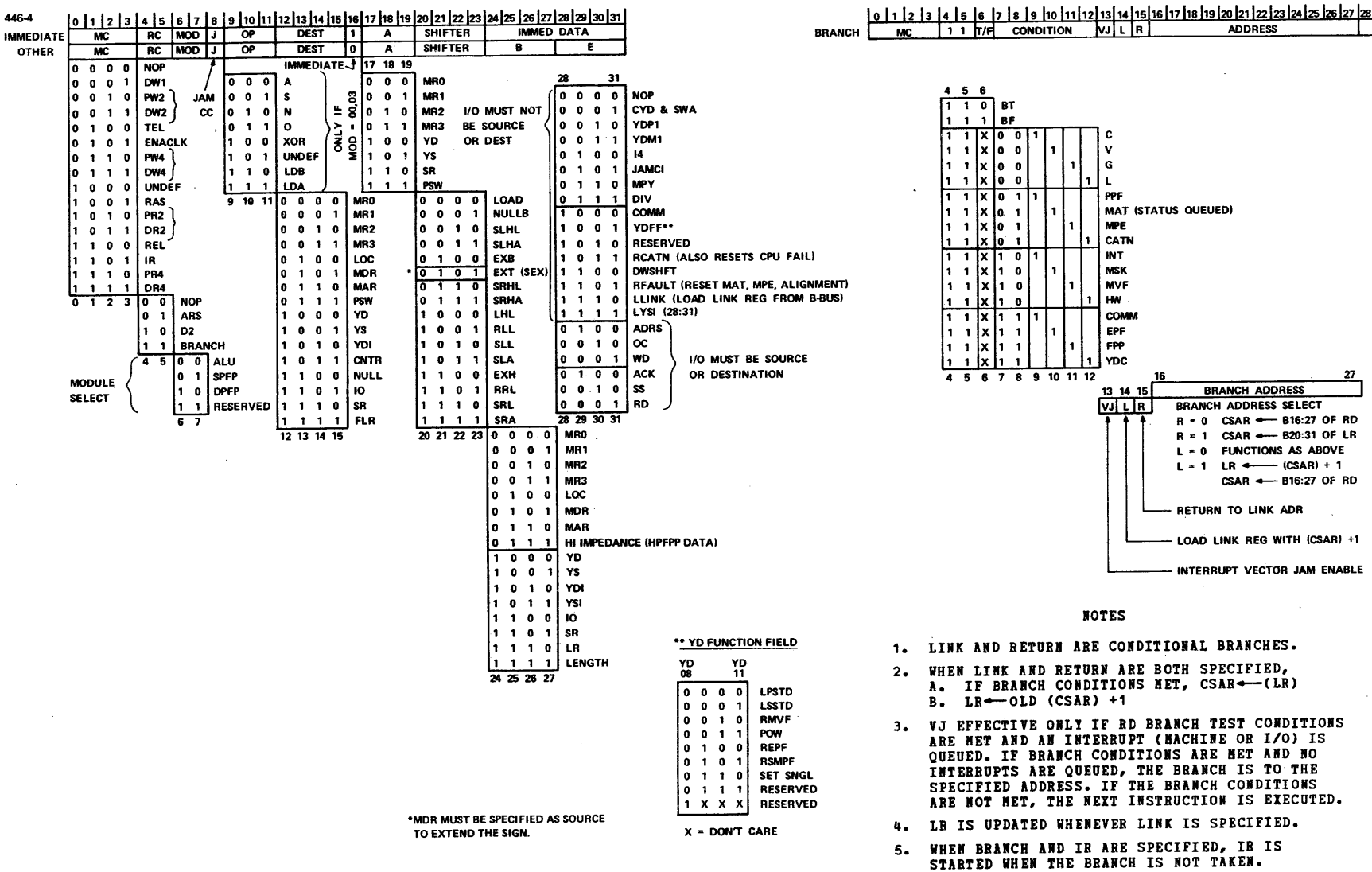
The Memory Control Field (MC) is primarily used either to read from, or to write into, memory. The memory address selected depends upon the contents of the Location Counter (LOC) (during IR only) or the Memory Address Register (MAR) and the bias added by the MAT. The type of memory operation (read or write) and the amount of data fetched is controlled by the MC. Privileged memory operations disable the relocation and protection of the MAT. Fullword memory operations must be aligned on fullword memory address boundaries. Halfword memory operations must be on halfword or fullword boundaries. Violation of these alignments causes alignment faults. All memory read operations access memory as a fullword. The MC causes the processor hardware to steer and load only the required portion of the data.

NOTE

All MC options which cause data to be written to main memory (with the exception of TEL) also cause the ECC bits, corresponding to the fullword receiving the data, to be updated.

TABLE 8-1 INSTRUCTION WORD FIELDS

FIELD	MEANING
A	Selects register to be used as first operand. Data is available on the A bus.
ADDRESS	Specifies branch address data to be loaded into the CSAR.
B	Selects register to be used as second operand. Data is available on the B bus.
COND	Specifies conditions tested for conditional branch.
D	Selects destination register to receive the result. Data is available on the S bus.
DATA	Specifies immediate data as second operand on B bus.
E	Specifies the extended options to be performed.
I	Enables loading of immediate data to the B bus. The data used is controlled by the D field.
J	Causes condition code to be updated, or controls data direction (read or write) when module 3 (WCS) is selected.
L	Causes the link register to be loaded with the address of the current microinstruction plus one.
R	Specifies that a branch to the address contained in the link register is performed if the specified branch conditions are met.
MC	Memory control field specifies type of memory operation.
MOD	Selects active CPU, fixed-point ALU, or floating-point processor.
OP	Specifies the fixed-point or floating-point operation.
RC	Control store addressing and alternate register set control field.
SHIFTER	Specifies B bus shifter function.
T/F	Specifies whether COND must be true or false to branch.
VJ	Enables interrupt vector jam when branch is taken.
YDFF	Specifies extended operations addressed by the YD field of the instruction register and enabled by the E field.



*MDR MUST BE SPECIFIED AS SOURCE TO EXTEND THE SIGN.

** YD FUNCTION FIELD

YD 08	YD 11	
0 0 0	0	LPSTD
0 0 0	1	LSSTD
0 0 1	0	RMVF
0 0 1	1	POW
0 1 0	0	REPF
0 1 0	1	RSMPF
0 1 1	0	SET SNGL
0 1 1	1	RESERVED
1 X X	X	RESERVED

X = DON'T CARE

NOTES

1. LINK AND RETURN ARE CONDITIONAL BRANCHES.
2. WHEN LINK AND RETURN ARE BOTH SPECIFIED,
   A. IF BRANCH CONDITIONS MET, CSAR←(LR)
   B. LR←OLD (CSAR) +1
3. VJ EFFECTIVE ONLY IF RD BRANCH TEST CONDITIONS ARE MET AND AN INTERRUPT (MACHINE OR I/O) IS QUEUED. IF BRANCH CONDITIONS ARE MET AND NO INTERRUPTS ARE QUEUED, THE BRANCH IS TO THE SPECIFIED ADDRESS. IF THE BRANCH CONDITIONS ARE NOT MET, THE NEXT INSTRUCTION IS EXECUTED.
4. LR IS UPDATED WHENEVER LINK IS SPECIFIED.
5. WHEN BRANCH AND IR ARE SPECIFIED, IR IS STARTED WHEN THE BRANCH IS NOT TAKEN.

Figure 8-1 Microword Format

NOTE

The E field, in formats other than register-to-register immediate data, identifies additional operations to be performed or options to the primary operation.

The MC field, in all formats, controls main memory accesses.

MC Value

0000 - NOP — No memory operation is attempted.

0001 - DW1 — Nonprivileged byte data write. Byte of data contained in the Memory Data Register (MDR) is written to the byte memory address specified by the MAR. Bits 16:31 of the MDR are gated to the memory bus. The data to be written must be in the appropriate byte position of the least significant halfword of MDR.

0010 - PW2 — Privileged halfword data write. Halfword of data contained in MDR bits 16:31 is written to the halfword specified by the MAR.

0011 - DW2 — The same operation as PW2, except that the MAR address may be relocated and/or protected by the MAT.

0100 - TEL — Test error logger operation causes a byte write operation to the address specified by MAR. Bits 24:31 of MDR are written into memory. The byte write is privileged and the error correction logic is disabled; thus, if the byte written is different from the previous contents, the Error Correction Code (ECC) in memory is incorrect. No error is logged in the error logger.

0101 - ENACLK — No memory operation is implied. Destination clocks for all machine registers (except YDI, flags, and CSAR) are disabled whenever a fullword or halfword boundary error, ECC error, or MAT violation occurs. To allow loading machine registers following such a condition, the ENACLK option must be specified.

0110 - PW4 — Privileged fullword memory write. The data contained in MDR 0:31 is written to the address specified by MAR.

0111 - DW4 — Nonprivileged fullword memory write. The relocation and protection of the MAT is enabled.

1000 - UNDEF The MC and the hardware are undefined.

1001 - RAS The halfword addressed by MAR is read into MDR, bits 16:31. Bit 16 of the data is set, and the halfword is written back to memory. The MAT is not disabled. The data in MDR, bits 16:31, reflects the previous state of the data in memory. Bits 0:15 of the MDR are undefined.

1010 - PR2 Privileged halfword read from memory. The MAT is disabled. A halfword of data selected by the address in MAR is loaded into MDR 16:31. Bits 0:15 of the MDR are undefined. The address is in the MAR.

1011 - DR2 Nonprivileged halfword read from memory. The MAT is enabled. Data is loaded into MDR in the same manner as PR2. The address is in the MAR.

1100 - REL Read error logger is treated as a PR2. The error logger, at the address corresponding to the contents of MAR, is interrogated. Error logger data replaces the contents of MDR bits 16:31. Bits 0:15 of the MDR are undefined.

1101 - IR Instruction read from memory. This operation causes a fullword read from memory. The data from the read is loaded into the instruction register and the MDR. The address is specified by the location counter. If CNTR contains a nonzero value, the IR is deferred until the CNTR equals zero.

1110 - PR4 Privileged fullword memory read operations. MDR bits 0:31 are loaded with the data read from the fullword address contained in the MAR. The MAT is disabled during the memory cycle.

1111 - DR4 Nonprivileged fullword memory read operation. Similar to PR4, except that the MAT is enabled.

8.3 ROM CONTROL FIELD (RC) - RD BITS 4 AND 5

00 - NOP Normal operation microinstructions are fetched in sequential order. The CSAR is incremented by one, unless IR is specified in the MC field.

01 - ARS Sequential order of microinstruction fetch is unaffected. The alternate register set is selected for use with a general register. The user-level machine has no access to this set of registers.

10 - D2 — Jam the address which is contained in Decoder ROM 2 (DROM2) into the CSAR. The address specified by DROM2 is controlled by the contents of the instruction register.

11 - BRANCH — Allows the CSAR to be jammed by RD bits 16:27 if conditions are met.

8.4 MODULE SELECT FIELD (MOD) - RD BITS 6 AND 7

00 - ALU — The microinstruction operation uses the fixed-point ALU and the fixed-point operation codes (RD bits 9, 10, and 11).

01 - SPFP — The microinstruction operation uses the High Performance Floating-Point Processor (HPFPP) for single-precision operations. Single-precision registers are used. The fixed-point ALU is conditioned to load the B bus to the S bus. The type of single-precision operation is defined by RD bits 9, 10, and 11.

10 - DPFP — The microinstruction operation uses the HPFPP for double-precision operations. Double-precision registers alone are affected by the operation. The fixed-point ALU is conditioned to load the B bus to the S bus. The type of double-precision operation is defined by bits 9, 10, and 11.

11 - RESERVED

8.5 JAM CONTROL - RD BIT 8

RD bit 8 is used to jam the flag register into the condition code portion of the PSW.

8.6 OPERATION INSTRUCTION WORD FIELD - RD BITS 9, 10, AND 11

Refer to Table 8-2 for fixed-point operations. Tables 8-3 and 8-4 list the single-precision and double-precision floating-point operations, respectively.

TABLE 8-2 FIXED-POINT ALU OPERATIONS

RD BITS			MNEMONIC	MEANING
9	10	11		
0	0	0	A	Add the A bus and B bus shifter output data.
0	0	1	S	Subtract the A bus and B bus shifter output data.
0	1	0	N	AND the A bus and B bus shifter output data.
0	1	1	OR	OR the A bus and B bus shifter output data.
1	0	0	XOR	Exclusive-OR the A bus and B bus shifter output data.
1	0	1	UNDEF	Undefined operation
1	1	0	LDB	Load B bus shifter output data to S bus.
1	1	1	LDA	Load A bus data to the S bus.

TABLE 8-3 SINGLE-PRECISION FLOATING-POINT OPERATIONS

RD BITS			MNEMONIC	MEANING
9	10	11		
0	0	0	RCC	Read condition code - place contents of HPFPP flag register on B bus.
0	0	1	RRE	Read register single-precision and place contents on B bus.
0	1	0	LE	Load single-precision data from B bus to HPFPP.
0	1	1	CER	Compare single-precision data register-to-register.
1	0	0	AER	Add single-precision data register-to-register.

TABLE 8-3 SINGLE-PRECISION FLOATING-POINT OPERATIONS (Continued)

RD BITS			MNEMONIC	MEANING
9	10	11		
1	0	1	SER	Subtract single-precision data register-to-register.
1	1	0	MER	Multiply single-precision data register-to-register.
1	1	1	DER	Divide single-precision data register-to-register.

TABLE 8-4 DOUBLE-PRECISION FLOATING-POINT OPERATIONS

RD BITS			MNEMONIC	MEANING
9	10	11		
0	0	0	LW	Load word - load most significant 32-bit portion of 64-bit double-precision floating-point number.
0	0	1	RRD	Read register double-precision and place contents on B bus.
0	1	0	LD	Load least significant 32-bit portion of 64-bit double-precision floating-point number.
0	1	1	CDR	Compare double-precision register-to-register.
1	0	0	ADR	Add double-precision register-to-register.
1	0	1	SDR	Subtract double-precision register-to-register.
1	1	0	MDR	Multiply double-precision register-to-register.
1	1	1	DDR	Divide double-precision register-to-register.

8.7 DESTINATION INSTRUCTION WORD FIELD - RD BITS 12, 13, 14, AND 15

Result data on the S bus is loaded into the specified destination. (Refer to Table 8-5.)

TABLE 8-5 DESTINATION REGISTERS

RD BITS				MNEMONIC	MEANING
12	13	14	15		
0	0	0	0	MR0	Microregister 0
0	0	0	1	MR1	Microregister 1
0	0	1	0	MR2	Microregister 2
0	0	1	1	MR3	Microregister 3
0	1	0	0	LOC	Location counter
0	1	0	1	MDR	Memory data register
0	1	1	0	MAR	Memory address register
0	1	1	1	PSW	Program status word
1	0	0	0	YD or ARSYD	General register specified by YD field of IR
1	0	0	1	YS or ARSYS	General register specified by YS field of IR
1	0	1	0	YDI	YD field of IR
1	0	1	1	CNTR	Counter
1	1	0	0	NULL	No destination. Used when the HPFPP is the implied destination.
1	1	0	1	IO	Used for output I/O instructions
1	1	1	0	SR	Shift register
1	1	1	1	FLR	Flag register

8.8 IMMEDIATE DATA CONTROL BIT - RD BIT 16

Microinstructions other than Branch may use the immediate data control bit. When this bit is active, RD bits 24:31 provide the least significant eight bits into the B bus shifter. The remainder of the B source is null.

When the PSW is the destination, bits 28:31 of the S bus are captured in the Flag Register (FLR). The PSW condition code field is updated from the FLR only when the JAM option is specified in the microinstruction word.

When the destination is YD or YS, the general or scratchpad register whose number is in the YD or YS field of IR receives the S bus data. The current set is selected by bits 24:27 of the PSW. When module 1 or 2 is selected (by RD bits 6 and 7), the floating-point register specified by the YD field of IR receives the resultant floating-point data.

By specifying YDI as the destination, the YD field of IR is loaded from S bus bits 28:31. Microflags resulting from the operation are still valid in this case. YDI is also the destination for CYD&SWA, YDP1, and YDM1 E field options.

8.9 A SOURCE INSTRUCTION WORD FIELD - RD BITS 17, 18, AND 19

Refer to Table 8-6 for first operand registers. Data from the A source appears on the A bus input to the fixed-point ALU only.

TABLE 8-6 FIRST OPERAND REGISTERS (A BUS DATA)

RD BITS			MNEMONIC	MEANING
17	18	19		
0	0	0	MR0	Microregister 0
0	0	1	MR1	Microregister 1
0	1	0	MR2	Microregister 2
0	1	1	MR3	Microregister 3
1	0	0	YD or ARSYD	Register specified by YD field of IR
1	0	1	YS or ARSYS	Register specified by YS field of IR
1	1	0	SR	Shift register
1	1	1	PSW	Program status word

When module 0 is selected, use of YD or YS as a source causes the general or scratchpad register whose number is in the YD or YS field of IR to be presented to the A ALU input.

When module 1 or 2 is selected, the specified floating-point register is presented as the HPFPP first operand input.

8.10 SHIFTER INSTRUCTION WORD FIELD - RD BITS 20, 21, 22, AND 23

Refer to Table 8-7 for shifter options. The shifter alters B bus data according to the selected option. The modified data is supplied to the fixed-point ALU as second operand data.

TABLE 8-7 SHIFTER OPTIONS

RD BITS				MNEMONIC	ACTION
20	21	22	23		
0	0	0	0	-	No action - pass data unmodified.
0	0	0	1	NULLB	Force data to zero.
0	0	1	0	SLHL	Shift left halfword logical (bits 16:31) by one.
0	0	1	1	SLHA	Shift left halfword arithmetic (bits 16:31) by one.
0	1	0	0	EXB	Exchange bytes (least significant 16 bits).
0	1	0	1	EXT	Extend sign - MDR must be source.
0	1	1	0	SRHL	Shift right halfword logical (bits 16:31) by one.
0	1	1	1	SRHA	Shift right halfword arithmetic (bits 16:31) by one.
1	0	0	0	LHL	Load halfword logical.
1	0	0	1	RLL	Rotate left logical by one.
1	0	1	0	SLL	Shift left logical by one.
1	0	1	1	SLA	Shift left arithmetic by one.
1	1	0	0	EXH	Exchange halfwords.

TABLE 8-7 SHIFTER OPTIONS (Continued)

RD BITS				MNEMONIC	ACTION
20	21	22	23		
1	1	0	1	RRL	Rotate right logical by one.
1	1	1	0	SRL	Shift right logical by one.
1	1	1	1	SRA	Shift right arithmetic by one.

8.11 B SOURCE INSTRUCTION WORD FIELD - RD BITS 24, 25, 26, AND 27

Refer to Table 8-8 for second operand register options. Second operand register data is propagated onto the B bus. The data is then passed through the shifter to the ALU.

8.12 E INSTRUCTION WORD FIELD - RD BITS 28, 29, 30, AND 31

Refer to Table 8-9 for the extended field options. The extended field provides the ability to extend the function of any microinstruction without requiring the use of a second microinstruction.

TABLE 8-8 SECOND OPERAND REGISTERS

RD BITS				MNEMONIC	MEANING
24	25	26	27		
0	0	0	0	MR0	Microregister 0
0	0	0	1	MR1	Microregister 1
0	0	1	0	MR2	Microregister 2
0	0	1	1	MR3	Microregister 3
0	1	0	0	LOC	Location counter
0	1	0	1	MDR	Memory data register
0	1	1	0	MAR	Memory address register
0	1	1	1	CBUS	Data bus from modules 1 and 2

TABLE 8-8 SECOND OPERAND REGISTERS (Continued)

RD BITS				MNEMONIC	MEANING
24	25	26	27		
1	0	0	0	YD or ARSYD	Register specified by YD field of IR
1	0	0	1	YS or ARSYS	Register specified by YS field of IR
1	0	1	0	YDI	YD field of IR
1	C	1	1	YSI	YS field of IR
1	1	0	0	IO	Used for input I/O instructions
1	1	0	1	SR	Shift register
1	1	1	0	LR	Link register
1	1	1	1	LENGTH	Length in halfwords of last instruction fetched

TABLE 8-9 EXTENDED FIELD OPTIONS

RD BITS				MNEMONIC	MEANING
28	29	30	31		
0	0	0	0	-	No action
0	0	0	1	CYD&SWA	Clear YD field of IR and set wait indicator.
0	0	1	0	YDP1	Increment YD field of IR by one.
0	0	1	1	YDM1	Decrement YD field of IR by one.
0	1	0	0	I4	Increment the MAR by 4.
0	1	0	1	JAMCI	Jam carry in ALU (arithmetic mode only)
0	1	1	0	MPY	Multiply
0	1	1	1	DIV	Divide

TABLE 8-9 EXTENDED FIELD OPTIONS (Continued)

RD BITS				MNEMONIC	MEANING
28	29	30	31		
1	0	0	0	COMM	Data on S bus is gated onto the I/O bus and accepted by the communication assist unit.
1	0	0	1	YDFF	YD function field
1	0	1	0	UNNLD	Unnormalized floating-point load - defeats HPFPP normalizing logic.
1	0	1	1	RCATN	Reset console attention and CPU fail indicator.
1	1	0	0	DWSHFT	Doubleword shift
1	1	0	1	RFAULT	Reset MAT, MPE, and ALIGN errors.
1	1	1	0	LLINK	Load link register from B bus bits 20:31.
1	1	1	1	LYSI	Load YS field of IR from S bus bits 28:31.
0	1	0	0	ADRS	I/O must be destination. ADRS selects device on the I/O bus.
0	0	1	0	OC	I/O must be destination. Data on the I/O bus is command for selected device.
0	0	0	1	WD	I/O must be destination. Data on the I/O bus is character information for selected device.
0	1	0	0	ACK	I/O must be source. Interrupting device address is received.
0	0	1	0	SS	I/O must be source. The status data of a selected device is received.
0	0	0	1	RD	I/O must be source. Data is received from the selected device.

NOTE

I/O is neither a source nor a destination.

If the ARS bit is set in the RC field, all sources or destinations specifying YD or YS for module 0 or 3 operations access the alternate register set. This bit is set by the microcode assembler whenever ARSYD or ARSYS is specified in the microinstruction.

Specifying MDR as a source immediately following a memory read operation causes the processor to stop until memory data becomes available. After a fullword memory read, all 32 bits of MDR are loaded.

NOTES

EXT may be specified only if the B source is MDR.

If MDR is either the B source or the destination, EXB performs as follows:

- If MAR contains an even number, EXB occurs; otherwise, no EXB occurs.

- If MDR is specified as the destination register and MAR contains an even number, only MDR 17:23 is modified. If MAR contains an odd number, only MDR 24:31 is modified.

Unless otherwise stated, extended field options shown in Table 8-9 may not be used when I/O is specified as either a source or a destination.

The POW command causes the system clear sense line to go inactive, thereby causing the signal SCLR0 to become active from the PSC. The entire system is consequently initialized.

The JAMCI option forces a carry-in of one to the least significant bit of the ALU. If the microinstruction is an add, the result on the S bus is one greater than the expected sum. If the microinstruction is a subtract, the result on the S bus in one less than the expected difference. If the microinstruction is neither add nor subtract, JAMCI has no effect.

The DWSHFT option causes SR to participate as the least significant 32 bits of the doubleword being shifted according to the B bus shifter option.

The most significant 32 bits are supplied by the specified second operand register. The doubleword shifted result replaces the contents of the specified destination register (most significant 32 bits) and the shift register (least significant 32 bits).

- When YSI is specified as the B source and LYSI is specified as the E field modifier, the YS field of the instruction register increments by one, regardless of any other microword directive.

- Any fullword memory operation specified in the MC field (i.e., PR4, DR4, PW4, DW4), when specified with YDP1 or YDM1 as E field modifiers, causes an automatic I4 (causing the MAR to increment by X'4').

8.13 YD FUNCTION FIELD (YDFF)

The YD Function Field (YDFF) is an extension of E field operations. The YDFF functions are selected by the value in the YD field of the instruction register and are enabled by code X'9' - YDFF in the E field. Refer to Table 8-10 for YDFF operations.

TABLE 8-10 YD FUNCTION FIELD OPERATIONS

YDI				MNEMONIC	FUNCTION
08	09	10	11		
0	0	0	0	LPSTD	Load Process Segment Table Descriptor
0	0	0	1	LSSTD	Load Shared Segment Table Descriptor
0	0	1	0	RMVF	Reset Memory Voltage Failure Interrupt
0	0	1	1	POW	Power Down, Initialize
0	1	0	0	REPF	Reset Early Power Fail Interrupt
0	1	0	1	RSMPF	Reset Shared Memory Early Power Fail Interrupt
0	1	1	0	SETSNGL	Set the Single-Step User Instruction Interrupt

TABLE 8-10 YD FUNCTION FIELD OPERATIONS (Continued)

YDI				MNEMONIC	FUNCTION
08	09	10	11		
0	1	1	1	RESERVED	
1	0	0	0	RESERVED	
1	0	0	1	RESERVED	
1	0	1	0	RESERVED	
1	0	1	1	RESERVED	
1	1	0	0	RESERVED	
1	1	0	1	RESERVED	
1	1	1	0	RESERVED	
1	1	1	1	RESERVED	

8.14 DATA FORMATS

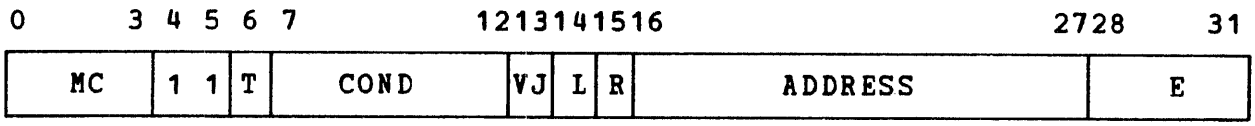
All internal data paths, except those to input/output control, are 32 bits wide. The basic machine operand is consequently a 32-bit fullword. Positive fixed-point data is expressed in true binary form with a sign bit of zero. Negative fixed-point data is expressed in two's complement notation with a sign bit of one. Floating-point data is expressed as a signed magnitude fraction with a biased exponent. The quantity expressed is the product of the fraction and 16 raised to the power of the exponent. Each single-precision floating-point number requires a 32-bit fullword; 8 bits are used for the fraction sign and exponent, and 24 bits are used for the fraction. Each double-precision floating-point number requires a 64-bit doubleword; 8 bits are used for the fraction sign and exponent, and 56 bits are used for the fraction.

Binary information is represented in hexadecimal notation (base 16) for simplicity.

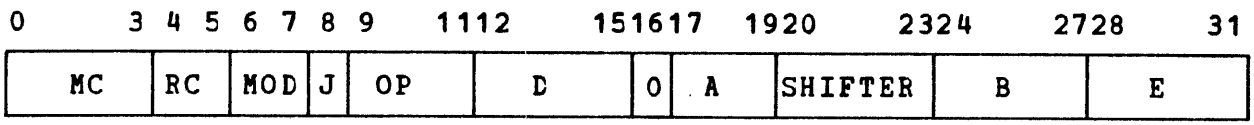
8.15 INSTRUCTION FORMATS

Microinstructions can be in any one of three formats designated Branch, Register-to-Register, and Register-to-Register Immediate. The instruction formats are shown in Figure 8-2.

BRANCH



REGISTER-TO-REGISTER



REGISTER-TO-REGISTER IMMEDIATE

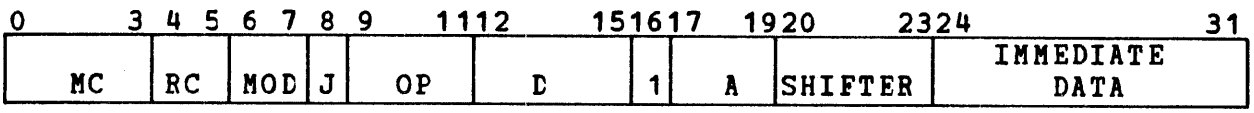


Figure 8-2 Instruction Word Formats

When the branch format is not specified by bits 4 and 5 of the microinstruction word being set, bits 6 and 7 select the processor module that performs the microinstruction. Module 0 is the internal fixed-point ALU. Module numbers 1 and 2 are directed to the optional High Performance Floating-Point Processor. Module number 1 identifies a single-precision operation, and module number 2 identifies a double-precision operation.

8.15.1 Branch

The specified condition(s) are matched against the corresponding machine state. If a match exists, the condition is true; if there are no matches, the condition is false.

The T bit in the branch formats specifies whether the true or false state of the conditions specified by the COND field is to be used. For example, if the condition is true and the T bit is one, or if the condition is false and the T bit is zero, a branch is executed by loading CSAR with the effective branch address.

If the L bit is set in the branch formats, the contents of CSAR are copied to the Link Register (LR), and the LR is incremented by one. If the branch conditions are met, the branch address is copied to CSAR. This is a Branch-and-Link operation.

If the R bit is set, the L bit reset, and branch conditions are met, the contents of LR are gated to CSAR, effecting a return from a prior Branch-and-Link operation.

If the L and R bits are both set and the branch conditions are met, a branch to the address specified by the contents of LR occurs, and LR is loaded with the address of the instruction following the branch instruction. This is a Branch-and-Link-Register operation.

The VJ bit enables direct-vectored hardware interrupts when set in the branch format. If the branch conditions are not met, no branch is taken, and VJ has no effect. If the branch conditions are met and VJ is set, one of eight distinct hardware interrupt vectors can become the branch address if a machine or I/O interrupt is queued. If no interrupt is queued, VJ has no effect, nor has it any effect on the loading of LR when the L bit is set. Refer to Table 8-11 for a description of the possible interrupt vectors. Interrupts have a priority reflected in the order of the vector addresses; the interrupt with the lowest vector address takes precedence over any other queued interrupt. The floating-point fault interrupt vector can be branched to only when a floating-point fault has occurred and the microword specifies an Instruction Read (IR) and a floating-point Read Condition Code (RCC).

TABLE 8-11 HARDWARE INTERRUPT VECTORS

VECTOR ADDRESS	INTERRUPT CAUSE
07	MAC or MPE error during instruction fetch, or illegal instruction detected
08	Alignment fault - halfword or fullword
09	MAT or MPE (noncorrectable memory error)
0A	Console attention, SNGL (single instruction cycle) or PPF
0B	EPF (Early Power Fail) or SEPF (Shared Memory Early Power Fail)
0C	I/O interrupt, ATN0
0D	I/O interrupt, ATN1
0E	I/O interrupt, ATN2
0F	I/O interrupt, ATN3
18	Floating-point processor arithmetic fault

8.15.2 Register-to-Register

These instructions combine a first operand register and a second operand register. The result is copied to one or two destination registers.

The OP field specifies the fixed-point or floating-point operation to be performed. The MOD field, in formats other than branch, acts as an extension to the OP field by causing the fixed-point ALU or optional HPFPP to be selected.

The J field (JAM) causes the PSW condition code field to be updated from the FLR.

The D field selects the S bus destination register; the A field selects the A input to the ALU; and the B field selects the B bus source.

The RC field (ARS) causes the scratchpad registers to be selected when YD or YS is the source or destination for module 0.

The SHIFTER field selects the function to be performed by the B bus shifter.

8.15.3 Register-to-Register Immediate

These instructions are similar to the register-to-register format except that the second operand is taken from the least significant 8 bits of the microinstruction, known as the immediate DATA field. These 8 bits become the least significant 8 bits on the B bus. The remaining 24 bits are forced reset.

CHAPTER 9
CPU-A BOARD

9.1 INTRODUCTION

The main function of the CPU-A board is the control of the micromachine. Fixed Control Store (FCS), branch logic, interrupt support, and initialize control are contained on this board. Functional Schematics 35-816D08 should be referenced with this chapter.

9.2 CONTROL STORE

9.2.1 Control Store Address Register (CSAR)

The CSAR provides the control store with the address of the next microinstruction to be fetched. The CSAR, a 12-bit up counter, is normally in the increment mode, addressing sequential microinstructions. When the microprogram specifies a D2, branch, calculate address (D1), or instruction read, the CSAR is loaded from its strobed 4-to-1 multiplexors (Sheet 2). The signals VSELA0, VSELB0, GDIR1A, and LDCSAR0 control the loading of the CSAR and steering for its multiplexors. Refer to Table 9-1 for the CSAR control line functions. The CSAR can be loaded from one of the four multiplexed inputs (two of which have steering of their own), or the outputs of the multiplexors can be disabled in order to load zeros on an instruction read. Refer to Figure 9-1 for a simplified block diagram of CSAR load sources. Figure 9-2 shows a flowchart which depicts the conditional loading of the CSAR. The CSAR can also be cleared to zero by System Clear (SCLR0D) for initialization.

The CSAR is loaded or incremented by the rising edge of RCLK1. When LDCSAR0 (3E4) is active, the CSAR is loaded on the rising edge of RCLK1; in all other cases it is incremented on this edge. Refer to Figure 9-3 for CSAR timing information.

TABLE 9-1 CSAR CONTROL LINE FUNCTIONS

CONTROL LINE				
LDCSARC	GDIR1A	VSELB0	VSELA0	CSAR OPERATION
0	0	0	0	LOAD FROM LINK REGISTER
0	0	0	1	LOAD FROM RD 16-27
0	0	1	0	LOAD INTERRUPT VECTOR
0	0	1	1	LOAD DECODER ROM VECTOR
0	1	X	X	LOAD ZERO (INSTRUCTION READ)
1	X	X	X	INCREMENT CSAR

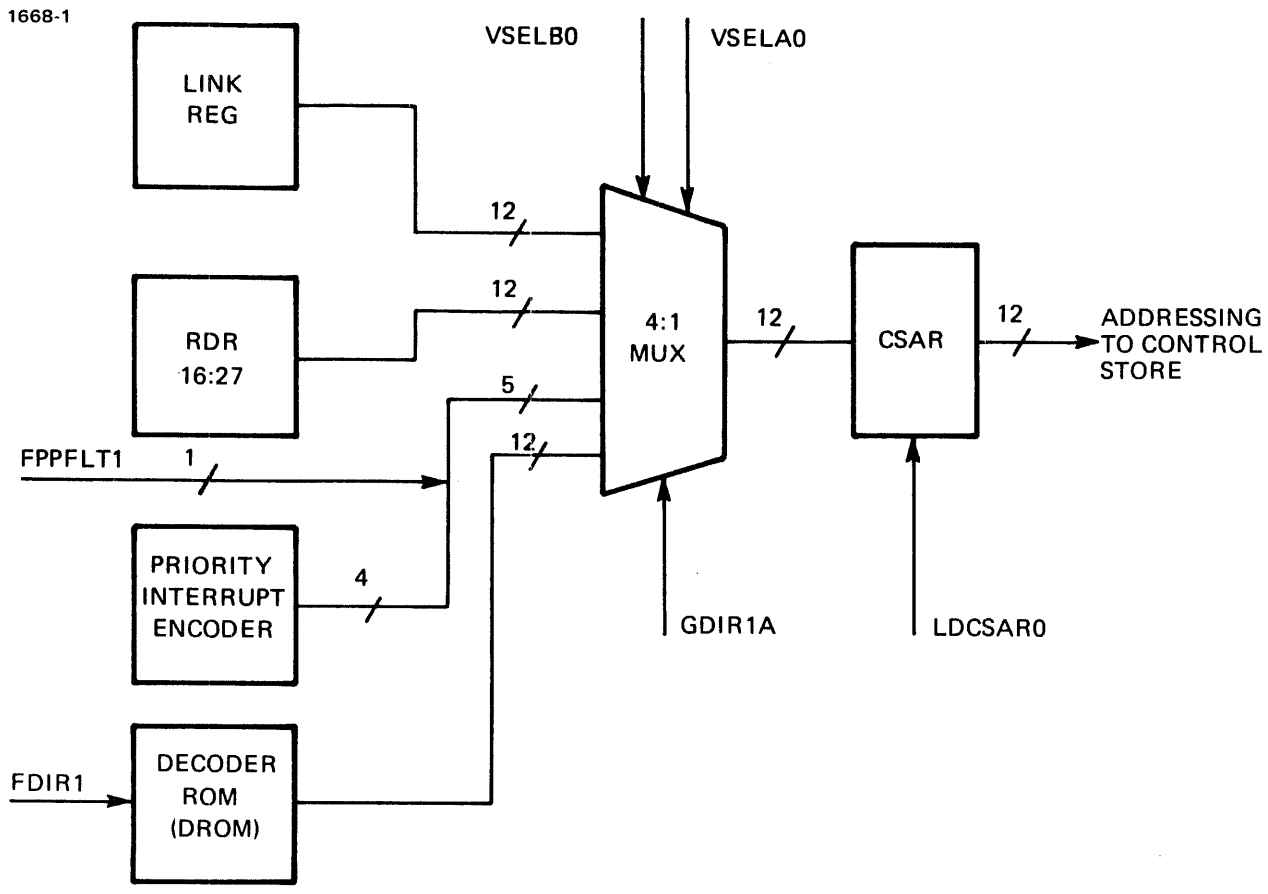


Figure 9-1 Simplified Block Diagram of CSAR Sources

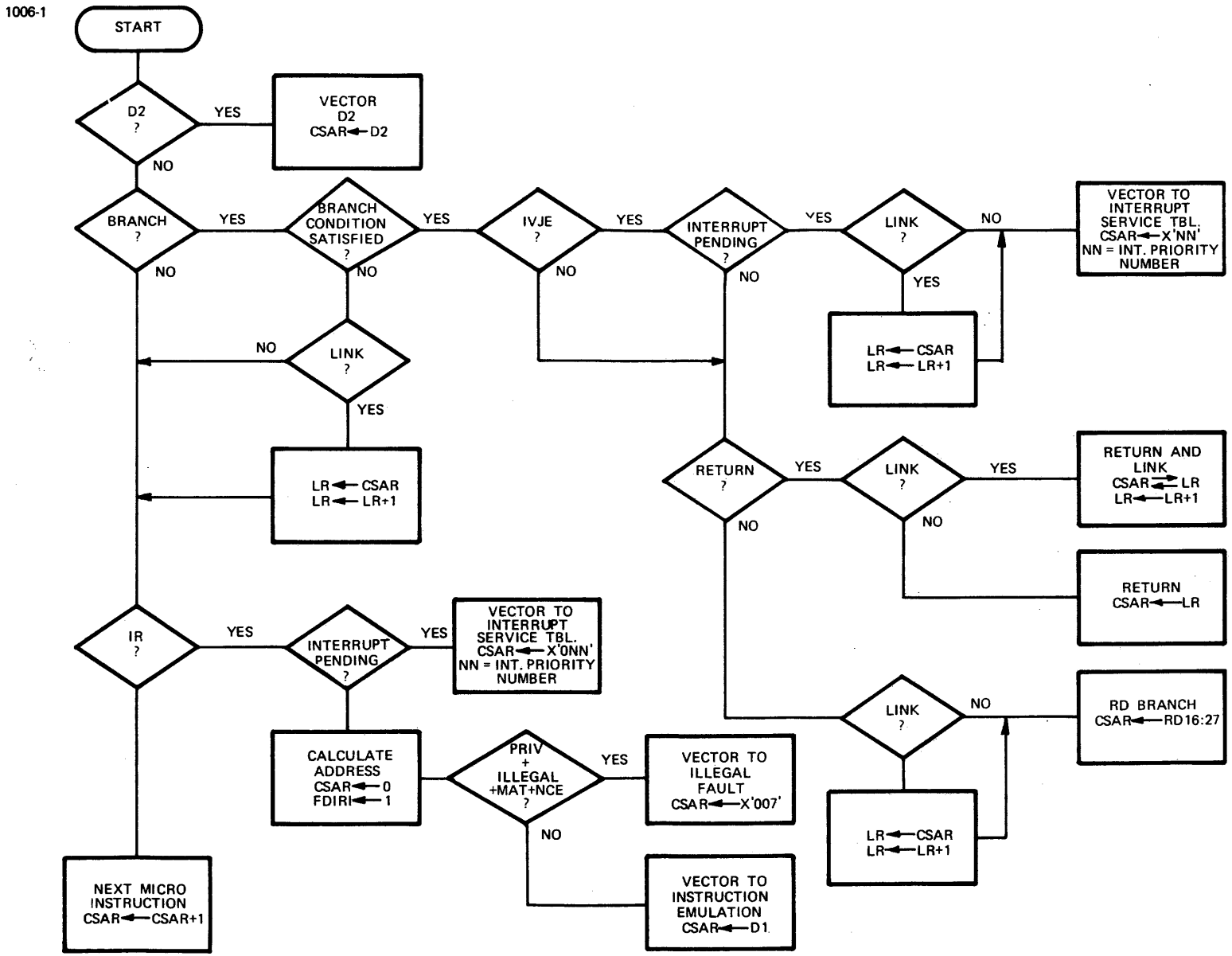


Figure 9-2 Flow Chart of CSAR Loading and Microinstruction Sequencing

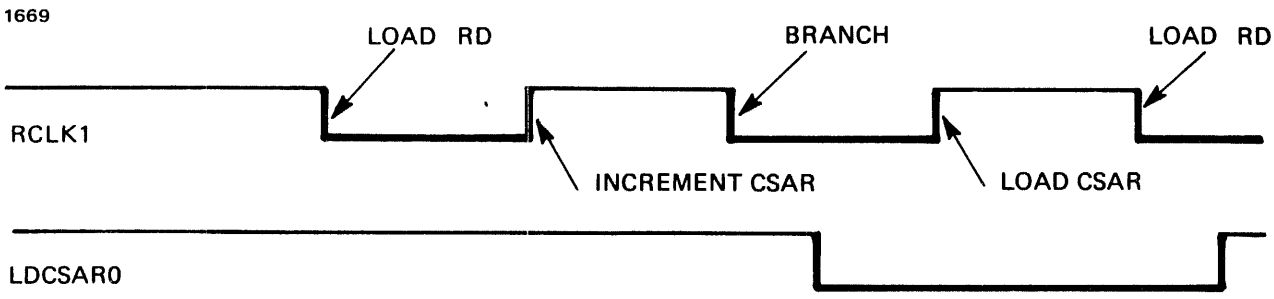


Figure 9-3 CSAR Timing

9.2.2 Link Register (LR)

The 12-bit Link Register (LR) (Sheet 3) provides the microprogram with a branch and link capability. In addition, it provides a means of branching to a calculated microprogram address. In a branch and link microinstruction, the LR is unconditionally loaded with the contents of the CSAR. The LR, a 12-bit up counter, is then allowed to increment by one, pointing to the microlocation immediately following the branch and link microinstruction. Timing for a branch and link microinstruction is illustrated in Figure 9-4. When a link is specified in the microprogram, gate A93-03 (3F5) goes high (a function of RD decoding), enabling gate A92-08 (3H7) to generate Link Register Clock (LRCLK0). LRCLK0 goes active twice during a link instruction. The first active condition performs a load from the CSAR, and the second active state increments the loaded quantity by one. LRCLK0 is generated by the following term:

LRCLK0=A93-03•[(RCLK0A•SCLK0A)+(RCLK1•SCLK1)].

The low active load input to the LR, A93-06 (3H5), goes active during a register-to-register microinstruction specifying load link from the B bus via A93-05 (3H5) or a branch instruction specifying link A93-04 (3H5). Refer to Figure 9-5 for load timing. LDLR1 A88-02 (3H4) active selects the CPU-B bus on the LR's input multiplexors and also generates LRCLK0 via A92-09 at RCLK1 time. The LR can be unloaded to the B bus via the multiplexors on Sheet 7.

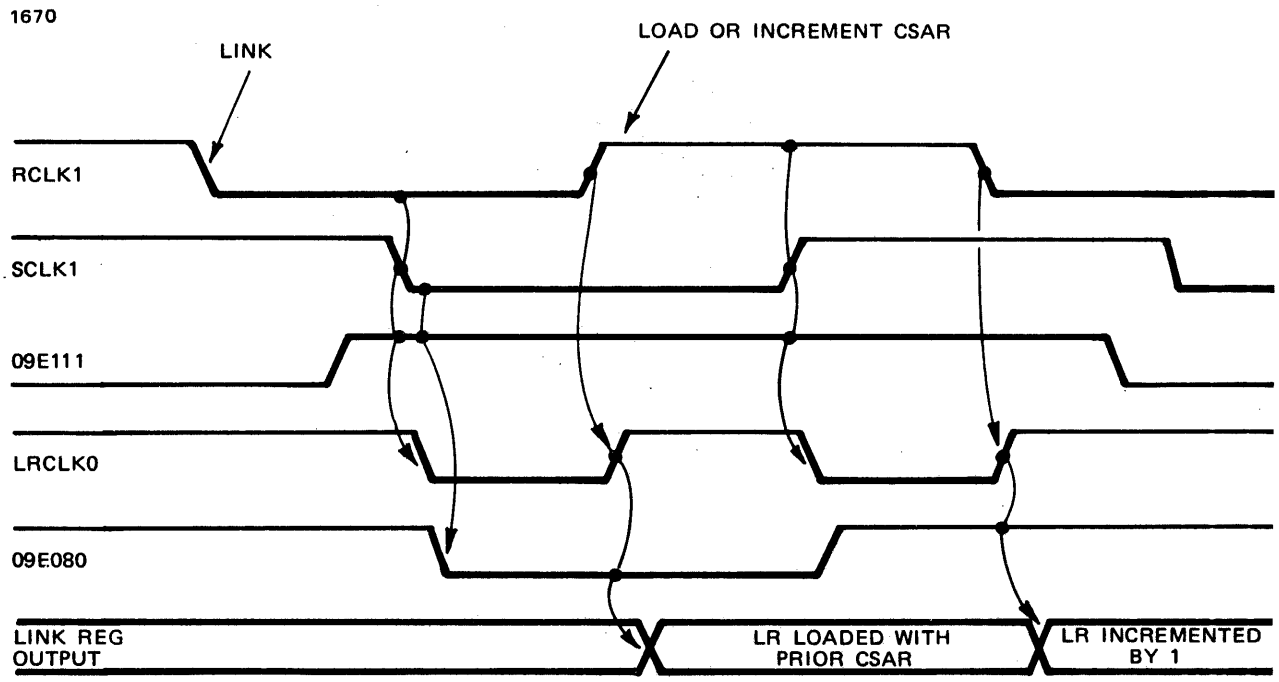


Figure 9-4 Link Register Timing for Branch and Link

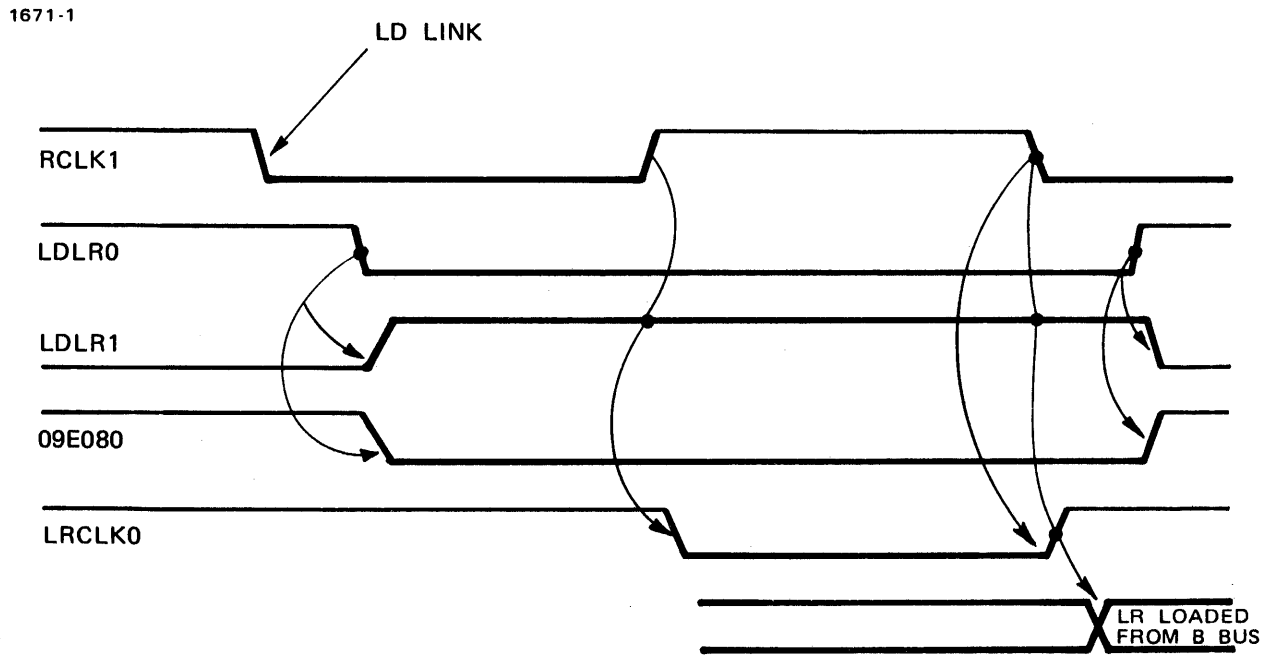


Figure 9-5 Link Register Load Timing

9.2.3 Fixed Control Store (FCS)

The Fixed Control Store (FCS) holds the processor emulator in high-speed ROM. FCS is organized as 2,048 words of 32 bits. Each 32-bit word represents one microinstruction. FCS is comprised of four 2k x 8-bit ROMs which are addressed by the CSAR.

FCS is addressed by the CSAR which is settled no later than 13 ns after the rising edge of RCLK1. The FCS ROM should be settled a maximum of 70 ns after CSAR addresses are settled. FCS is input to the ROM Data Register (RDR), which is clocked by the falling edge of RCLK1 and requires an 8 ns set-up. Figure 9-6 shows FCS timing.

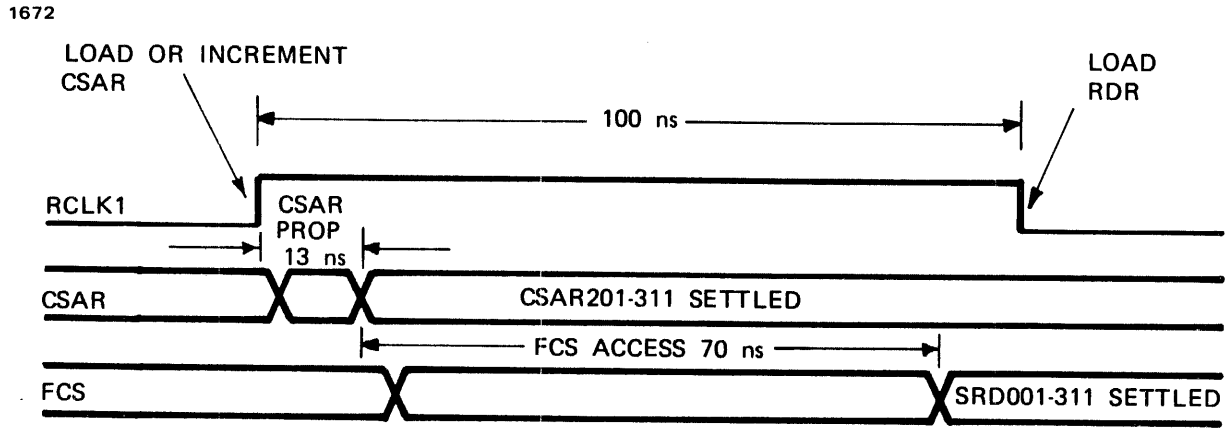


Figure 9-6 FCS Timing

9.2.4 ROM Data Register (RDR)

The ROM data register latches the output of control store on a microinstruction fetch and presents its outputs to the processor as the ROM Data (RD) bus. (Refer to Sheet 5 of the schematics.) The four most significant bits of the RDR (RD001-RD031) are composed of J-K flip-flops and are clocked by the falling edge of RCLK1A. The remaining 28 bits (RD041:RD311) are composed of quad-D flip-flops and are clocked by the rising edge of RCLK0. (Refer to Figure 9-6, FCS Timing.)

On an initialize, the RDR is cleared by the ROM Data Clear signal (RDCLR0). RDCLR0 is the output of a cross-coupled latch (2K7) which is set by SCLR0D (Systems Clear) and remains set, holding the RDR cleared, until the CSAR increments to X'004'. RDCLR0 is reset when CSAR290 goes active.

9.2.5 Decoder ROM (DROM) and Privileged/Illegal ROM (PILROM)

The DROM and PILROM provide the hardware with the calculate address (D1, D2), privileged and illegal instruction vector addressing for the Processor Emulator (05-090). Listings for the DROM and PILROM (and the format ROM on the CPU-D board) appear in the microprogram listing (05-090A13). Refer to Table 9-2 for an explanation of this data.

The DROM is organized as 512 words of 12 bits each and consists of three 512k x 4-bit high-speed ROMs (Sheet 7). The DROM is addressed by the 8-bit op-code field of the instruction register (IR000-IR070), located on the CPU-D board, and provides the D1 or D2 vector address to the CSAR multiplexor. FDIR1 (3E8) (decoded instruction read flip-flop) goes active on the first clock of an instruction fetch and is used as the most significant address of the DROM. When FDIR1 is active, D1 is selected; when inactive, the DROM outputs the D2 vector address.

TABLE 9-2 LISTING INFORMATION FOR DROM, PILL ROMs AND FORMAT ROM

Refer to the listing of the Processor Emulator (05-090A13).

ADDRESS	DATA	DESCRIPTION
08NN	0000 XYYY	PILL, D1 VECTOR
09NN	0000 ZWWW	Format, D2 VECTOR

where: NN = IR001 - IR071, the 8-bit op-code field of the instruction register.

X = PRIV1, COMILL1, and FLTILL1, respectively, the output of the PILL ROM (see Note) in hexadecimal.

YYY = DD201 - DD311, the output of the decoder ROM's D1 vector in hexadecimal.

WWW = DD201 - DD311, the output of the decoder ROM's D2 vector in hexadecimal.

Z = RX1, RI20, RXRX1, and RR1, respectively, the output of the CPU-D format ROM in hexadecimal.

NOTE

The listing (05-090A13) represents the 19-188F27 PILROM, for a WCS equipped CPU-A board in a Model 3230 only. A Model XXXX CPU-A board, however, is

equipped with the 19-188F25 PILL ROM which has the following differences underlined:

08E5	0000	43B5	ILEG
08E8	000C	43B7	ILEG
08E9	0000	43B3	ILEG

The PILROM is addressed by the op-code field of the instruction register and its outputs are tested at D1 time (FDIR1 active) to determine whether the instruction is a privileged or illegal operation. Refer to Sheets 3 and 7 of the schematics. Having passed all prior interrupt tests, the CSAR, at D1 time, is conditioned to load the D1 vector address, (i.e., LDCSAR0-active; VSELA0, VSELB0, and LDIR1A-inactive) unless one of the conditions listed in Table 9-3 causes an illegal fault. In the latter case, VSELA0 goes active and the CSAR is loaded from the priority interrupt encoder input. The priority interrupt encoder is jammed to X'007' by FDIR1 (Sheet 13), the illegal fault microprogram location.

TABLE 9-3 ILLEGAL FAULT CONDITIONS

Base Algorithm for VSELA0 at D1 time

$\overline{VSELA0}$ = FDIR1•[COMILL1+FDIR1•PRIV1•PSW231+FLTILL•($\overline{FPP1}$+FPP1•PSW131)+MATMPE0]

EXPLANATION OF FAULT CONDITIONS

FAULT CONDITION	REASON
FDIR1•COMILL1	Illegal Instruction
FDIR1•PRIV1•PSW231	Privileged Instruction
FDIR1•FLTILL1•$\overline{FPP1}$	Illegal Floating-Point Instruction (HPFPP not equipped)
FDIR1•FLTILL1•FPP1•PSW131	Privileged Floating-Point Instruction
FDIR1•MATMPE0	Machine Malfunction

9.3 BRANCH LOGIC

The branch logic provides 16 testable conditions for microprogram decisions. These conditions are input to four 4-to-1 multiplexors with RD071 and RD081 controlling their select lines, breaking the conditions down into four groups of four conditions each (see Sheet 6). Furthermore, the outputs of the multiplexors are NORed, which allows more than one condition to be tested at a time by enabling or disabling individual multiplexors. Refer to Table 9-4, which shows the grouping of conditions and the controlling RD bits. A branch microinstruction begins with RD041 and RD051 active, causing BRANCH0 and its complement BRANCH1 to become active (see Sheet 3). The four multiplexor outputs are NORed with BRANCH0 to cause True Branch (TBRCH0) active when the selected condition(s) are true. RD061 determines whether a true branch (RD061 inactive) or a false branch (RD061 active) condition is specified. Load CSAR (LDCSAR0) is used to load the CSAR with the branch address. LDCSAR0 goes active on a branch by the following algorithms:

LDCSAR0=TRBRCH1+FBRCH1
True branch TRBRCH1=TBRCH0•$\overline{\text{RD060}}$•BRANCH1
False branch FBRCH1=$\overline{\text{TBRCH0}}$•RD061

Vector selects A and B (VSELA0 and VSELB0), used to steer the CSAR input multiplexor, are affected by the following algorithms during a branch:

VSELB0=BRANCH1•GBRCH1•$\overline{\text{RD131•INT1}}$
GBRCH1=TRBRCH1+FBRCH1
$\overline{\text{VSELA0}}$=$\overline{\text{RD131•INT1}}$•RD150•(RD060•TBRCH1•BRANCH1+TBRCH0•RD061)

A conditional return is specified during a branch when RD150 is active, which causes VSELA0 to be low. An Interrupt Vector Jam Enable (IVJE) may also be specified with a branch and is represented above as $\overline{\text{RD131•INT1}}$, IVJE inactive. IVJE is explained in Section 9.4.

TABLE 9-4 BRANCH CONDITION GROUPS

	RD 061	RD 071 RD 081	RD 091 RD 101 RD 111 RD 121	CONDITION	DESCRIPTION
	0			BT	Branch True
	1			BF	Branch False
Group 1		0 0	1	C	Carry Flag
			1	V	Overflow Flag
			1	G	Greater Than Flag
			1	L	Less Than Flag
Group 2		0 1	1	PPF	Primary Power Fail Interrupt
			1	MAT	Memory Address Translator Interrupt
			1	MPE	Noncorrectable Memory Error Interrupt
			1	CATN	Console Attention Interrupt
Group 3		1 0	1	INT	Priority Encoder Interrupt Pending
			1	MASK	User Branch
			1	MVF	Memory Voltage Failure
			1	HW	I/O Halfword Signal
Group 4		1 1	1	COMM	Communications Option Strap
			1	EPF	Early Power Fail Interrupt
			1	FPP	Floating-Point Processor Strap
			1	YDC	Carry-out from YD Register

9.4 INTERRUPT SUPPORT

9.4.1 Priority Interrupt Encoder (PIE)

The Priority Interrupt Encoder (PIE) provides the microprograms with the means of handling interrupts in the order of their priority. Inputs provide 11 possible conditions. The PIE generates the vector address for the highest priority interrupt pending (if enabled) and jams the interrupt line (INT1) active (8H8). Refer to Table 9-5 for a listing of interrupt priorities and their resulting vector addresses. At calculate address time (D1 time), FDIR1 goes active and disables the priority encoder, jamming its output to X'007' which is used for the illegal fault vector.

External interrupts (ATN00-ATN30) are masked by certain PSW bits. Refer to Table 9-6 for external interrupt masking. A 256 x 4-bit ROM decodes the PSW mask bits and outputs external interrupt enable lines (8D6). A listing for the external interrupt mask ROM appears in Table 9-7.

TABLE 9-5 INTERRUPT PRIORITIES

INTERRUPTS (IN ORDER OF PRICRITY)	ACTIVE SIGNAL	MASK	ENTRY TO INTERRUPT SERVICE TABLE	ENTRY TO ILLEGAL FAULT SERVICE
Alignment Fault	ALGNO	None	008	Disabled
Noncorrectable Memory Error	FNCEO	PSW21	009	007
Memory Address Translator Fault	MATO			
Primary Power Fail	FPPF1	None	00A	Disabled
Console Attention	CATNO			
Single Step	SNGLO			
Early Power Fail	FEPF1	PSW18	00B	
External Interrupt Level 0	ATN00	See Table 9-7	00C	
External Interrupt Level 1	ATN10		00D	
External Interrupt Level 2	ATN20		00E	
External Interrupt Level 3	ATN30		00F	
Illegal Instruction	COMILL1	None	Disabled	007
Privileged Instruction	PRIV1	PSW23		
Floating-Point Instruction	FLTILL1	PSW13		
Floating-Point Processor Arithmetic Fault	FPPFLTO	See Note	018	Disabled

NOTE

FPPFLTO is enabled by an Instruction Read (IR) and Read Condition Code (RCC) from the HPFPP.

TABLE 9-6 EXTERNAL INTERRUPT MASKING

PSW BITS		
17	20	
0	0	All Levels Disabled
0	1	Higher Levels Enabled
1	0	All Levels Enabled
1	1	Current and Higher Levels Enabled

where the current level is a function of the currently active register set.

PSW BITS					EXTERNAL INTERRUPT ENABLED			
17	20	25	26	27	LEVEL 0	LEVEL 1	LEVEL 2	LEVEL 3
0	0	X	X	X	NO	NO	NO	NO
0	1	0	0	0	NO	NO	NO	NO
0	1	0	0	1	YES	NO	NO	NO
0	1	0	1	0	YES	YES	NO	NO
0	1	0	1	1	YES	YES	YES	NO
0	1	1	0	0	YES	YES	YES	YES
0	1	1	0	1	YES	YES	YES	YES
0	1	1	1	0	YES	YES	YES	YES
0	1	1	1	1	YES	YES	YES	YES
1	0	X	X	X	YES	YES	YES	YES
1	1	0	0	0	YES	NO	NO	NO
1	1	0	0	1	YES	YES	NO	NO
1	1	0	1	0	YES	YES	YES	NO
1	1	0	1	1	YES	YES	YES	YES
1	1	1	0	0	YES	YES	YES	YES
1	1	1	0	1	YES	YES	YES	YES
1	1	1	1	0	YES	YES	YES	YES
1	1	1	1	1	YES	YES	YES	YES

X = Don't Care

TABLE 9-7 LISTING FOR ROM IC 19-142F44 EXTERNAL INTERRUPT MASK ROM

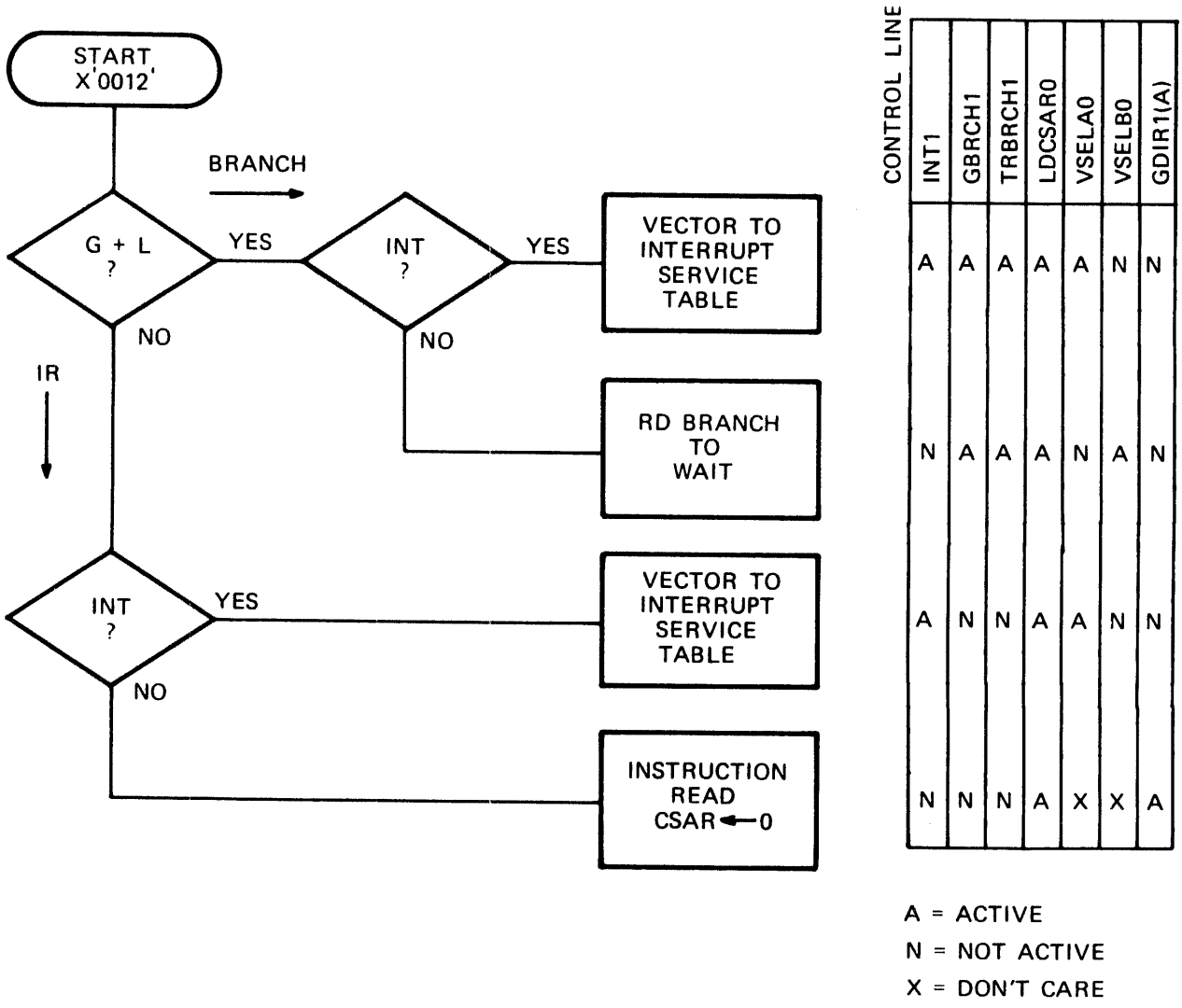
ADDRESS	DATA	ADDRESS	DATA	ADDRESS	DATA
00	0	10	F	20	Not used, should be zero
01	0	11	F	•	
02	0	12	F	•	
03	0	13	F	FF	
04	0	14	F		
05	0	15	F		
06	0	16	F		
07	0	17	F		
08	0	18	8		
09	8	19	C		
0A	C	1A	E		
0B	E	1B	F		
0C	F	1C	F		
0D	F	1D	F		
0E	F	1E	F		
0F	F	1F	F		

All data in hexadecimal

9.4.2 Interrupt Vector Jam Enable (IVJE)

The IVJE logic provides the microprogram with a conditional vectored branch capability for interrupt handling. The microprogram can enable the IVJE logic with a branch IVJE microinstruction. A branch microinstruction enables IVJE by setting RD151. In this case, a 2-way branch is possible. If the branch condition is satisfied (GBRCH1 active), and INT1 (interrupt) is active, the CSAR loads from the priority interrupt encoder and a branch is taken to the Interrupt Service Table, X'008-00F', (refer to Figure 9-2). If the branch condition is satisfied and INT1 is not active, the CSAR loads the RD branch address (Sheet 2). If the branch condition is not satisfied, the CSAR does not load (LDCSAR0-inactive, 3E5), INT1 is ignored, and the CSAR increments to the next sequential microprogram address. An instruction read microinstruction enables IVJE automatically. INT1 active jams GDIR1 and GDIR1A inactive, aborting the Instruction Read; the CSAR loads from the priority interrupt encoder causing a branch to the Interrupt Service Table. If INT1 is inactive, GDIR1 and GDIR1A go active, beginning an Instruction Read.

Branch IVJE and IR may be specified in the same microinstruction. Refer to Figure 9-7 for an example of this condition.



NOTE: THIS EXAMPLE IS EXTRACTED FROM THE PROCESS EMULATOR - 05-090.

Figure 9-7 Example of a Branch with IVJE and IR

9.5 INITIALIZE CONTROL CIRCUITRY (ICC) THEORY OF OPERATION

9.5.1 General

The ICC is located on the CPU-A board and is responsible for the following three interface and control functions:

1. Receipt of power supply generated power fail detect signal (PFDT0) and coordination of system clear signal (SCLR0) during power-up and power-down of the system.

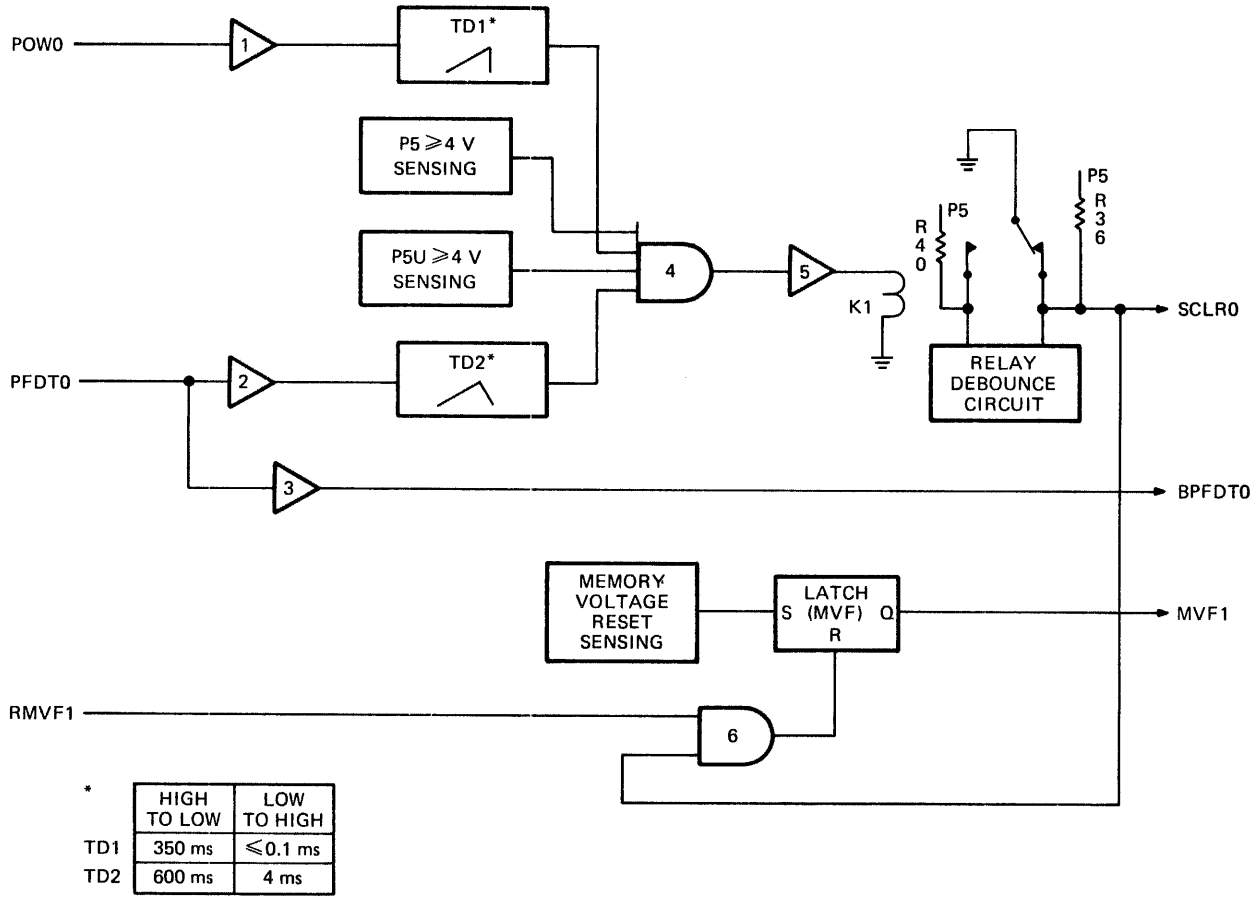
2. Receipt of microcode generated shutdown signal (POWO) and coordination of SCLRO during an initialize sequence.

3. Generation of a latched memory voltage fault signal (MVF1) in response to reestablishment of the memory voltage (P5U) supply.

The logic circuits found in the ICC are implemented using quad-comparator (19-190) and transistor logic, which allows the ICC to operate with supply voltages (P5 and P5U) as low as 2.5 VDC. The logic block diagram for the ICC is presented in Figure 9-8. This diagram is a close functional approximation of the ICC schematic appearing in Sheet 9 of Functional Schematic 35-798D08 (CPU schematic). The following description of operation is referenced to the logic block diagram.

9.5.2 Description of DC Power-On Control Sequence

Initially, with all system DC voltages down, relay K1 is depowered and a set of normally open contacts clamps SCLRO to ground potential. Before the power supply starts to build up the P5U voltage, a logic low is applied to PFDTO and this active signal is maintained until the P5 voltage is fully established. This occurs approximately 800 milliseconds after the consolette mounted key switch is set in the ON (or LOCK) position. At this time, the power supply drives the PFDTO input inactive, which provides an enabling input to gate 4 after propagating through a 600 millisecond time delay (T.D.2). During the power-on sequence, the POWO input from the microcode comes up in the inactive state and this signal provides the second enabling input to gate 4 after propagating through a 350 millisecond time delay (T.D.1). The other two enabling inputs to Gate 4 are present when both the P5 and P5U system voltages are above 4.0 VDC. When the input enabling conditions to Gate 4 are met, K1 relay coil is energized through power driver Gate 5 and SCLRO is driven inactive by the attached pull-up resistor. A relay debounce circuit, consisting of cross-tied power gates across the normally open and normally closed contacts of K1, ensures that the SCLRO signal remains clean (no multiple edges) during making and breaking of the K1 relay contacts.



*

	HIGH TO LOW	LOW TO HIGH
TD1	350 ms	≤0.1 ms
TD2	600 ms	4 ms

Figure 9-8 Initialize Control Circuit Logic/Block Diagram

9.5.3 Description of Initialize Control Sequence

If the CPU detects a request for initialize while it is running; i.e., SCLR0 is inactive, the microcode issues an active POW0 signal after completing its initialize routines. This removes one of the enabling input signals to Gate 4 which causes K1 to de-energize and drive SCLR0 into the active state. The POW0 signal from the microcode is driven inactive once SCLR0 is changed to the active state. With POW0 inactive, Gate 1 provides the missing enabling input to Gate 4 after a propagation delay of 350 milliseconds through T.D.1. In turn, Gates 4 and 5 outputs result in the K1 relay coil being energized and SCLR0 is returned to the inactive state.

9.5.4 Description of DC Power-Down Control Sequence

Initially, with the CPU operating normally and SCLR0 inactive, the power supply will notify the ICC of an imminent DC power-down condition by driving PFDT0 active. This signal is then applied to the CPU through buffer Gate 3 (BPFDT0) and initiates a CPU shutdown sequence; i.e., shutdown of software and subsequent

microcode shutdown. Upon completion of microcode shutdown, the microcode (approximately 1 millisecond after receiving BPFDT0) drives POW0 active. This removes one of the enabling input signals to Gate 4, which causes K1 to de-energize and drive SCLR0 into the active state. Concurrent to the CPU shutdown path initiated by BPFDT0, the ICC starts a backup time-out through T.D.2. If after 4 milliseconds POW0 is not driven active, Gate 4 receives a disabling input from T.D.2, which also results in SCLR0 being driven active.

9.5.5 Memory Voltage Fault Latching

During a CPU restart sequence, the CPU requires notification of a memory voltage fault; i.e., the memory voltage decayed to 0 prior to the restart, indicating a dropout of the battery backup for P5U. During the DC power-on control sequence, if the P5U is reestablished, the ICC Memory Voltage Reset Sensing circuit sets the Memory Voltage Fault (MVF) latch. After SCLR0 is driven inactive, the MVF1 signal is interrogated by the microcode. If MVF1 is active, the microcode initiates a cold start and after completion of the cold start, issues a MVF latch reset signal by driving the RMVF1 line active for 1.4 milliseconds. If the MVF1 signal is inactive during a CPU restart, no RMVF1 signal is generated by the microcode.

9.5.6 Block Diagram Correspondence to Schematic Components

This section provides a correlation between the active (I.C. or semiconductor) schematic components and the functions (gates, time delays, and sensing circuits) depicting on the Logic/Block diagram.

- Gate 1: A118-02
- T.D.1: A118-01
- P5 $\geq$ 4V SENSING: D9
- P5U $\leq$ 4V SENSING: D6
- Gate 4: A118-14, A119-14
- Gate 2: A119-13
- Gate 3: A119-02
- T.D.2: A119-14
- Gate 5: Q3, Q2
- RELAY DEBOUNCE CIRCUIT: A117
- MEMORY VOLTAGE RESET SENSING and MVF LATCH: A119-01
- Gate 6: Q1, D2

9.6 TEST AID

A Test Aid is provided on the CPU-A board which gives the customer engineer or technician the means for halting the microprogram or a SYNC pulse for troubleshooting. (Refer to Sheet 10 of the schematics.)

The Test Aid provides four switch selectable methods of halting the processor. The 16 DIP switches in the connector 5 location of the CPU-A board enable the four match conditions, as well as providing an input for the microaddress match/SYNC. A chart is provided at schematic location 15H1 which shows the switch functions. The external trap (EXTRAP0) condition is enabled by placing switch 1 in the ON position. Its input must be settled 20 ns before the falling edge of CLK1.

The second DIP switch causes the processor to halt whenever a MAT or MPE is active. This is to provide a convenient memory fault or memory access fault trap. The single switch (switch 3) places the microprocessor in the single-step mode. In this mode, one microinstruction is executed each time the ADVANCE switch located on the CPU-D board is depressed.

The fourth switch enables the CSAR address match condition. Switches 5-8 and 1-8 on the right-hand DIP provide the address match information.

Any of the previously mentioned conditions, when enabled, cause TRAP0 to go active, signaling the CPU-D to halt clocks.

The SYNC (SYN0) output goes active when the match switches and the CSAR outputs are the same and RCLK0 is inactive, providing a low active pulse at the beginning of the selected microinstruction. This pulse may be used as SYNC input to an oscilloscope or logic analyzer.

9.7 MNEMONICS

The following is a list of mnemonics found on the CPU-A board. The meaning and the 35-816D08 schematic source of each signal are provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
AENH0	"A" enable high - used by CPU-B to control the most significant 16 bits of the A bus	8E4
AENL0	"A" enable low - used by CPU-B to control the least significant 16 bits of the A bus	8E5

MNEMONIC	MEANING	SCHEMATIC LOCATION
ALGNO	Alignment error signal from CPU-D that indicates an alignment fault has been detected	8A9
APSW281:311	Auxiliary PSW bits 28:31 - used by the branch logic to determine user mask match	6G8
ATNOOO:030	I/O attention lines - these are the four levels of I/O interrupts from the multiplexor bus.	8A7
B161:311	B bus bits 16:31 - B bus source data from the CPU-A	Sheet 7
BRANCHO	Branch decoded from RD bits	3E4
BSTKSO	RD decoded output for the B stack latch on the CPU-B	8N4
CATN1	Console attention interrupt from the System Control Panel	6F4
CCATNO	RD decoded clear console attention	7J3
CLO7O	Control line 7 - early indication of pending power failure provided for I/O devices	9F4
CLK1A	System clock net for CPU-A from the CPU-D board	7A2
CLKCCO	Clock condition code - used by the CPU-A to load the auxiliary condition code	6D9
CLKPSWO	Clock PSW - clock decoded by RD to load the PSW	8E3
COMILL1	Communication illegal - defines communication instructions option as being illegal	7F9, 10K9
COMM1	Strap option to allow the communication instruction package	6J2
CSAR200:310	Control store address register bits 20:31 - used to select words in control store	Sheet 2

MNEMONIC	MEANING	SCHEMATIC LOCATION
DCLK0	Destination clock - clock used to load registers	7E4
DD201:311	Decoder read-only-memory data - data used to vector to instruction emulation routine	Sheet 7
DEXB0	RD decoded exchange byte for the CPU-C board	8N1
DEXT0	RD decoded sign extension - signal to CPU-C to perform sign extension on the MDR source	8E1
DFTEN0	RD decoded double-precision floating-point enable - optional High Performance Floating-Point Processor is conditioned for a double-precision operation.	8N9
DIR0	RD decoded instruction read - used to initiate instruction fetch and calculate address	3B5
DISA0	Disable A source data - generated on the CPU-D board during calculate address to inhibit data from the general register selected by the YS or X2 fields	8B5
DISB0	Disable B source data - generated on the CPU-D board during calculate address to inhibit data from the B source MDR	8J3
DIV0	RD decoded fixed-point divide operation	7J3
DSTOP0	Destination stop - inhibits the generation of destination clocks	7B4
DWSHFT0	RD decoded doubleword shift - provides 64-bit shift capability	7L8
ENB0	Enable CPU-A board B bus sources	7L8
ENBS0	Enable B source data on the CPU-B board - gates bits 0:15 of the shift register or zeros onto the B bus	7L8

MNEMONIC	MEANING	SCHEMATIC LOCATION
ENCSAR1	Enable control store address register - allows the CSAR to count up by one on each RCLK	2B5
EXTRAP0	External trap - test feature provided to allow an external function to cause the microprocessor to halt when the external event occurs	10C9
FCATN1	Flip-flop set side output of console attention	6H5
FDIR0	Flip-flop reset side output of gated decoded instruction read - set first clock after DIR if branch is not valid	3E8
FEPF1	Flip-flop set output of early power fail detections	9H1
FLR281:311	Output of the flag register used to be directly tested by the microcode or to be loaded into the auxiliary PSW	Sheet 6
FLTILL1	Floating-point instructions are illegal - Privileged/Illegal read-only-memory output that can force vector to illegal instruction	7G9
FNCE0	Flip-flop reset output from CPU-D board which indicates that a double-bit error has occurred in local memory	6B2
FPPFLT0	Floating-point processor fault - indicates an arithmetic fault interrupt from the high performance floating-point processor	8A9
FPPF0	Output of the primary power failure flip-flop - the signal causes a testable branch condition to become valid, causing the microprogram to shut down.	9H1

MNEMONIC	MEANING	SCHEMATIC LOCATION
FPP1	Strap option on the CPU-A that, depending on how it is strapped, indicates the presence, or lack of presence, of the high-speed floating-point processor	6H5
FSCATN0	Output of latch used to synchronize the console attention interrupt to the system clocks	6G3
FSMPE0	Output of latch used to delay the receipt of the double-bit error indication from the CPU-D	6G2
FSPPF0	Output of latch used to delay the branch testability of the primary power failure flip-flop	6G2
GBRCH1	Gated branch - this signal indicates that a branch occurs, regardless of whether it is a true or false branch.	6R3
GDIR0	Gated decoded instruction read - signal provided for the CPU-D board to indicate the start of an instruction fetch. Consists of RD decoded IR and branch not valid.	3E7
GFLR291	Gated flag register bit 29 - flag register bit 29 (overflow) is ORed with the false SYNC timeout of the I/O system.	8N1
GMVF0	GMVF0 indicates, if NCE0 is also active, that nonpresent memory has been accessed.	6B6
GRD091:111	Gated RD bits that control the type of operation to be performed by the fixed-point ALU. When floating-point operations are specified in the microinstruction, the ALU is forced into a load B operation. When the calculate address logic disables the B source, the ALU is forced into a load A operation.	8N2
GSNGL0	Gated single - the single cycle flip-flop output is gated by decoded instruction read.	6F5

MNEMONIC	MEANING	SCHEMATIC LOCATION
HWO	Halfword I/O signal - when this signal is low, the currently selected I/O device provides for halfword data paths.	6B6
INT1	Interrupt pending - this signal is used by the CSAR control logic to force pending interrupt service.	8H8
IR000-IR070	Instruction register bits 0:7 - this is the user-level operation code portion of the Instruction Register. The DROM uses the op-code for vector address data.	7A8
JAMCIO	Jam carry-in to the ALU on CPU-B board	7K3
LDCSARO	Load the control store address register - the outputs of the CSAR multiplexors are loaded into the CSAR on the leading edge of RCLK.	3E5
LDIOO	RD decoded load I/O - used to disable E field decoding during I/O operations	8E2
LDLRO	RD decoding of load link register - data in the B bus is loaded into the CSAR on the trailing edge of DCLK.	7J4
LFLRO	RD decoding of load flag register - signal generated by the CPU-B enables the flag register to load from the S bus.	8E3
LR201-LR311	Link register bits 20:31	Sheet 3
LRCLKO	Link register clock - used to load and increment the link register	3J7
LSRO	RD decoded load shift register - the shift register on the CPU-B is the destination and is loaded with the data on the S bus.	8D2

MNEMONIC	MEANING	SCHEMATIC LOCATION
MAT0	Signal supplied by the CPU-C board that indicates a MAT interrupt	6G3
MATMPE0	Logical OR of MAT interrupt and noncorrectable error interrupt - used to force interrupt vector	8E9
MAT201-MAT311	Test aid match data switches used to select CSAR address match	Sheet 10
MEXTC	Match external switch - allows the stopping of the micro-program because of an external event	10C8
MPY0	RD decoding cf the E field specifying a multiply operation	7J3
MSK1	Branch mask valid - the ANDing of the PSW condition code and the YD field of IR has been satisfied. User instruction branch takes place.	6L7
MSNGL0	Test aid switch that allows the microprogram to be advanced one step at a time. Actual stepping is done on the CPU-D board.	10C8
MVF1	Memory voltage failure - this signal indicates that the Memory Voltage (P5U) went out of regulation (memory data is unreliable).	11B6, 9S9
PFDT0	Power failure detected - caused by the power supply, INITIALIZE switch, or KEY switch. This signal causes the eventual shut-down of the processor.	9C8
POWC	RD decoding of the E and YDFF, indicating a command to power-down the processor	8N8
PRIV1	Privileged instruction op-code is contained in the instruction register. This is an output of the PILROM.	7F9
PSW131:271	Program status word bits 13:27	Sheets 3,8

MNEMONIC	MEANING	SCHEMATIC LOCATION
RCATNO	Reset console attention - part of the HALT/RUN switch on the System Control Panel. Controls console attention interrupt.	6B5
RCLKO	System clock that is allowed only when RSTOP is inactive - used to advance CSAR, load RD register, etc.	7D3
RD001:311	RD register data output bits 0:31 - this data represents the micro-instruction word.	Sheet 5
RDCLRO	RD register clear	2L9
REPFO	Reset early power fail interrupt	8M6
RSMINTO	Reset shared memory early power fail interrupt	8M7
RSTOPO	ROM stop - used to inhibit system clocks when necessary to prevent the incrementing or loading of the CSAR and RDR	7B2
SCATNO	Set console attention - part of the HALT/RUN switch on the System Control Panel. This controls the console attention interrupts.	6B5
SCLK1	Skewed system clock - this clock is delayed by 50 ns from the regular clock.	7B5
SCLRO	Systems clear - resets the processor and all devices	9M7
SETSNGLO	Set single step - active low causes the single-step user instruction flop to be set.	8M7
SFTENO	Single-precision floating-point operation enabled	8J3
SHO	Shift - generated by the CPU-B board - disables the A bus multiplexor during multiply operations when a shift only is required	8B5
SMINTO	Shared memory early power fail interrupt	8M5

MNEMONIC	MEANING	SCHEMATIC LOCATION
SNGL0 SNGL1A	Signals from the single switch on the System Control Panel - these signals cause the micro-program to cycle each user instruction and halt until HALT/RUN is depressed.	6B4 3B9
SR00:10	Shift register control signals - these signals are generated for the CPU-B to control shift register operations (load, shift right, shift left).	8E3
SRD001:311	Source RD bits 00:31 - these are control store output signals that set or reset RD bits.	Sheet 4
SVC	Set overflow - generated by the I/O control logic on the CPU-D when a false SYNC timeout occurs.	8G2
SWA0	Set wait - decoded from the E field portion of the micro-instruction	7J2
SYN0	SYNC - test point which is activated each time a system clock occurs during the selected CSAR address match	10K5
TBRCH0	True branch - indicates the specified branch condition has been met	6R2
TRAP0	Trap - test aid signal indicating that the selected match function has been found. The CPU-D causes an RSTOP to occur when Trap is active.	10K6
ULLR0	Unload link register - RD decoding of the link register as a source	7K6
ULSR0	Unload shift register - RD decoding of the shift register as a source; supplied to the CPU-B	7J6
UNNLD0	Unnormalized load - E field decoding of unnormalized load. The normalizing logic of the HPFPP is disabled.	7J3

MNEMONIC	MEANING	SCHEMATIC LOCATION
UPSW0	Unload program status word	8D4
VECT01:31	Vector jam data lines - these lines are loaded into the least significant four address lines of the CSAR for interrupt service.	Sheets 2,3
VSELA0 VSELB0	Data select lines on the 4:1 multiplexors that determine the source of data to be loaded into the CSAR	3L2 2B1
WAIT0	This signal is generated by the CYD&SWA E field option. When active, the WAIT indicator on the System Control Panel is illuminated.	9M1
YD081:111	YD field of the instruction register - the YD field selects one of 16 general registers, normally used for a user instruction destination.	Sheet 6
YDC1	YD field carry - this signal indicates that the YD field is equal to X'F'.	6K5
YDFEN0	YD function enable - low active enables the YD function field decoder.	7J3

CHAPTER 10
CPU-B BOARD

10.1 INTRODUCTION

The CPU-B board contains the main Arithmetic Logic Unit (ALU), the register stack, the Program Status Word (PSW) register, the Flag Register (FLR), and a 32-bit Shift Register (SR). Logic is also located on this board to perform fixed-point multiply, divide, and shift operations.

All of the above functions are described in this chapter. The functional schematics for the CPU-B board, 35-768D08, should be used as a reference for this chapter.

10.2 INTERNAL PROCESSOR BUSES

Within the CPU, data is transferred between the various registers of the processor over three distinct 32-bit buses. These are identified as the A bus, the B bus, and the S bus.

Data from the source registers, specified by the microprogram, is gated onto the A and B buses and presented to the B and A inputs of the ALU, respectively. The ALU, in turn, performs the operation specified by the microprogram. The result of that operation is formed at the outputs of the ALU and is called the S bus. Data on the S bus is loaded into the indicated destination register. The A and B buses are high impedance buses formed by devices with 3-state outputs. The only source on the S bus is the output of the ALU and is, therefore, driven by totem pole devices.

10.3 ARITHMETIC LOGIC UNIT (ALU)

The ALU section comprises a 32-bit parallel arithmetic/logic network using a fast look-ahead carry. The arithmetic or logical result, performed by the ALU network, is formed on the 32-bit S bus. Refer to the table on Sheet 14 of the functional schematics for information concerning the logical level of the select and mode inputs to the ALU integrated circuits for the functions used. Each ALU function used is described in the following paragraphs. All gate references are to the arbitrary labels on Figure 10-1.

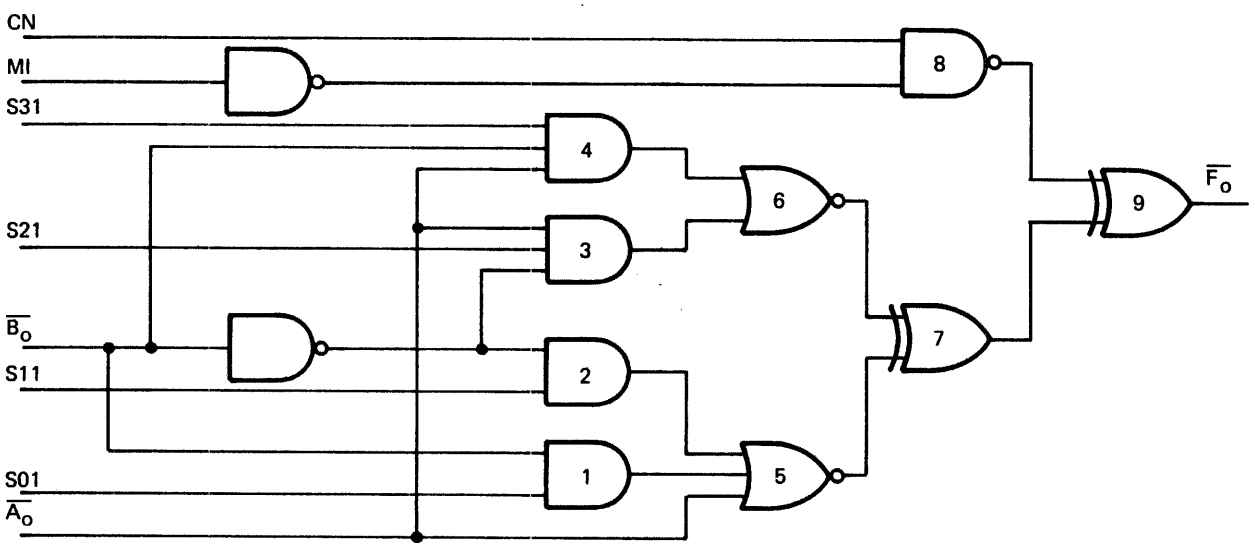


Figure 10-1 Least Significant ALU Stage

10.3.1 AND

The AND function, produced by the AND microinstruction, conditions the ALU to logically AND each bit from the output of the B bus shifter with the cutput of the A bus multiplexor. In this mode, the output equation for gate 5 is (Bo.Ao) and the output equation for gate 6 is (Ao). The simplified expression for the output from gate 7 is (Ao.Bo). Since gate 8 is disabled by the M1 input to the ALU, its output is high, causing the output from gate 9 to be defined by the same equation as the output from gate 7, the AND function.

10.3.2 OR

The OR microinstruction causes each bit from the output of the B bus shifter to be logically ORed with the corresponding bit from the gated output of the A bus multiplexor. Gate 5 produces a low because of the complementary Bo inputs. The outputs equation for gates 6 and 7 is (Ao+Bo) which corresponds to the $\overline{Fo}$ output from gate 9.

10.3.3 Exclusive-OR

The Exclusive-OR microinstruction produces a logical low at the S bus if the corresponding bits from the output of the B bus shifter with the output of the A bus multiplexor are at different logic levels. The expressions for the outputs from gates 5 and

6 are (Ao.Bo) and (AoBo), respectively. The function of the output from gate 7 is, therefore, $Ao\overline{Bo}+\overline{Ao}Bo$, the Exclusive-OR function. Since the output from gate 8 is again high, $\overline{Fo}$ is the same as the output from gate 7.

10.3.4 Add

The ALU is conditioned to the Add mode, an Add microinstruction. Note that with the exception of the M1 control line, Add is the same as Exclusive-OR. The M1 control line enables the Carry network internal to the ALU device so that the output from gate 8 is CN. The function, Fo, now becomes CN (AoBo+AoBo)+CN (AoBo+AoBo). Figure 10-1 shows only the least significant stage of the 19-067 4-bit ALU. The next three stages are identical except for the internally propagated carry.

10.3.5 Subtract

The Subtract function produced by the 4-bit ALU device is A-B-1. For this reason, the carry-in to the least significant stage is inverted by the Exclusive-OR gate (14C1) on a Subtract microinstruction. The output equation for gate 5 is (Ao.Bo) and the equation for gate 6 is $(Ao+\overline{Bo})$. Gate 7 produces a high output when the equation (Ao.Bo+AoBo) is satisfied. The output function, $\overline{Fo}=CN\ (\overline{AoBo})+\overline{CN}\ (AoBo+A\overline{oBo})$, yields A-B.

10.3.6 Load B

For the Load B operation, the ALU is conditioned to the F=A mode since the B bus shifter is tied to the A input to the ALU. In this mode, gates 1, 2, 3, and 4 are enabled by S01, S11, S21, and S31, respectively, and gate 8 is disabled by M1. Since both gates 1 and 2 are enabled, at least one of their outputs is high, producing a low at the output from gate 5. The state of gate 6 is the inverse of $\overline{Ao}$. If $\overline{Ao}$ is low, the output of gate 7 is high and the output of gate 8 is low ($\overline{Fo}$). For $\overline{Ao}$ high, the inverse is true at each stage, causing $\overline{Fo}$ to also be high. Therefore, in this mode, the state of $\overline{Fo}$ is the same as the state of $\overline{Ao}$, independent of the $\overline{Bo}$ input. The state of the gated B bus is passed, unmodified, to the S bus.

10.3.7 Load A

During a Load A, the ALU is conditioned to the F=B mode since the A bus is tied to the B inputs to the ALU. In this mode, gates 1 and 3 are disabled, gates 2 and 4 are enabled, and gate 8 is disabled by M1. If the $\overline{Bo}$ input is low, the output of gate 5 is low and the output of gate 6 is high, causing two highs at the inputs to gate 9 and a low at $\overline{Fo}$. When $\overline{Bo}$ is high, the inputs to gate 7 are equal (both low if Ao is high or both high if $\overline{Ao}$ is low), causing $\overline{Fo}$ to follow $\overline{Bo}$.

10.4 REGISTERS

10.4.1 Register Stack

The 8 sets of 16 user general registers, 4 microregisters used by the microprogram, and the 16 auxiliary registers used for interruptible instructions are all located in the register stack (Sheets 8, 9, 10, and 11).

The register stack is actually comprised of two separate stacks with common inputs and independent outputs forming a dual output port stack. Any of the registers may be accessed on the A stack, independent of the register specified on the B stack. Since the inputs to the A stack and B stack are common, the corresponding registers in each half contain identical information.

Data inputs to the register stack (DIN000-DIN310) are generated from 2:1 multiplexors (Sheets 8 and 9). In the normal mode, these multiplexors are conditicned to select the S bus data. The only exception to this is during a divide operation. (Refer to Section 10.6.) The outputs of the register stack are stored by transparent octal latches. During the read mode, READOA and READOB inactive (6H5), these latches are in the transparent mode. The outputs follow the inputs. When READO goes active, the data present at the inputs becomes latched. (Refer to Figure 10-2.)

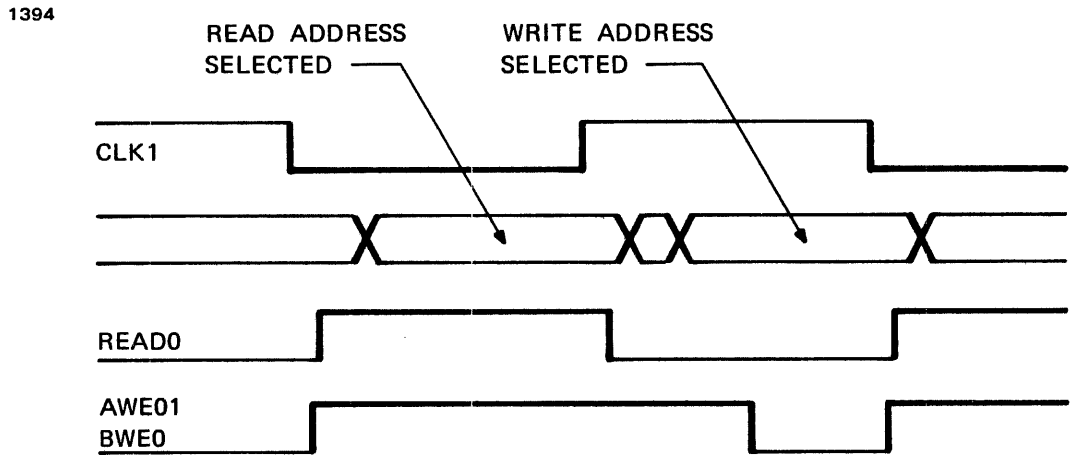


Figure 10-2 Register Stack Timing

The address and chip select inputs to the register stack are generated on Sheets 6 and 7 of the functional schematics. The functions are decoded separately during the read and write porticns of the cycle using AND/NOR gates, so that different

registers within the stack may be accessed and modified for a single microinstruction. Refer to the table on the upper right-hand quarter of Sheet 7 for information on the logic levels of the various address lines for the specific register being used.

10.4.2 Shift Register

The Shift Register (SR), located on Sheet 12, is a 32-bit register which may be used as a general purpose register by the microprogram, or may operate in either a shift right mode or a shift left mode for multiply and divide operations (refer to Sections 10.5 and 10.6). The SR is also used in conjunction with the B bus shifter for 64-bit shift operations. Refer to the table on Sheet 12, location S8, for information on the logical states of the select inputs for the various modes of operation for the shift register.

The decoding for the mode select inputs to the SR is located on the functional schematics for the CPU-A board, 35-767D08, Sheet 13.

10.4.3 Program Status Word (PSW) Register

The Program Status Word (PSW) register contains the status portion of the user's PSW. The status portion of the PSW is 32 bits long. Only 24 bits, however, are implemented in the hardware of this machine. PSW bits 00:07 are forced to appear reset when the PSW is unloaded.

The PSW, located on Sheet 13 of the functional schematics, is constructed using 19-231 integrated circuits. This device is a 4-bit edge-triggered latch with both totem pole (Q) and tri-state (Y) outputs. The Y outputs are used to form the A bus while the Q outputs are used for decoding functions.

Bits 08:27 are loaded on the trailing edge of CLK1 from the S bus when PSW is the selected destination register (CLKPSW0 active). The condition code portion of the PSW, bits 28:31, is copied from the flag register on the leading edge of the next SCLK1 after jam condition code is specified by the microprogram (CLKCC0 active). The tri-state outputs of the PSW are enabled when PSW is the selected A bus source, 03T03 low (13E9).

10.4.4 Flag Register (FLR)

The Flag Register (FLR) (Sheet 15) is a 4-bit register which contains additional information about the last logical or arithmetic microinstruction. The FLR contains the Carry flag (C), the Overflow flag (V), the Greater Than flag (G), and the Less Than flag (L).

The FLR is loaded from the S bus whenever either the FLR or the PSW register is specified as a destination. The contents of the FLR are copied into the CC when Jam CC is specified. The outputs from the FLR are also used by the branch circuit for conditional branches.

On any microinstruction other than a branch, and if the FLR and PSW are not the specified destination registers, the FLR is modified as follows:

1. Carry Flag - The C flag sets on an add operation if the carry-out of the ALU look-ahead carry circuits (CARRY1) (2B9) is active, or on a subtract operation if CARRY1 is inactive. The C flag is modified on shift operations according to the state of the B bus bit indicated in Table 10-1. The C flag sets if the corresponding B bus bit is set and resets if the B bus bit is inactive. For all other cases, the C flag is reset.

TABLE 10-1 SHIFT TABLE

OPERATION	B BUS BIT
Shift left halfword logical (16 bits)	B161
Shift left halfword arithmetic (16 bits)	B171
Shift left logical (32 bits)	B001
Shift left arithmetic (32 bits)	B011
Shift right halfword logical (16 bits)	B311
Shift right halfword arithmetic (16 bits)	B311
Shift right logical (32 bits)	B311
Shift right arithmetic (32 bits)	B311

2. Overflow Flag - The V flag is set on an Add if:

   - the B bus number sign is positive, and if the B bus sign is the same as the A bus sign and the resulting sign (S bus) is negative.

   - the B bus number is negative, and if the B bus sign is the same as the A bus sign and the result is positive.

   This flag is also set on a Subtract operation if the B bus sign is positive and the signs of the B bus and A bus differ and the result sign is negative, or if the sign of the B bus is negative and the B and A bus signs differ and the result is positive. For all other combinations of A, B, and S bus signs on Add and Subtract, the V flag becomes reset.

3. Greater Than and Less Than - The G flag is set if the result of the operation is not zero and the sign bit is not set. (For fullword operations (32-bit), the sign bit is S001; for halfword operations (16-bit), the sign bit is S161.) The L flag is set if the sign bit is active. Either flag is reset if its corresponding conditions are not met.

10.5 MULTIPLY OPERATIONS

Since a signed multiply algorithm is used, no special set-up is required for the operands. (Refer to Figure 10-3.) During a multiply, the ALU is conditioned to the Add mode and the B bus shifter and SR are conditioned to the shift right mode.

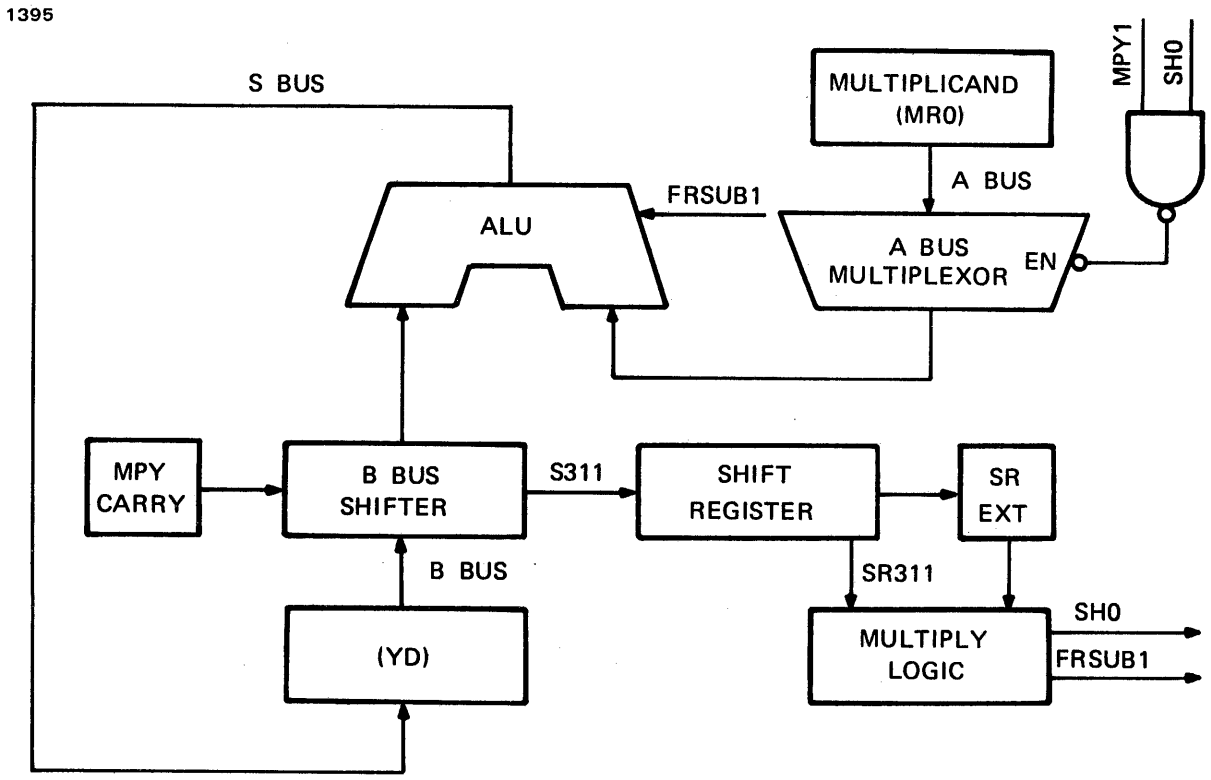


Figure 10-3 Simplified Block Diagram for Multiply

Refer to Table 10-2 to determine the function to be performed for each setting of SR131 and the SR extension (SR EXT) bits. If a shift operation is required (SH1 active) (14G9), the A bus multiplexor is disabled, forcing the B bus data to be shifted by the B bus shifter and added tc zero. When a subtract is called for, the ALU select bits are changed from an add, as indicated by the microprogram, to a subtract (FRSUB1 active) (14H8), yielding B minus A. The Add mode is selected by default.

TABLE 10-2 MULTIPLY TABLE

SR311	SR EXT	OPERATION
0	0	SHIFT
0	1	ADD
1	0	SUBTRACT
1	1	SHIFT

10.5.1 Halfword Multiply

Initial Setup

MR0 bits 0:15=multiplicand
MR0 bits 16:31=zero
SR bits 16:31=multiplier
Counter=16

Operation

1. Shift YD right one place, bringing in multiply carry (MPCY1).

2. Test SR311, SR EXT

   If 0,0 or 1,1 - Load YD with shifted data (A bus multiplexor disabled). MPCY=last value of MPCY1.

   If 0,1 - Load YD with multiplicand added to shifted data. MPCY1=sign of multiplicand.

   If 1,0 - Load YD with multiplicand subtracted from shifted data (FRSUB active). MPCY=sign of multiplicand.

3. Shift SR right one place.

4. Repeat 1, 2, and 3, 15 times.

5. Shift YD right one place to YD.

Result

Result is contained in YD.

10.5.2 Fullword Multiply

Initial Setup

MR0=multiplicand
SR=multiplier
Counter=32

Operation

Same as halfword multiply, Section 10.5.1.

Result

Most significant 32-bit result in YD; least significant 32-bit result in SR.

10.6 DIVIDE OPERATIONS

During a divide microinstruction, the ALU is conditioned to the Add mode; the B bus shifter and shift register are conditioned to the shift left mode. Prior to executing a divide, the microprogram ensures that the divisor is in two's complement negative form and the dividend is positive. Refer to Figure 10-4 for a simplified block diagram of divide operations.

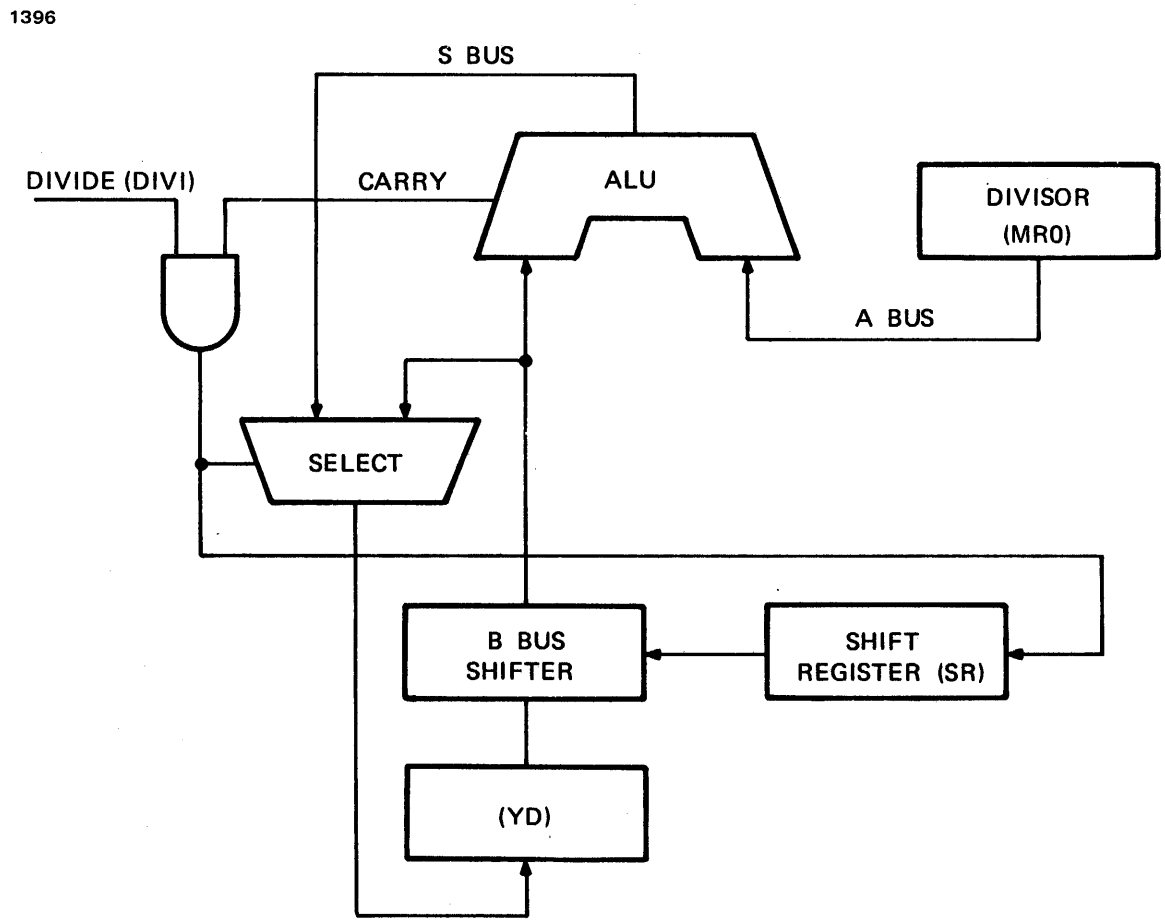


Figure 10-4 Simplified Block Diagram for Divide

10.6.1 Halfword Divide

Initial Setup

MR0 bits 0:15=divisor
MR0 bits 16:31=zero
YD=positive dividend (32 bits)
Counter=16

Operation

1. Shift YD left one place and add to divisor.

2. Test for carry-out from ALU.

   If Carry=1, load YD from S bus and shift SR left, bringing in Carry.

   If Carry=0, load YD from shifted B bus (shift only) and shift SR left, bringing in zero.

3. Repeat 1 and 3, 16 times.

Result

YD bits 16:31 contain remainder.
SR bits 16:31 contain quotient.

10.6.2 Fullword Divide

Initial Setup

MR0=divisor
YD=most significant 32 bits of dividend
SR=least significant 32 bits of dividend
Counter=32

Operation

1. Shift YD left one place and add to divisor.

2. Test for carry-out from ALU.

   If Carry=1, load YD from S bus and shift SR left, bringing in Carry.

   If Carry=0, load YD from shifted B bus (shift only) and shift SR left, bringing in zero.

3. Repeat 1 and 2, 32 times.

Result

YD=remainder
SR=quotient

10.7 B BUS SHIFTER

The B bus shifter (Sheets 2 through 5) performs all the shift functions indicated by the shift control field of the microformat word, except sign Extension (EXT). For EXT, the B bus shifter is conditioned to the load mode and the sign extension is actually performed on the CPU-C board.

The shift control ROM data bits, RD201-RD231, are decoded by three Read-Only-Memories (ROMs, Sheet 14) in order to condition the integrated circuits forming the shifter to the correct mode for each operation. The table provided in the schematics indicates the information contained in the ROMs.

Generally, the B bus shifter is constructed by using two tri-state 2:1 multiplexors that are wire OR-tied for four bits. One multiplexor provides the Load and Exchange Halfword functions, while the other provides for shifting left or right one position. For bits 16:31, a tri-state buffer is also provided to implement exchange byte. Additional open collector AND/NCR gates are used at bit positions 0, 16, and 31 to control bits shifted into the B bus shifter at the boundary positions.

10.8 MNEMONICS

The following is a list of mnemonics found on the CPU-B board. The meanings and 35-768D08 schematic source of each signal are also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
A001-A311	A bus. A source data bus.	10H
ADD1	Add operation decoded.	14G2
AENH0	Enable for the most significant 8 bits of the A bus multiplexor.	2H1
AENL0	Enable for the least significant 24 bits of the A bus multiplexor.	3N1
AMUXS0	The select input to the A bus multiplexor.	13E9
AMX000	The most significant bit of the A bus multiplexor. The second operand sign bit.	2D6

MNEMONIC	MEANING	SCHEMATIC LOCATION
ASTKS0	Output enable for the A stack latch.	13C8
AWE0	Write enable to the A half of the register stack.	6K5
AYDEN1	Enables the A stack address decoding logic to look at the YD field of the Instruction Register (IR).	6C4
AYSDEN1	Enables the A stack address decoding logic to select the general registers or alternate register set.	6A4
AYSEN1	Enables the A stack address decoding logic to look at the YS field of the IR.	6C4
B001-B311	B bus - B source data bus.	Sheets 8,9
BMC001-BMC111	B bus shifter control bits used for selecting the operation to be performed by the B bus shifter.	Sheet 14
BMX000-BMX310	Outputs of the B bus shifter used as the first operand to the ALU.	Sheets 2,3, 4,5
BRD200	Buffered ROM data bit 20.	14M9
BRD210	Buffered ROM data bit 21.	14M8
BSTKS0	Output enable for the B stack latch.	8F4
BWE0	Write enable to B stack.	8D1
BYDEN1	Enables the B stack address decoding logic to look at the YD field of the IR.	7C4
BYSDEN1	Enables the B stack address decoding logic to select the general registers or alternate register set.	7A4
BYSEN1	Enables the B stack address decoding logic to look at the YS field of the IR.	7C4
CARRY1	Carry out from the ALU.	2B9
CISR1	Carry in to bit zero of the shift register.	5N9

MNEMONIC	MEANING	SCHEMATIC LOCATION
CLFLR0	Clear the flag register. Clears the flag register for I/O operations if FLR is not the destination.	15N2
CLK1B	Basic system clock.	6J1
CLKCC0	Clock condition code. Copies FLR to condition code register.	13E3
CLKPSW0	Clock program status word. Loads status portion of the PSW.	13E8
CN08111	Carry out from bits 8:11 of ALU.	2C7
CN12151	Carry out from bits 12:15 of ALU.	2A8
CN24271	Carry out from bits 24:27 of ALU.	4C7
CYIN1	Carry in to least significant ALU.	14D1
DCLK0	Destination clock low active.	6H3
DCLK1	Destination clock high active.	6H3
DIN000-DIN310	Data input to register stack.	Sheets 8,9
DIV1	Divide operation decoded.	8G8
DSTOP0	Destination stop. Disables destination clock when required.	6J1
ENBS0	Enable B source. Gates bits 0:15 of SR or all zeros onto the B bus.	12A9
EXB0	Exchange byte. Condition B bus shifter to perform an exchange byte operation.	4C1
FLR281	Carry flag	15N8
FLR291	Overflow flag	15N6
FLR301	Greater Than flag	15N4
FLR311	Less Than flag	15N2
FRSUB1	Force subtract. Changes the mode of the ALU from an add operation to a subtract operation during a multiply.	14J9

MNEMONIC	MEANING	SCHEMATIC LOCATION
GO811	Generate out from bits 8:11 of ALU.	2B5
GO12151	Generate out from bits 12:15 of ALU.	2B5
G16311	Generate out from bits 16:31 of ALU.	2C8
G24271	Generate out from bits 24:27 of ALU.	4B5
G28311	Generate out from bits 28:31 of ALU.	4B5
GFLR291	Gated overflow flag. Set overflow when false SYNC is detected on an I/O operation.	13E3
GPSWXX1	Gated PSW bits 25, 26, and 27. These bits are forced high when the alternate register set is selected by the microprogram.	13L4
GRD091	Gated ROM data bit 9. RD091 forced high for HPFPP operations.	14B1
GRD101	Gated ROM data bit 10. RD101 forced high for HPFPP operations.	14B4
GRD111	Gated ROM data bit 11. RD111 forced low for HPFPP operations.	14B2
HZERO1	Halfword zero. An all-zeros condition detected on bits 16:31 of the S bus.	15D4
JAMCIO	Jam carry in to ALU decoded.	14B1
LOAD1	The ALU conditioned to the load mode. F=A or F=B.	14G1
LFLRO	Load flag register. The flag register is the selected destination register.	15E9
M1	Mode select to the ALU. Conditions the ALU to the logical mode when high.	14G1
MPCY1	Multiply carry. Carry in to bit 0 of B bus shifter during a multiply.	14G7
MPYO	Multiply operation decoded.	14C9
PO8111	Propagate out from bits 8:11 of ALU.	2C5

MNEMONIC	MEANING	SCHEMATIC LOCATION
P12151	Propagate out from bits 12:15 of ALU.	2B5
P16311	Propagate out from bits 16:31 of ALU.	4B8
P24271	Propagate out from bits 24:27 of ALU.	4B5
P28311	Propagate out from bits 28:31 of ALU.	4B5
PSW081:271	The Q outputs of the Program Status Word register.	Sheet 13
RAA00:70	Address bus to the A half of the register stack.	Sheet 6
RBA00:70	Address bus to the B half of the register stack.	Sheet 7
RDXX0	ROM data bits low active.	Sheets 6, 7,13
RDXX1	ROM data bits high active.	Sheets 6, 7,13
S000-S310	S bus. Low active outputs of the ALU.	Sheets 2,3, 4,5
S001-S311	S bus. Buffered outputs of the ALU.	Sheets 2,3, 4,5
SCLK1	Skewed clock. A clock skewed by 50 ns past CLK1.	6J1
SCLR0B	System clear. Initialize signal to the B board.	12A1
SH0	Shift. Disables the A bus multiplexor during multiply operations when a shift only is required.	14J9
SHCRY1	Shifted carry. The input to the C flag during shift operations.	15E1
SR00-SR10	The select inputs to the shift register.	12A9
SR001-SR311	Outputs of the shift register.	Sheet 12
SSEL0	Select line to the input multiplexors of the register stack.	8J9
SUB1	Decoded subtract operation.	14G2

MNEMONIC	MEANING	SCHEMATIC LOCATION
ULSRO	Unload shift register. Selects the SR as the B bus source.	12A1
XRP1	External pullup resistor.	6E1
YD081-YD111	The user destination field of the instruction register.	Sheet 6
YS01-YS031	The user source field of the instruction register.	Sheet 6
ZER01	All zeros detected on the most significant 16 bits of the S bus.	2N7
ZERRO	All zeros detected on the full 32-bit S bus.	15E4

CHAPTER 11
CPU-C BOARD

11.1 INTRODUCTION

The CPU-C Board, Part Number 35-769, contains the processor's Location Counter (LOC), Memory Address Register (MAR), and the Memory Data Register (MDR). In addition, the CPU-C contains the MDR adder (or summer) which is used during calculate address for RX2 and RX3 user instructions. The C board also has the Memory Address Translator (MAT) logic which provides memory address relocation and protection.

The functional schematics for the CPU-C board, 35-769D08, should be used as a reference for this chapter.

11.2 PROCESSOR MEMORY ADDRESS LOGIC

11.2.1 Memory Address Register (MAR) and Fault Memory Address (ZMAR) Register

Refer to Sheets 2, 6, 7, 14, 15, and 16 of Functional Schematic 35-769D08 during this discussion.

The MAR is a 24-bit register/counter. The contents of MAR are used for addressing a specific location in memory. If the Program Status Word (PSW) bit 21 is set, the contents of MAR are used by the MAT to generate a new (relocated) address.

MAR is loaded from the S bus when the microinstruction specifies Load MAR (LMAR0) or a Decoded Instruction Read (DIR0), provided MAR Stop (MARSTP0) is inactive. If the microinstruction calls for Increment MAR (IMAR0), the register increments by four. The load or increment occurs on the trailing edge of CLK1C unless Memory Stop (MSTOP0) is active.

The output of MAR (MAR081:311) connects to the program address multiplexors and the ZMAR multiplexors. MAR081:151 are also output to the multiplexors that source SPA081:151 for the MDR adder.

When DIR0 is not active, MAR081:311 drive program address lines PA08:31 which feed the program address latch, FPA081:311. These lines also input to the ZMAR multiplexors. The FPA register latches the current processor memory access when the Data Unavailable flip-flop (FDUA0) goes active. The ZMAR multiplexors normally output MAR081:311 on their corresponding ZMAR lines.

however, if during a memory access a memory fault occurs (i.e., alignment, MAT fault or uncorrectable error), Enable Interrupt MAR (EIMAR1 and EIMAR0) go active to output the contents of the FPA register to ZMAR lines, and to inhibit the FPA register from latching a new program address. A microinstruction, specifying MAR as a source after a memory fault, Unload MAR (UMAR), retrieves the faulting address from ZMAR via the B bus multiplexors. (Note that the faulting address is the program address unmodified, even if MAT is enabled.) All subsequent MAR reads return the contents of MAR.

MAR081:MAR151 through SPA081:151 and FPA161:311 input to the MDR adder during Calculate Address (CAMA0).

11.2.2 Location Counter (LOC)

Refer to Sheets 2, 6, 7, 14, 16, 22, and 23 of 35-769D08.

The LOC is a 24-bit register/counter and its contents always point to the address of the next user instruction to be executed. On an instruction fetch, LCC is used during calculate address. LOC is loaded from the S bus when it is specified as the destination by the microinstruction and Destination Stop (DSTOP0) is not active. In addition, LOC is incremented by 2 when Increment LOC is active during calculate address. The load or increment is performed on the trailing edge of CLK1C.

The LOC outputs, LOC081:301, input to the program address multiplexors and B bus multiplexors. LOC081:151 drive the multiplexors that source SPA081:151 for the MDR adder. Note that LOC311 is not implemented and is forced reset.

11.2.3 Program Address Multiplexors (PA MUX)

Refer to Sheets 6, 7, and 16 of 35-769D08

The PA MUX selects either the LOC or MAR outputs. LOC outputs are selected during instruction fetch and calculate address; the MAR outputs are selected at all other times. PA081:311 input to the program address latch. PA081:151 connect to the Process Segment Table Entry (PSTE) comparator and the MAT relocation summer. PA081:201 are used by the program address relocation summer and PA211:311 input to LMA drivers. The segment limit detection involves PA161:201. PA301 is transmitted to the CPU-D board and defines the halfword memory boundaries. PA080:150 are used to select one of 256 Segment Table Entries from the MAT register stack.

11.2.4 Memory Data Register Summer (MDRΣ)

Refer to Sheet 20 of 35-769D08 during this description.

The MDR summer (MDRΣ) is a 24-bit full adder using bits 8:31 of the Memory Data Register (MDR) and the 24-bit PA multiplexor

outputs as the numbers to be added. The MDR is used exclusively during calculate address to determine the address displacement of the second operand for RX2 and RX3 instructions. The RX2 and RX3 format instructions require three values to arrive at the program address of the second operand data to complete the instruction. The RX2 format requires that a 15-bit displacement (negative or positive) in the second halfword of the instruction be added to an index value contained in a general register specified by the YS field of the Instruction Register (IR). The result of this addition is then added to the value of the incremented LOC (location of next instruction). This final number is the program address of the second operand. The RX3 format requires that the least significant 24 bits of MDR (represented by the least significant 24 bits of the 48-bit RX3 instruction) be added to an index value contained in the general register specified by the YS field of the IR. The result is then added to a second index value contained in the general register specified by MDR bits 4:7. This final number is the program address of the second operand.

The MDRΣ provides the ability to add three numbers together in a single microinstruction. During an RX2 address calculation, the incremented LOC and the least significant 15 bits of MDR are added and provided as SUM8:31. The MDR data is sign extended at the inputs of the MDRΣ by 2:1 multiplexors and logic on MDR161. The MDR during RX2 contains the same data in both halfwords of the MDR. MDR bit 01 represents the sign of MDR displacement data. The state of MDR bit 01 is forced on the adder inputs from bits 16:12. This provides either a negative or positive displacement. The PA multiplexor has the incremented LOC on its outputs. The MDR, when specified as a B bus source during calculate address of the RX2 format, yields the added MDR and LOC. If the RX3 format second operand address is being calculated, the MAR contains the first level index indicated by the YS field of the IR. The first level index and the MDR displacement are added and supplied as the MDR data on the B bus.

11.2.5 Memory Address Bus Drivers

Refer to Sheets 10 and 12 of 35-769D08 during this description.

The memory address bus drivers provide a 24-bit physical address in memory on the LMA080:310 lines. These lines are active if the processor or MAT access the memory. A set of tri-state line drivers is provided for each. On a processor access of memory, ENRPA0 (Enable Regular Path) outputs the program address relocation summer and PA211:311 to the LMA bus. On a MAT access, ENMAA0 (Enable MAT Access) outputs the MAT relocation summer and four gated MAT bits, GMA251:281 to LMA, and LMA290:310 are forced inactive.

11.3 PROCESSOR MEMORY DATA LOGIC

11.3.1 Processor Memory Data Register

Refer to Sheets 17, 18, and 19 of 35-769D08 during this description.

The MDR is a 32-bit register used by the microprocessor to receive or send data to memory.

Data loaded into the MDR from the MDR data multiplexors may come from two different sources: the S bus when the microinstruction specifies the MDR as a destination, or the Memory Data Sense (MDS) bus during instruction read or memory read operations. The MDR is split into two halfwords: MDH and MDL. Each may be loaded independently. On a fullword read, a fullword of data is loaded into the MDR. On a halfword read, only MDL (MDR16I:311) is loaded. For an instruction read on a fullword address boundary, MDS160:310 are loaded into both MDH and MDL. On an instruction read that resides on a halfword boundary, MDR is not loaded. If a second halfword has to be fetched for the instruction, it is loaded into both halves of MDR.

11.3.2 Memory Data Multiplexors

Refer to Sheets 17, 18, and 19 of 35-769D08 during this description.

The memory data multiplexors select the data to be loaded into the MDR and the bus from which it is loaded: the MDS bus or the processor S bus. When selecting the buffered MDS bus, the memory data multiplexor can load either the most significant or least significant halfword of MDS into MDRH or MDRL. The MAT status register also may be loaded into the MDRL. This occurs when a microinstruction specifies a memory read operation and Reset Fault (RFAULT) is specified by the microprogram with a MAT interrupt queued. The memory operation must be performed within resident local memory. When these conditions are satisfied, the multiplexors output the MAT status bits EMAT291:311 to the MDR forcing zeros on all other bits.

11.3.3 Local Memory Data Bus Drivers

Refer to Sheet 21 of 35-769D08 during this description.

The local Memory Data Bus (MDB) drivers supply the data to be written into memory by the processor. The MDB drivers are connected to the MDS bus, which is a bidirectional data bus used for reading from and writing to memory. The MDB drivers are enabled only during a memory write operation provided that the MAT does not require an access (FMATCY1). Halfword memory write operations from the processor always position the halfword to be written in the MDR (bits 16:31). This data may be written to a

halfword or fullword boundary. MDR161:311 drive MDS160:310 on any processor to memory write operation (LWRTO, LHWRTO). To write a halfword to a fullword boundary, LHWRTO is active to output MDR161:311 to MDS000:150.

11.4 MEMORY ADDRESS TRANSLATOR (MAT)

11.4.1 MAT Function

When the MAT is disabled, the program address lines (PA081:310) directly address the memory via the local memory bus (LMA080:310). With MAT enabled, the memory location specified by LMA080:310 is the sum of the least significant 16 bits of the program address (PA161:311) and a bias value contained in an entry of the Process Segment Table (PST) in memory.

The PST for a task can consist of a maximum of 256 contiguous double fullwords or entries. Only the first 32 bits of an entry are of significance to the hardware. The starting address of the PST is specified by the Process Segment Table Descriptor (PSTD). The CPU-C board has a PSTD register which is loaded from the MDR on command from a microinstruction - Load PSTD (LPSTD). The PSTD register is implemented in hardware as shown in Figure 11-1.

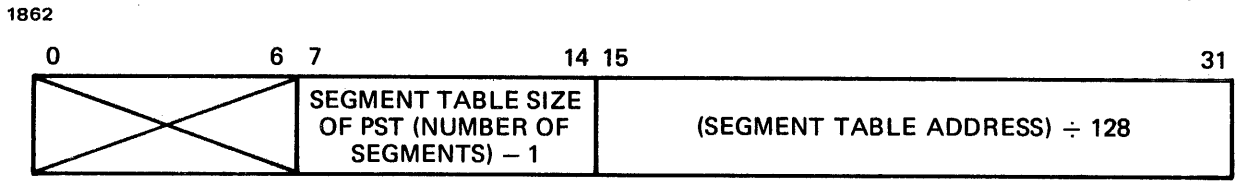


Figure 11-1 Process Segment Table Descriptor (PSTD)

When the MAT is enabled, the program address is considered to consist of two fields - the segment field and the offset field, as shown in Figure 11-2. With PSTD bits 15:31, PA08:15 are used as an index into the PST to select an entry. The accessed entry indicates if it is private or shared. If private, the Segment Table Entry (STE) contains the starting address of a segment in memory to which the offset field of the PA serves as an index. If PA08:15 is greater than the segment size specified by the PSTD, a MAT fault is generated.

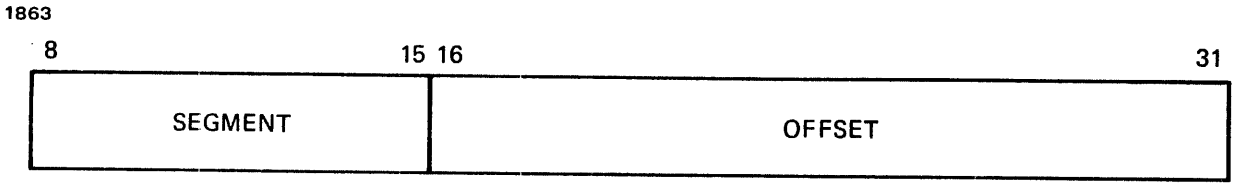


Figure 11-2 Program Address (MAT Enabled)

If the entry is shared, the Shared Segment Table (SST) must be accessed to obtain the STE. The SST can consist of 8,192 double fullwords or entries. The starting address in memory of the SST is contained in the Shared Segment Table Descriptor (SSTD). The CPU-C board has an SSTD register which is loaded from the MDR on command by a microinstruction - Load SSTD (LSSTD). The SSTD is implemented in hardware as shown in Figure 11-3. Before the SST is accessed, the shared segment size in the STD is compared with the PST STE. If SSTD bits 2:14 are less than the STE size, a MAT fault results; if not, the SST is accessed. SSTD bits 15:31 point to the first location in the SST and the STE serves as an index. The STE obtained from the SST points to the segment in memory and PA16:31 index into the segment. Only the first 32 bits of a Segment Table Entry relate to the hardware. An STE, whether private or shared, has the format shown in Figure 11-4.

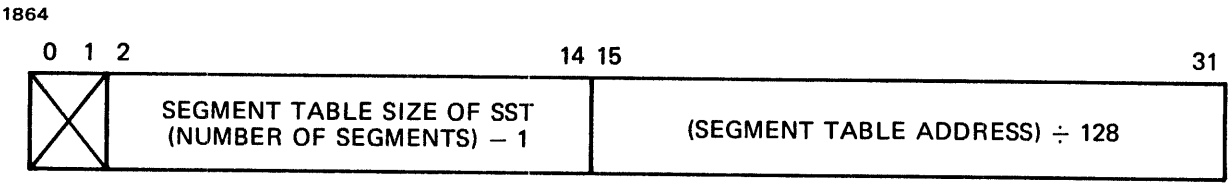


Figure 11-3 Shared Segment Table Descriptor (SSTD)

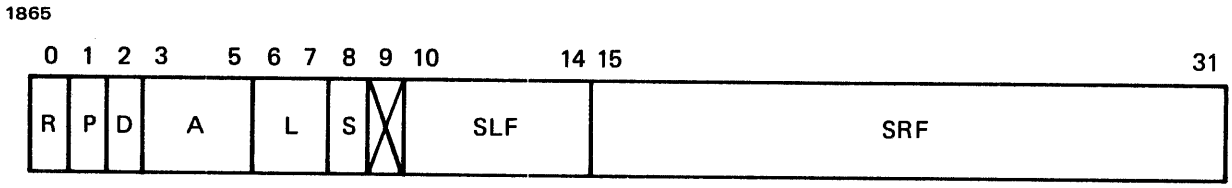


Figure 11-4 Hardware Segment Table Entry

The fields are defined as follows:

Bit(s)	
0	R - Reference Bit. This bit is set in the STE when the segment is accessed.
1	P - Presence Bit. This bit is set when the segment described is present in memory; it is reset when the segment is not present. A reference to a segment that is not present (P=0) results in a MAT fault and the CPU ignores bits 2:31 of the STE.
2	D - Dirty Bit. This bit is set by hardware when a Write is to be executed in the segment.
3:5	A - Access Mode Bits. The A field specifies the allowed modes of access to the segment. Bit 3, when set, allows read accesses; bit 4, when set, allows write access; and bit 5, when set, allows instruction read accesses. An attempt to access a segment in a mode that is not enabled results in a MAT fault.
6, 7	L - Access Level Bits. The L field is used in conjunction with PSW 10 and 11. If the contents of PSW 10 and 11 are greater than or equal to the L field, then access of the segment is allowed. If the contents of PSW 10 and 11 are less than the L field, a MAT fault occurs.
8	S - Shared Bit. If the Shared bit is zero, MAT performs the protection and the relocation functions as defined for a private segment. If S=1, the selected segment is shared. In this case, the SRF field of the PST STE is used in conjunction with the address contained in the STD as a byte offset into the Shared Segment Table. The S bit in the Shared Segment Table must be zero for all entries. The contents of the A fields of the PST STE and the SST STE are ANDed to determine the allowed access mode. All other protections and relocations are performed using the data from the SST STE.
10:14	SLF - Segment Limit Field. The SLF specifies the size of the segment. If the SLF is less than PA[16]1:20[1], a MAT fault results.
15:31	SRF- Segment Relocation Field. The interpretation of this field depends upon the state of the S bit. If S=0 in the PST, the SRF is the bias value of the segment divided by 128, to which the offset field of the program address is added to obtain the physical address in memory. If S=1 in the PST, the PST SRF is the byte offset or index into the SST where the STE for the segment is located. If the PSTE SRF is greater than

the segment size specified by the STD, a MAT fault results. Note that for a shared segment the least significant three bits of the PST SRF must be zero because the SST is aligned on a double fullword boundary. For all other cases, the least significant four bits must be zero as the SRF is the address of a segment aligned to a 2^{11} byte boundary divided by 2^{7}. As a result, bits 29:31 are not implemented in the hardware.

In order to eliminate repeated memory accesses to gain a segment entry, the CPU-C board stores the STE in a register stack when it is first obtained. The stack has a capacity for 256 entries. The only other memory access to an entry that resides in the stack would be to set the Dirty bit on a memory write operation if the access mode permits a write.

Two stacks are provided for the Presence bit. The Presence stacks must be set to zero whenever the CPU is powered up or initialized. When the PSTD register is loaded, a Presence stack is initialized to zero. When both stacks are in the process of initializing, the CPU is halted.

11.4.2 Process Segment Table Descriptor (PSTD) and Segment Size Comparator (Sheet 3 of 35-769D08)

The PSTD is loaded from MDR071:311 by Load PSTD (LPSTD0). The first eight bits - the segment size - are compared to PA081:151. An error (EPSTD1) is generated if the program address exceeds the segment size.

Segment Table Descriptor bits STD161:311 are disabled when GETSSTE1 is active. These bits are tied to those of the SSTD and input to the MAT Relocation Summer.

11.4.3 Shared Segment Table Descriptor (SSTD) and Shared Segment Size Comparator (Sheet 4 of 35-769D08)

The SSTD is loaded from MDR021:311 by DCLK1 when a Load SSTD (LSSTD0) is specified. The first 13 bits (the shared segment size) are compared with the Buffered Relocation bits BRF091:211. An error (ESSTD0) is generated if BRF091:211 is greater than the shared segment size when a shared STE is to be accessed.

STD151:311 are enabled on an STE memory access (GETSSTE0). These connect with those of the PSTD and input to the MAT Relocation Summer.

11.4.4 MAT Relocation Summer and LMA Drivers (Sheet 10 of 35-769D08)

The MAT Relocation Summer generates the memory address for the MAT when an STE must be obtained. The Segment Table Descriptor bits STD151:311 are input to the summer. On a nonshared access, PA081:111 are added to the STD bits. PA121:151 generate Gated Memory Address bits GMA251:281 and are input to the LMA drivers. When a Shared Segment Entry is to be obtained (GETSSTE0 active), Buffered Relocation bits BRF091:171 are selected for the addition and BRF181:211 assert GMA251:281.

The adder outputs and GMA251:281 connect to the LMA drivers when enabled by Enable MAT Access (ENMAA0A). LMA290:310 are forced inactive.

MAT Program Address bits MPA081:111 are used in decoding the memory that is to be accessed.

11.4.5 Stack Load Buffer (Sheet 8 of 35-769D08)

The buffer is loaded from the buffered Memory Data Bus (MDS lines) with an STE when MAT Cycle (FMATCY0) goes inactive. The buffer has both active and tristate outputs. The latter are enabled by Disable Stack (DISSTK0) when the STE is to be written in the Segment Table Register Stacks.

The following outputs connect to the stack:

PRES1 - Presence bit
DIRT0 - Dirty bit
LC1:11 - Access level bits
SLF01:41 - Segment Limit Field
SRF081:201 - Segment Relocation Field

The active buffer outputs FSHARED1 and the Buffered Access Mode bits BA01:21 connect to a tristate 2:1 multiplexor and a quad register which stores the bits if the buffer indicates that the PSTE is shared. The stored access bits are ANDed with BA01:21 of the shared STE. ASHARED1 selects the quad-register outputs, and the multiplexor drives SHARED1, A01, A11, and A21 of the stack.

The remaining active buffer outputs are Buffered Relocation bits (BRF091:211) which specify the Shared Segment Table Entry.

11.4.6 Segment Table Register Stacks (Sheet 8 of 35-769D08)

The MAT stacks consist of three 256x9 and two 256x1 Random Access Memories. The two Presence stacks - A stack and B stack - are accessed by AP081:151 and BP081:151, respectively. The remaining stacks are directly addressed by Program Address bits PA080:150.

The 256x9 stacks are always selected and the Presence stacks are enabled by A/B Chip Select (ACS0 and BCS0). The outputs of the stacks go tristate when Disable Stack (DISSTK1) and A/B Write Enable (AWE0 or BWE0) go active. The Presence bit is written to the selected stack by an active write enable. The 256x9 stacks are written into by Write Stack 0 (WSTK0).

11.4.7 MAT Control (Sheet 9 of 35-769D08)

The MAT control determines if the MAT requires a memory access. When a MAT memory cycle is necessary, the MAT control takes care of loading the stack buffer, writing into the stacks, and generating a MAT cycle to memory if the retrieved PSTE is a shared entry.

On initialize or power up (BSCLR0A), the MAT is disabled (MATEN1 low) until the PSTD register (LPSTDCK0) is loaded. The MAT is enabled when PSW 21 is set; a privileged memory operation (RD031) is not to be executed and Decoded Enable Clock is inactive. If a segment is not present in the stack or if present and a processor write to memory is to be performed, ENRAP0 is gated inactive and ENMA00 active. Figure 11-5 shows the timing waveforms for a MAT cycle tc memory.

ENRAP0 disables the LMA drives of the PA Relocation Summer and ENAMA00 enables those of the MAT Relocation Summer. ENMA00 goes to the CPU-D board 35-770 to initiate a memory cycle, and the MAT Read and Set Reference bit (MATRSR0) goes to the memory. The MAT Read and Set Dirty bit (MATRSD0) is sent to memory if the segment is to be written into and a write is permitted.

When FMATCY is set, it disables the MDS drivers to memory and allows FFMATCY to toggle set on the trailing edge of the CLK1 which directly sets FMATCY. Data Unavailable (DUA0) from memory is toggled into FDUA if it is active on CLK0. An inactive DUA0 allows FMATCY and FDUA to toggle reset on the trailing edge of CLK1. FMATCY0 going high toggles the MDS lines into the stack buffer. After FDUA0 goes high, the stacks are disabled (DISSTK1), SHCLK0 is generated and, if the segment is not shared, the stack is written into (WSTK0) from the buffer register. CLK0 then toggles FMATCY reset.

If FSHARED1 is active, GETSSTE0 is generated to indicate that another MAT cycle is required.

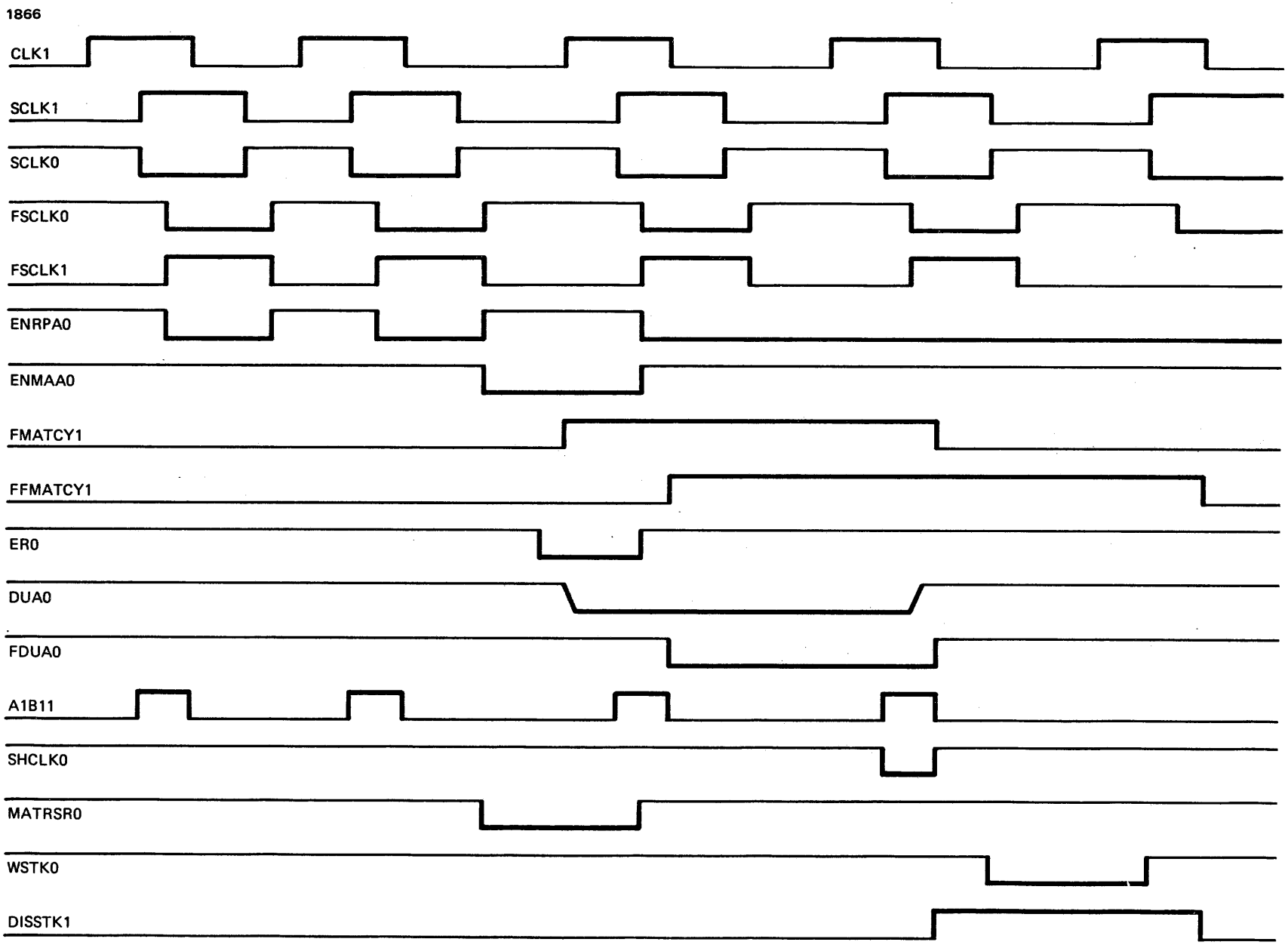


Figure 11-5 MAT Cycles to Memory Timing

11.4.8 Program Address Relocation Summer and LMA Drivers (Sheet 12 of 35-769D08)

When the MAT is disabled, PA081:201 are gated through the adder to the LMA drivers. PA211:311 connect directly to the drivers. With the MAT enabled (MATEN0), PA081:151 are zeroed to the adder. The Segment Relocation Fields - SRF081:201 and PA161:201 are summed. ENRPA0 enables the LMA drivers. Relocated Program Address bits (RPA081:111) are used in decoding the memory that is to be accessed.

11.4.9 MAT Fault Decode (Sheet 11 of 35-769D08)

On memory references when the MAT is enabled, the protect function comes into play. MAT interrupts (MATFALT0 and MAT) are set when a MAT violation occurs. The checks that are made are listed in the table on Sheet 11 - MAT Fault Codes. The fault code is generated by the 8:3-line priority encoder and the code is latched in EMAT291:311. It remains latched until Clear States (CLSTA0) goes active; this also clears the MAT. MATFLT0 can also set on a Memory Fault (MFAULT0) and is directly cleared by RFAULT0.

11.4.10 Presence Bit Initialization (Sheet 5 of 35-769D08)

Each of the Presence stacks has its own initialization control. The logic consists of a pair of 8-bit counters that are cleared by BSCLR0. This line also sets FAINCR and FBINCR and their associated J-K registers. With these registers set, Write Enable (AWE0 and BWE0) and Chip Select (ACS0 and BCS0) to the stacks go active. FAINCR1A and FBINCR1A select the output of the counters as the address (APA081:151 and BPA081:151) for their stacks. ACP1 and BCP1 increment the counters on the trailing edge of CLK1 until a carry is generated. At this time, A11 is allowed to toggle the first set of J-K registers reset and A/BWE0 and A/BCS0 are disabled and directly clear their respective FA/BINCR.

If neither stack is selected, the A stack is chosen when LPSTD1 goes active and generates APE1 to permit the first J-K to be toggled set and the A counter to be loaded from MDR080:150 by ACP1. The A stack remains selected while a new task is loaded in the PSTD. LPSTD1 now activates BPE0, allows the first J-K of the B stack logic to be toggled set, and enables the J input of FAINCR. BPE0 permits the B counter to be loaded from MDR080:150 by BCP1 and A1B11 toggles FAINCR set; the A stack then initializes. When both stacks are being initialized, MATSTOP0 is generated to halt the processcr.

11.4.11 Local/Shared Memory Detection (Sheet 13 of 35-769D08)

The chosen strapping option is a function of shared memory. The strapping shown is for no shared memory. RPA081:111 are generated by the Program Address Relocation Summer and MPA081:111 by the MAT Relocation Summer. If Processor to Shared Buffer Controller (PSBC0) is active, it indicates a shared memory access by the processor. If MAT to Shared Buffer Controller (MSBC0) is active, it indicates a shared memory access by the MAT.

11.5 B BUS MULTIPLEXOR

Refer to Sheets 22 and 23 of 35-769D08 during this description.

The CPU-C B bus multiplexor supplies the data contents of the register specified by the microinstruction B source field. The B bus multiplexor is capable of driving the B bus from the following four sources: memory data register (processor MDR), memory address register, location counter, and the memory data register adder output. The memory data register adder output is used only during the calculate address sequence of instruction reads. The MDR data contents may be sign extended from bit 16 of the MDR. The state of MDR 16 is propagated through to MDR bit 00. This is used for halfword reads from memory where MDR bits 0:15 are undefined. LOC is a 24-bit source. Bits 0:7 and bit 31 are forced reset by the B bus multiplexor when LOC is specified as the source. The MAR is a 24-bit source. Bits 0:7 are forced reset by the B bus multiplexor when the MAR is the specified source. When the MAR is the source under special conditions, the fault memory address register (ZMAR) contents are used instead of the MAR.

11.6 MNEMONICS

The following is a list of the mnemonics found on the CPU-C board. A brief description and the schematic source of each signal are provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
A01:21	Access mode bits	8B9
A1B11	Pulse generated from the AND of CLK1 and SCLK1	3H6
ACP1	A presence stack clock	5M3
ACTR080:150	A presence stack counter output	Sheet 5

MNEMONIC	MEANING	SCHEMATIC LOCATION
ALGNO	When low, a memory alignment fault has occurred. This fault may be caused by a fullword access to a halfword address or a halfword access to a byte address.	15F8
APA081:111 APA121:151	Program address bits for the A presence stack	Sheets 6 and 7
APE1	A presence stack counter load enable	5H2
ASHARED0	Shared bit of auxiliary register	8A5
ASHRD1	Second buffered shared bit	8C9
AXRP1	1 k ohm resistor connected to P5 - used to give noise immunity to unused inputs.	4R6
B001:311	Second operand data (B bus) from the CPU-C board - RD bits 24, 25, 26, and 27 determine the specific source register. The source registers may be: Location Counter (LCC), Memory Data Register (MDR), Memory Address Register (MAR), or Fault Memory Address Register (ZMAR) and the adder output of the MDR (SUM). The MDR may be sign extended from bit 16:00.	Sheets 22 and 26
BA01:21	Access mode bits of stack buffer	8C3
BCLR0	B net of system clear	3L7
BCP1	B presence stack clock	5M9
BCS0	B presence stack chip select	5M6
BCTR080:150	B presence stack counter output	Sheet 5
BPA:081:111 BPA:121:131	Program address bits for the B presence stack	Sheets 6, 7
BPE0	B presence stack counter load enable	5N8
BRF091:211	Segment relocation field bits - active outputs of stack buffer register	Sheet 8
BWE0	B presence stack write enable	5M5

MNEMONIC	MEANING	SCHEMATIC LOCATION
CAGDIR0	Calculate address gated decoded instruction read	14F2
CAMA0	Calculate memory address signal from CPU-D during calculate address that controls the output of the PA multiplexor - during RX2, LOC is added to the MDR. During RX3, when CAMA0 is low, the MAR (first) level of index is added to the MDR.	14B2
CLK1	Buffered output of CLK1C, system clock - this clock is to synchronize the CPU-C logic to the rest of the processor.	5N3
CLK1C	The CPU-C net of system clock generated on the CPU-D	3G4
CLRA0	Clear auxiliary register	11N2
CLSTA0	Clear MAT status (fault) register	11N4
CWR0	Change write to a read memory operation - this signal is generated after any memory fault (MAT, MPE, or ALGN) and prevents any further access until error recovery starts.	11N5
DCLK1	Destination clock - DCLK1 allows a selected destination on the CPU-C to be loaded; similar to CLK1, except no clock is generated during DSTOP.	3H7
DENCLK0	Decoded enable clock	15D8
DEXB0	Decoded exchange byte - RD decoding of exchange byte supplied by the CPU-A	19K6
DEXT0	Decoded sign extension - RD decoding of MDR sign extend; if not inhibited by the calculate address sequence, the state of MDR16 is propagated through to MDR00.	22F8
DIR	Decoded instruction read - RD decoding of instruction read used to control PA multiplexors (when low selects the LOC contents) and loading of the MDR during calculate address	4H6
DIRT0	Dirty bit - tri-state output of stack buffer register	8B3

MNEMONIC	MEANING	SCHEMATIC LOCATION
DISA1	Disable A byte - enables loading of MDR bits 8:15. This signal is also used to inhibit loading the most significant byte of the least significant MDR halfword.	19R6
DISB1	Disable B byte - enables loading of MDR bits 0:7. This signal is also used to inhibit loading the most significant byte of the MDR most significant halfword.	19R6
DISEXTO	Disable MDR sign extension - signal from CPU-D during calculate address to inhibit RD implied MDR sign extend	22G8
DISSTK1	Disable stack	9R5
DRD1	Decoded data read - RD decoded memory data read (memory data read, not instruction read). This signal is used to help define when to clear a fault.	15B8
DSTOPO	Destination stop - this is used to control whether to allow a clock to occur and thereby load a selected destination.	3H4
DUAO	Data unavailable - line from memory	9J3
EAL	Error of access level	9G8
EEDCLKO	Even EDMA memory data register clock - signal from the CPU-D that, on the positive transition, loads the data from either the local memory or from the EDMA.	11M1
EIMARO	Enable interrupt MAR - this signal, when low, indicates that a memory fault has occurred and that the fault address may be read. The output enable of the normal MAR is disabled and the ZMAR is enabled. Reading the fault address resets the EIMAR flip-flop allowing the MAR to be read.	15E4
EMAT291:311	MAT code fault bits	11M6,11M8, 11M9
ENMAAC	Enable MAT LMA drivers - also indicates MAT access to memory	9G5
ENPARC	Enable MAT relocated LMA drivers - when inactive on a PMEM, it indicates a MAT access of memory	9G4

MNEMONIC	MEANING	SCHEMATIC LOCATION
EP241	Execute protect bit 24 - this bit, when active, indicates that the current memory segment selected causes a MAC interrupt if used for program execution.	4N5
EPSTD1	Error - process segment size	3B9
ESLF1	Error of segment limit field	9L7
ESSTD0	Error - shared segment size	4C9
EXB0	Exchange byte - when low, an exchange byte occurs on the least significant halfword on the B bus (bits 16:31).	19R7
FAINCR1	A presence stack increment flip-flop	5N2
FBINCR1	B presence stack increment flip-flop	5N7
FDIRT0	Dirty bit of stack buffer register	8A3
FDUA0	Data unavailable from memory flip-flop	9L2
FFMATCY	Auxiliary MAT memory cycle flip-flop	9M3
FMATCY	MAT memory cycle flip-flop	9K3
FNCE0	Flop output of noncorrectable error - signal is generated on the CPU-D. It is an indication that a double-bit error has occurred.	6B8
FPA081:151	Program address register bits - stores 8 bits of PA on a memory fault	Sheet 15
FPACLK1	Clock for FPA register	15J5
FPRES1	Presence bit of stack buffer register	8A3
FSCLK	Skewed SCLK flip-flop	9A4
GDIR0	Gated decoded instruction read - controls steering of PA multiplexor during calculate address	3N9
GETSSTE0	Get shared segment table entry	9N6
GEXT1	Gated MDR sign extension - when active, causes the state of MDR16 to be propagated to MDR00	22F7

MNEMONIC	MEANING	SCHEMATIC LOCATION
HALTO	Halt processor - DMA request queued or memory is busy	9G2
ILOCO	Increment location counter - generated on CPU-D during calculate address	2N6
IMAR	Increment MAR	2L1
JAMDIRTO	Jam dirty bit into stack buffer register	19E6
JAMSHRD1	Jam shared bit into stack buffer register	19E6
L01:11	Access level bits	8D3, 8E3
LHWRTO	Local halfword memory write - used to gate least significant halfword to local memory for halfword memory write	21A8
LLOCO	Load location counter - RD decoding specifying the location counter as a destination	23C8
LMA08O:310	Memory address data line - this is the physical address presented to memory.	Sheet 25
LMARO	Load memory address register - RD decoding of MAR as a destination register	23C7
LMDRO	Load memory data register - RD decoding of MDR as a destination register	23C7
LOCO81:301	Location counter output lines	Sheet 2
LPSTDO	Load process segment table descriptor	3L1
LPSTDCKO	Load process segment table descriptor clock	3M1
LSSTDO	Load shared segment table descriptor	4L5
LWRTO	Local memory write enable - gates the selected inputs of the 2:1 multiplexor onto the MDS bus	21A1
MARO81:311	Memory address register data output lines	Sheet 2

MNEMONIC	MEANING	SCHEMATIC LOCATION
MARSTP0	MAR stop - generated on CPU-D during calculate address of RX squared (RXRX) format. This signal allows the MAR to be loaded with DSTOP active.	2A1
MAT0	MAT interrupt	11N4
MATEN1	MAT enable	9D2
MATRSD0	MAT read and set dirty bit	19E8
MATRSR0	MAT read and set reference bit	9J5
MATSTCP0	MAT stop	5K3
MCLK1	System clock gated by memory stop (MSTOP)	5L1
MDHLK0	Memory data register high clock - data on the inputs of MDR bits 00:15 are latched on the positive transition of clock.	17R1
MDHSA1	Memory data register multiplexor steering signal - select data input to MDR bits 00:15	17M1
MDLCK0	Memory data register low clock - data on the inputs of memory data register bits 16:31 are latched on the positive transition of clock.	18R1
MDLSA1	Memory data register low multiplexor select line - selects the type of data input to the memory data register bits 16:31	15B1
MDR000:311	Memory data register data output lines	Sheets 17,18,19
MDRΣ0	Memory data register sum output select	23B2
MDS000:310	Memory data system bidirectional data lines - data either to be written to or read from local memory	Sheet 16
MDSB0	Memory data register multiplexor select generated by CPU-D - selects type of data to be loaded into the MDR	18D1
MEMSA0 MEMSB0	B bus multiplexor enable for CPU-C source registers	22G2 22G3

MNEMONIC	MEANING	SCHEMATIC LOCATION
MFAULTO	Memory fault - indicates that a memory fault has been queued because of a non-correctable errcr, MAT interrupt, or alignment fault	15A6
MPA081:111	MAT program address bits	Sheet 13
MSBCO	MAT to shared buffer controller	13F4
MSELB1	B bus multiplexcr select line	23B2
MSTOPO	Memory stop - used to inhibit system clocks while the memory system is busy or data is unavailable	3G4
PA081:311	Program address multiplexor outputs - the outputs reflect the contents of the location counter during calculate address or the contents of the MAR at any other time.	Sheets 6, 7 and 14
PMEM1	Processor memory operation request	9G2
PRES1	Presence bit - tri-state output of stack buffer register	8B3
PSBCO	Processor to shared buffer controller	13F2
PSEL1	Processor selected - generated by the CPU-D when memory address and data are relevant to a processor as opposed to an EDMA memory cycle	9A3
PSW10 PSW11	Program status word bits indicating access level of the processor	9A8, 9A7.
PSW211	Program status word bit 21 - this is the relocation/protection bit of the PSW that enables the MAC.	9A2
RD00:03	Memory control field of microinstruction	Sheet 4
RD150	ROM data register bit of the microinstruction word - the RD bits control all processor level functions. They do not control EDMA or memory refresh.	23A5
RD240	ROM data register bit of the microinstruction word - the RD bits control all processor level functions. They do not control EDMA or memory refresh.	22B2

MNEMONIC	MEANING	SCHEMATIC LOCATION
RD001:041	ROM data register bits of the microinstruction word - the RD bits control all processor level functions.	3A6,3A1, 3A7,16B2
RD261	ROM data bit 26	23B2
RD051	ROM data register bits of the microinstruction word - the RD bits control all processor level functions. They do not control EDMA or memory refresh.	16B2
RD121:141	ROM data register bits of the microinstruction word - the RD bits control all processor level functions. They do not control EDMA or memory refresh.	23A6, 23A7
RD161	ROM data register bits of the microinstruction word - the RD bits control all processor level functions. They do nct control EDMA or memory refresh.	22B2
RD251:271	ROM data register bits of the microinstruction word - the RD bits control all processor level functions. They do not control EDMA or memory refresh.	22B1, 23B1
RD271A	ROM data register bits of the microinstruction word - the RD bits control all processor level functions. They do not control EDMA or memory refresh.	23B1
READ1	Read but not read and set	11D7
RFAULTO	Reset fault - used to clear memory fault conditions	11N3
RPA081:111	Relocated program address bits	Sheet 13
S001:311	S bus data output from the CPU-B	Sheet 13
SCLR0C	Systems clear CPU-C net	3L4
SHCLK0	Shared clock	9N3
SCLK1	Skewed CLK1 clock	3H5
SHARED	Shared bit of stack	8B9
SLF01:41	Segment limit field bits	8E3, 8G3
SPA081:151	Program address bits	Sheet 16

MNEMONIC	MEANING	SCHEMATIC LOCATION
SRF091:201	Segment relocation field bits - tri-state outputs of stack buffer register	Sheet 8
STD151:311	Address field of segment descriptors	Sheets 3, 4,10
SUM081:311	Cutputs of adder used during calculate address to resolve effective address of RX2 and RX3 formats. The contents of MDR and LOC (RX2) or the MDR and MAR (RX3) are added together. The resulting data is available on the B bus as the MDR data.	Sheet 20
ULOC0	Unload location counter - RD decoding of location counter as the B bus source register	22F1
UMAR	Unload memory address register - RD decoding of the MAR as the B bus source register	22H2
UMDR0	Unload memory data register - RD decoding of MDR as the source register	22G2
WSTK0	Write into segment table register stacks	9N3
XRPA	Pull-up terminations for unused inputs to provide noise immunity	3K1
XRPB	Pull-up terminations for unused inputs to provide noise immunity	3E1
XRPC	Pull-up terminations for unused inputs to provide noise immunity	5M8
XRPD	Pull-up terminations for unused inputs to provide noise immunity	6D8
XRPF	Pull-up terminations for unused inputs to provide noise immunity	7A1
XRPG	Pull-up terminations for unused inputs to provide noise immunity	14L9
ZMAR081:311	Output of a 2:1 MUX-ZMAR is the contents of the FPA register on an MFAULT0; otherwise, it is the contents of MAR.	Sheet 15

CHAPTER 12
CPU-D BOARD

12.1 INTRODUCTION

The CPU-D Board, part number 35-770, contains the processor clock control, processor-to-memory logic, and memory control. It also has the extended direct memory access (EDMA) protocol control, EDMA transceivers, EDMA-to-memory contention and mode logic, EDMA address and data registers, and the memory bus logic. In addition, the board includes the user's instruction and auxiliary instruction registers, instruction ROM format, calculate address logic, source, destination, and E field decoders, the repeat counter, input-output control, S bus buffers, and B bus multiplexors.

12.2 PROCESSOR AND MEMORY TIMING SIGNALS

Processor timing signals are derived from a 2-stage Johnson counter (Sheet 9) whose sequence is modified by the skip logic when memory is accessed. The two J-K flip-flops of the counter and the two D flip-flops of the skip logic are initialized by A System Clear (ACLR0) on power up/down. OSC0, a 20 MHz square-wave, is the buffered output of a crystal oscillator and the toggle input for these flip-flops. Clock (CLK) and Skew Clock (SCLK) are each a buffered output of the Johnson counter. A1B1 is a decoded state of the counter.

When memory is not being accessed, the J input of FA is a function of the state of the FB flip-flop, and CLK and SCLK are square-waves of a 200 ns period (refer to Figure 12-1). A1B1 is active for 50 ns.

When memory is accessed, the processor timing is modified by the skip logic to accommodate the memory cycle. Figure 12-2 shows the waveforms of a processor-to-memory operation.

A memory cycle is started when the processor activates an Early Read Line (LER0 or SER0, Sheet 4). In response, the memory enables and then disables the Data Unavailable line (DUA0). DUA0 must be brought low before the trailing edge of CLK1, and when DUA0 is brought high by the memory, it must do so again before the trailing edge of CLK1. In addition, on the first falling edge of CLK1 after ER0, memory enables the Memory Busy line (LMBSY0 or SMBSY0) if memory has not completed its cycle at that time. The basic memory cycle is 500 ns.

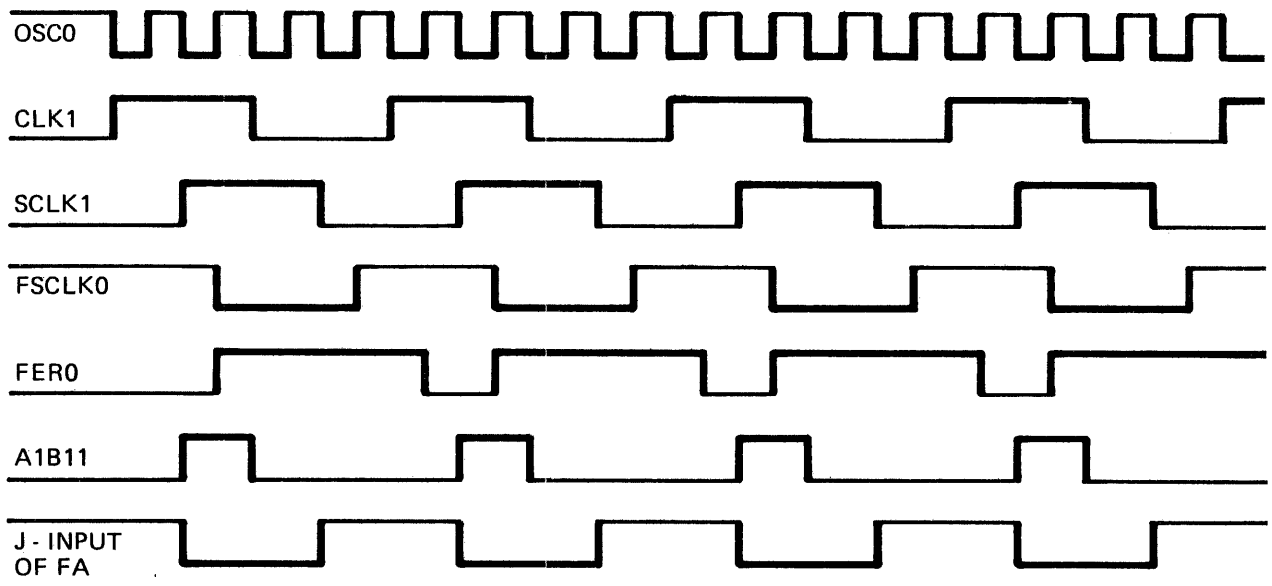


Figure 12-1 Processor Timing - No Memory Access

All memory, whether local or shared, has the same address and data bus. Local ERO (LERO) and Shared ERO (SERO) determine which memory is to be accessed.

A processor-to-memory operation (PMEM1) is decoded on Sheet 4 after the falling edge of CLK1. If no EDMA memory access is pending and the memory is not busy (HALTO high), the J-input of FA is now also controlled by FERO. An inactive FERO and HALTO and a decoded PMEM1 inhibits the Johnson counter from changing state for an interval of 50 ns - the period of the crystal oscillator. FER1 enables the LERO line (assume shared memory does not exist) nominally 25 ns before the rising edge of CLK1. The memory now enables DUAO. DUAO remains low until after the trailing edge of CLK1. On this edge, FDUA and FDUSKP are toggled set (Sheet 4) and the memory asserts the LMBSYO line which brings HALTO down. With FDUSKP set, FERO again controls the J-input of FA and causes the Johnson counter to remain in the reset state for an additional 50 ns. Before the trailing edge of CLK1, the memory removes DUAO, and FDUA and FDUSKP toggle reset on this edge. If DUAO is not removed, FDUA remains set but FDUSKP toggles reset and further skips are prevented for this memory cycle.

Normally, LMBSYO is removed on the CLK1 falling edge following the removal of DUAO. Memory can maintain LMBYSO active if it is not ready to accept another memory access in the following clock cycle or whenever it must perform a refresh operation. For refresh, no skips are performed.

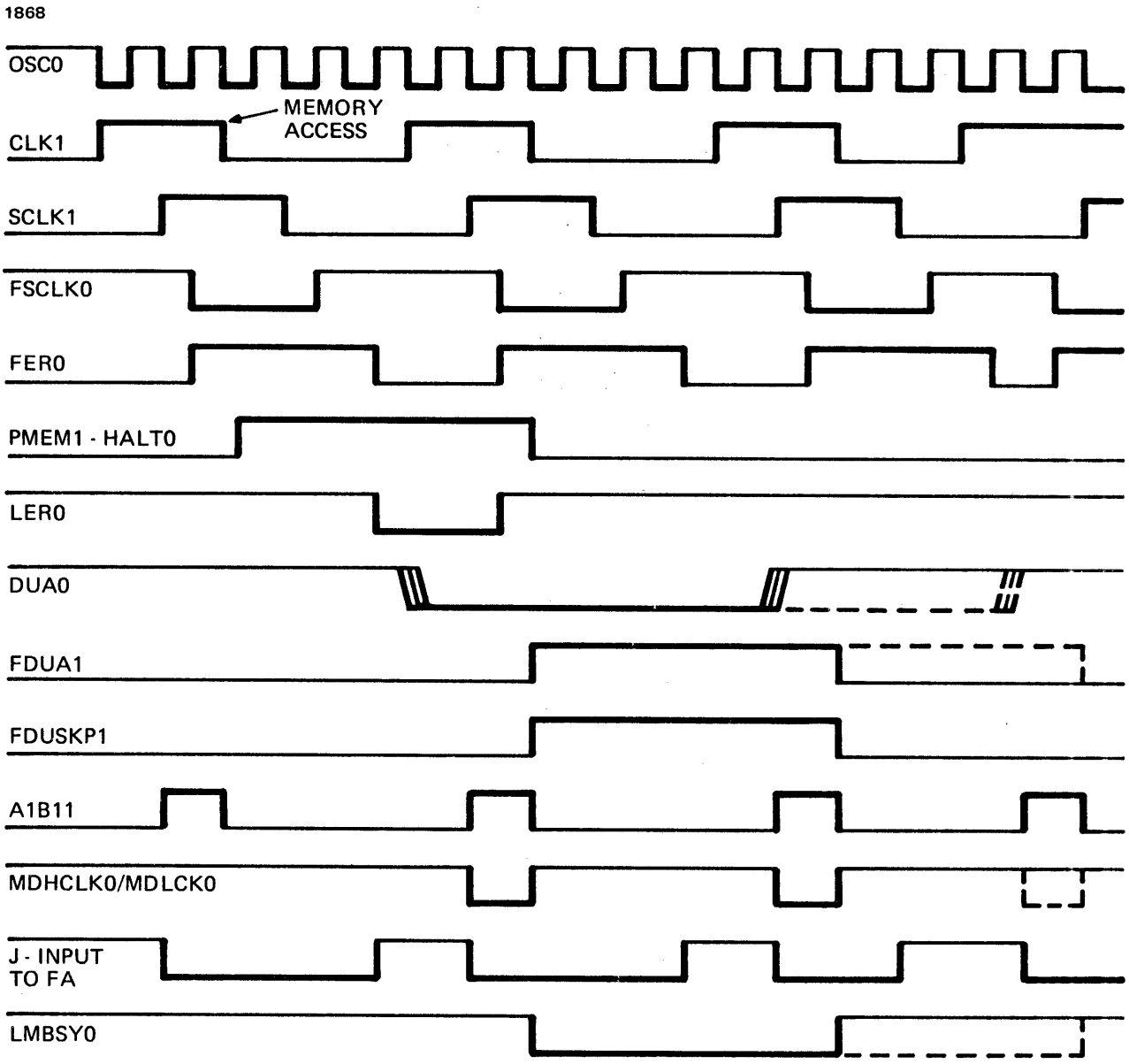


Figure 12-2 Processor Timing - Processor-To-Memory Access

12.3 PROCESSOR MEMORY OPERATICN DECODE

Processor-to-memory operations are decoded from the memory control field of the microinstruction, RD00:03. Table 12-1 lists the operations specified by these bits.

TABLE 12-1 RD BIT OPERATIONS

RD BIT				OPERATION
00	01	02	03	
0	0	0	0	Nc Action
0	0	0	1	DW1 - Data Write Byte
0	0	1	0	PW2 - Privileged Write Halfword
0	0	1	1	DW2 - Data Write Halfword
0	1	0	0	TFL - Data Write Byte, No ECC
0	1	0	1	ENACLK - Enable Destination Clocks
0	1	1	0	PW4 - Privileged Write Fullword
0	1	1	1	DW4 - Data Write Fullword
1	0	0	0	Undefined
1	0	0	1	RAS - Read and Set
1	0	1	0	PR2 - Privileged Read Halfword
1	0	1	1	DR2 - Data Read Halfword
1	1	0	0	REL - Read Error Logger
1	1	0	1	IR - Instruction Read
1	1	1	0	PR4 - Privileged Read Fullword
1	1	1	1	DR4 - Data Read Fullword

Microinstructions are clocked on the trailing edge of CLK.

Decoded Memory (DMEM) is generated from RD00:03 on Sheet 4. Processor-to-Memory (PMEM) is asserted by DMEM0, a gated decoded instruction read (GGDR0), second part of instruction read (2IR0), gated second instruction read (GSIR0) or calculate memory address read halfword (CMR20).

Memory operations are more finely resolved on Sheet 6 where the result of the decoding is latched in a pair of quad-D registers. On power up/down, the registers are initialized reset by D System Clear (DCLR0). Latching is done on the leading edge of CLK1E and the clocking is inhibited if Processor Data Unavailable (PDUA0) is active. PDUA0 is always enabled/disabled on the trailing edge of CLK.

The quad registers store the following information about the memory access: Both Instruction Read (FBIR), Odd Instruction Read (FOIR), Even Instruction Read (FEIR), Read (FRD), Even Data (EVDAT), and fullword data. Instruction read accesses are contained in Set Calculate Address Part 1 (SCAP11), which is a function of GDIR0 and inhibited by ROM Stop (RSTOP0A). A Read operation is an active RD001 cr CWR0 - change write to a read. A write is the complement of the read, provided the Instruction Register flip-flop (FINR0) is reset. Fullword data is signaled when RD011 and RD021 are both active and halfword data is signaled when either of these bits is inactive. CMR20 and DMEM0 serve as a gate enabling function.

On instruction reads and halfword data operations, program address bit 30 (PAR30) indicates whether or not the instruction to be fetched or the halfword data operation is on a fullword address boundary. If the instruction lies on a fullword boundary, FBIR is toggled set and a fullword is accessed. The first 16 bits of the readout are loaded in the instruction register and the second 16 bits are loaded in both halves of the Memory Data Register (MDR). If the instruction resides on an odd boundary (PAR 301 active), FOIR is toggled set, the halfword is accessed, and the second Instruction Read flip-flop (FSIR) is set on the trailing edge of MCLK0. The accessed 16 bits are stored in the instruction register and, if the instruction is not of a short-format (RR0 inactive), GSIR0 is generated and FEIR is toggled set on the next available CLK1E. The even halfword is accessed and loaded into both halves of the MDR. If the instruction fetched from the odd halfword is a short (16-bit) format (RR0), FEIR and GSIR0 are not enabled and memory is not accessed.

On a halfword data operation that is to be executed on a fullword address boundary, EVDAT gets set. For a halfword read, memory bus data bits 00:15 are loaded into 16:31 of the MDR, and for a halfword write, bits 16:31 of the MDR are asserted on memory data lines 00:15.

Outputs of the quad-D registers and their logical combinations generate Fullword (FW) and Read Fullword (RDFW). Gated Read (GRD) is generated from FRD when PDUA1 is active or HALT0 is high.

12.4 LOCAL/SHARED MEMORY

Local and shared memory are accessed over the same memory address and data buses. An access is initiated by activating an ER0 line. Each memory has a dedicated ER0 line - Local ER0 (LER0) and Shared ER0 (SER0), Sheet 4. In addition, each memory has a dedicated busy line - Local Memory Busy (LMBSY0) and Shared Memory Busy (SMBSY0) controlled by the respective memory. The Data Unavailable (DUA0) line is common to both.

LER0 and SER0 (Sheet 4) can be activated by the processor, the Memory Address Translator (MAT), or by an EDMA device.

12.5 PROCESSOR-TO-MEMORY

Figure 12-2 shows waveforms for a processor-to-memory operation. All processor accesses are to local memory unless Processor to Shared Bank Controller (PSBC0), Sheet 4, is active. On a processor-to-memory operation (PMMEM1), if an EDMA bus operation is not pending (HALT0 high), the Enable MAT Access (ENMAA0), PSBC0, and LMBSY0A lines are inactive, and LER0 is pulsed low by FER1 if the Change Write to Read line (CWR0) is high. If PSBC0 is active, SER0 is gated low by FER1. In either case, if CWR0 is low, no FR0 can be sent.

If the processor must perform a MAT access of memory, ENMAA0 active inhibits the CPU path to the ER0 lines and enables the MAT path. Here again, PSBC0 determines whether LER0 or SER0 is to be gated.

Before an ER0 line is pulsed, the processor has output the memory address and, in the case of a write into memory operation, the memory data. On a write to memory, DAWT1 has been decoded and the write line (WRT0) enabled. In addition, Load Write (LWRT0), Sheet 7, outputs the memory data bits of the MDR to their respective MDS lines. For an even data halfword write (EDAT1), Load Halfword Write (LHWRT0) steers MDR bits 16:31 to MDS00:15.

For a processor read from memory, MDSB0, MDHSA1, and MDLSA1 (Sheet 7) steer the readout into the appropriate half or halves of the MDR. Memory Data Register Low Clock and High Clock, (MDLCK0 and MDHCLK0) toggle the MDR halves as a function of A1B11. MDR is loaded on the rising edge of MDLCK0 and MDHCLK0. MDHCLK0 pulses low for an RDFW, FBIR, or FEIR, and MDLCK0 during an FEIR or GRD. Note that the MDR clocks are present until FDUA is reset. When FDUA resets, the memory operation decode register changes state and disables the MDR toggles.

Periodically, the memory requires time to perform a refresh which is under the control of the memory logic. The memory cycle-steals a refresh cycle by asserting its memory busy line. As long as a busy line is active, no access to memory is attempted.

12.6 PROTOCOL LOGIC TO ACQUIRE THE EDMA BUS

Bus occupancy on the EDMA is controlled by the EDMA Protocol Logic. Figure 12-3 shows the signals and nominal timing generated by the logic in response to a request for bus occupancy. The Extended Request (XREQ0) line, common to all devices on the EDMA, is activated by a device that wants to use the bus. An active XREQ0 results in a QUE0 which queues and synchronizes the requesting EDMA device to the protocol timing. Transmit Priority Chain (TPC0) is then sent. TPC0 is connected to each device in a daisy chain fashion. A device that has not been queued sends TPC0 to the next device on the bus. A queued device does not transmit TPC0. The EDMA device that has captured TPC0 now must activate the Local Memory Request line (LMREQ0) if

it desires access to local memory; otherwise, the access will be interpreted as that for shared memory. The device that has captured TPC0 is granted the EDMA only when the Start of Transmission (SOT) signal is received from the protocol logic. When the device is finished with the bus, it signals the protocol logic by sending an End of Transmission (EOT) signal, not shown in Figure 12-3.

The protocol logic is found on Sheet 6. It is separated into two parts:

1. Three flip-flops (two D and one J-K) toggled by an LC oscillator, and

2. A quad-D register connected as a ring counter that is toggled by a separate L-C oscillator.

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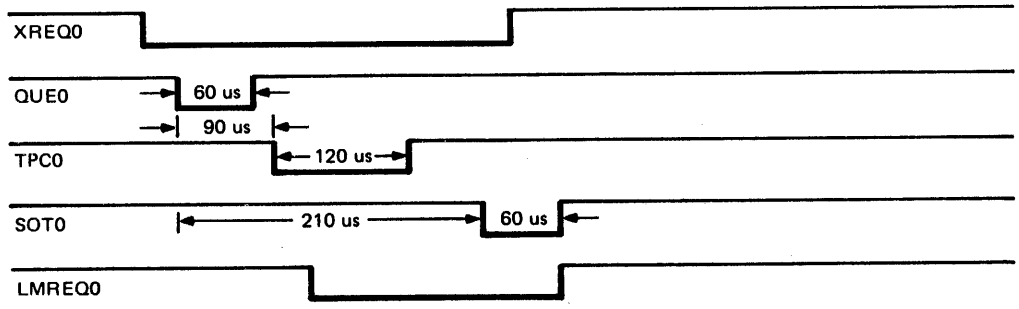


Figure 12-3 EDMA Protocol

Each oscillator is adjusted for a nominal 60 ns period. Figure 12-4 contains the waveforms for the protocol logic.

On power up/down, the C net of System Clear (CCLR0) inhibits the upper oscillator and forces the two D flip-flops clear. System Clear (SCLR1) (Sheet 8) forces FPC reset through Reset C (RESC0). This initialized state inhibits the lower oscillator and holds the quad-D register cleared. In the idle state, the clock inputs to all registers are low.

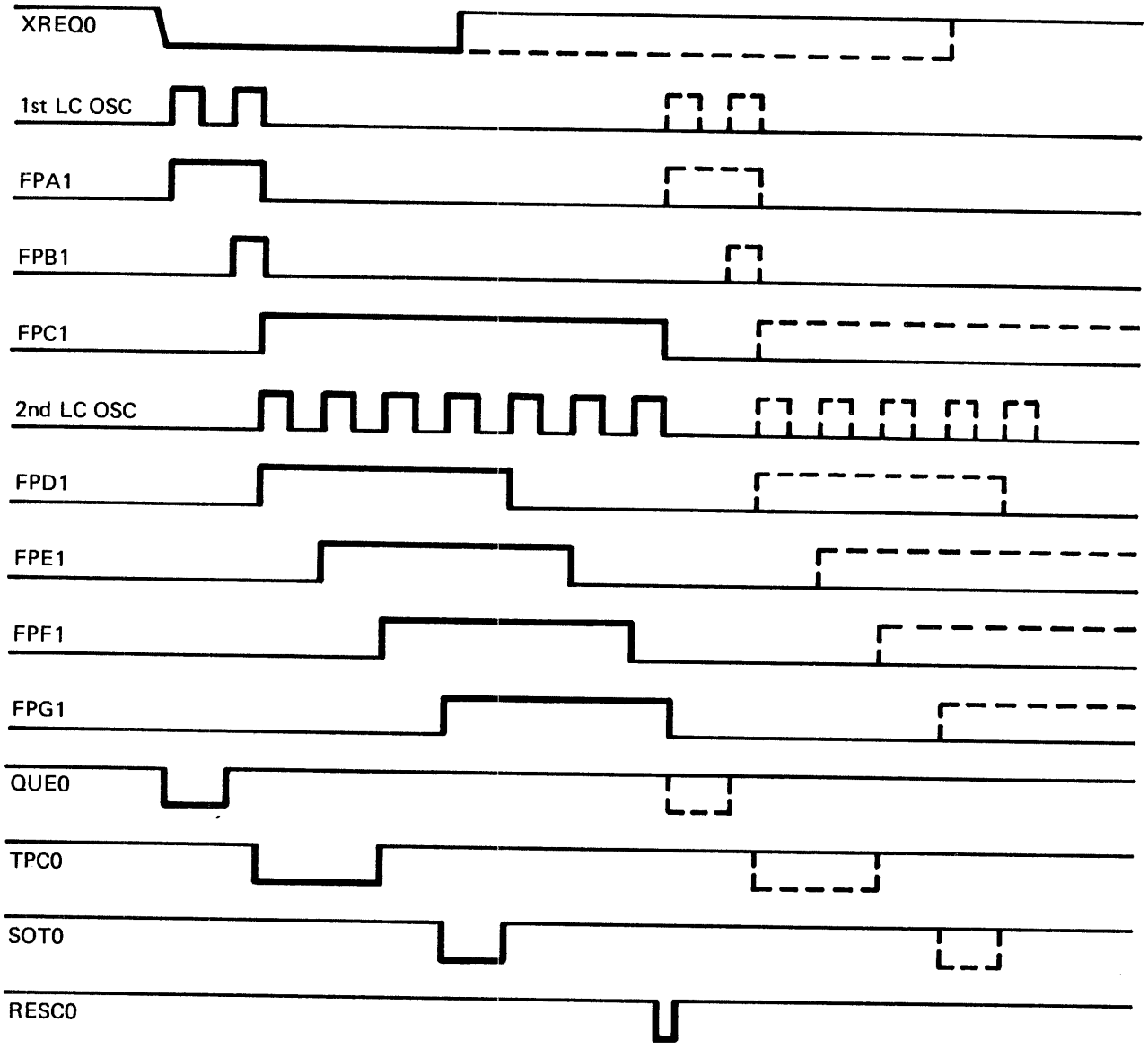


Figure 12-4 EDMA Protocol Logic Waveforms

On XREQ0, the forced clear is removed from the D flip-flops, and the upper oscillator is enabled. On the first rising edge of the buffered output of the oscillator, QUE0 is enabled and terminated on the next rising edge and the enabling of the lower oscillator starts. The next falling edge sets FPC which gates TPC0. FPC0 disables the upper oscillator, forcing the D flip-flops reset and removes the low from the clear inputs of the quad-D register. This register also changes state on the rising edge of the buffered oscillator output. TPC0 is disabled when FPF is set. SOT0 is gated when FPG is set and terminated by the cleared state of FPH.

The protocol logic returns to the idle state when RESC0 goes active. RESC0 (Sheet 8) is pulsed low by the protocol oscillator (PROSC1) during the interval when FPG is set and FPD reset. A reset FPC disables the lower oscillator, holds the quad-Ds cleared, and allows another protocol sequence to start if XREQ0 is active.

The width of TPC0 is increased if an EOT has not been received in response to the previous SOT0 to clear FEOT (Sheet 8). Hold Start (HOST1) inhibits the transmission of SOT0 (Sheet 8) if a burst mode to local memory is being executed; or if an EDMA device is waiting for an answer from memory [(FLADR+FLADRA)•FERD+DMASEL•FERD+ENACSC].

Test points are available for maintenance and factory use.

P5 pull-up resistor = TPH, TPC, TPE, and TPF
GRD = TPD

NOTE

TPC and TPD are normally strapped.

12.7 EDMA BUS TRANSMISSIONS

When the selected device has received an SOT0, it must output an address and a memory control field followed by a Load (LOAD0) pulse. If the access is a read from memory, LOAD0 is accompanied by an End of Transmission (EOT). If the access is a write, EOT is not sent with the address LOAD0; rather, after the address, the device outputs a halfword of data followed by a LOAD0. On a halfword write, an EOT is sent with this LOAD0. However, on a fullword write, an EOT is not transmitted until the device outputs the second halfword, and then outputs a LOAD0 with EOT. (Refer to Figure 12-5).

When a memory outputs a halfword readout, it also sends two bits to identify the responding memory, a parity error bit, and a memory malfunction bit. This is followed by an Answer (ANS0) pulse. On a fullword read, another halfword is sent, also followed by an ANS0.

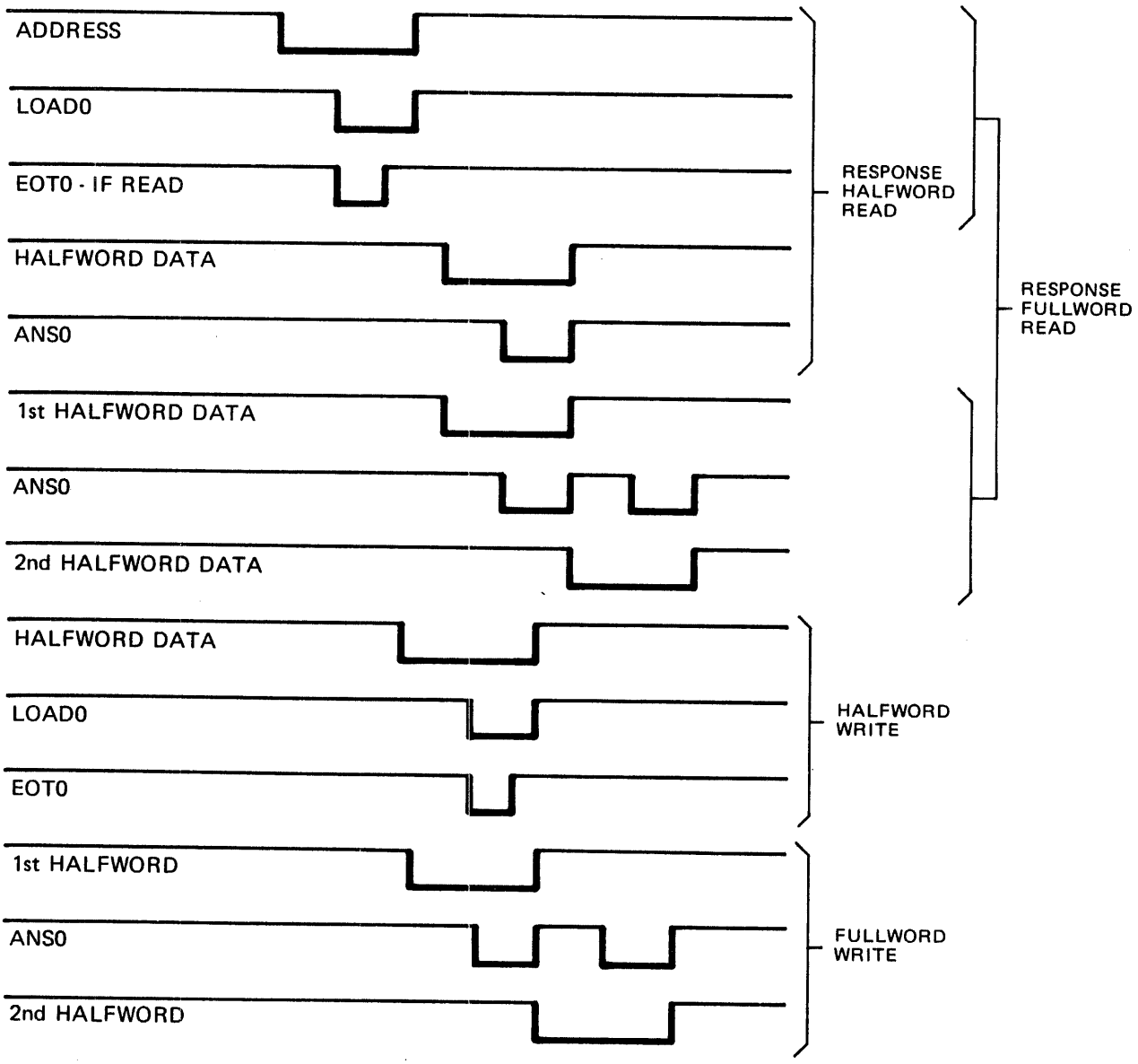


Figure 12-5 EDMA to Memory

12.8 EDMA TO MEMORY

An EDMA request to memory is indicated by XREQ0 (Sheet 2) which is activated by the EDMA device (refer to Figure 12-6) and directly sets FMREQ. The state of FMREQ is synchronized by the edges of A1B11 (Sheet 2) and the double-ranked quad-D registers to the processor timing. On synchronization, HALT is generated to prevent the processor from accessing local memory on the next available memory cycle. When the device is granted the EDMA bus via SCT0, FSCT is set and generates LDMAL0 (Load EDMA MAR) (Sheet 7) and enables the ILDMA0 (Increment or Load MAR) gate. FSCT also enables the D input of FLADR (Load EDMA Address Register) (Sheet 2).

The EDMA transceivers, memory address register (EDMAR), the data register (EDMA MDR), LMA bus drives, and the data bus logic are found on Sheets 15-18.

FLADR sets on the leading edge of LCAD0. ILDMA0 goes high to load the memory address; HOST1 goes active; and the memory control field (DMA15:17) is loaded into the D registers (Sheet 5). In addition, the state of FLADR is synchronized to the processor timing. If the stored DMA15:17 bits indicate a read from memory (FERD1), the trailing edge of SCLK1 enables DMASEL if memory is not busy. The decision to select DMA to local memory (DMALM1) or DMA to shared memory is determined by the FLMRQ0 state which was set by SCT0. A low FLMRQ0 is an EDMA to local memory and a high to shared memory. However, if a read of memory is not indicated (FERD0), EEDCLK0 (Even EDMA Data Clock) is low (FLADRA0 inactive), and/or if a halfword write is to be performed (FEFW0 and DL301D), OEDCLK0 (Odd EDMA Data Clock) is low (Sheet 7). The leading edge of the LOAD0 for the first halfword of data sets FLDARA (Load EDMA Data A) and the data loaded into the EDMA MDR and FLDARA0 keeps HOST1 active. The state of FLDARA is also synchronized to the processor clocks for a write halfword. On synchronization, DMASEL would be asserted on the trailing edge of SCLK1 if the memory is available.

If the EDMA request is neither a read nor write halfword, a fullword write is indicated (FEFW1). With EDMA Fullword Write (EFWRT1) active, OEDCLK0 is low. On the leading edge of the second data halfword LOAD0, FLDARB toggles set and OEDCLK0 clocks the data into the lower half of the EDMA MDR. The state of FLDARB is synchronized to the processor timing. On synchronization, DMASEL1 is asserted on the falling edge of SCLK1 if the memory is available.

When DMASEL1 goes active, the skip logic comes into play to modify the processor timing as described in Section 12.2. DMASEL1 and DMBZY1 (the latter on Sheet 2) perform the first skip; FDUSKP1 and FERO perform the second skip.

For a write operation, DMASEL1 and FERD0 enable WRT0 to memory (Sheet 4) and DMAWRT0 (Sheet 7) to output the EDMA MDR to the memory data bus (Sheet 7). An EDMA halfword operation to memory is signaled by DMAHW0 (Sheet 5).

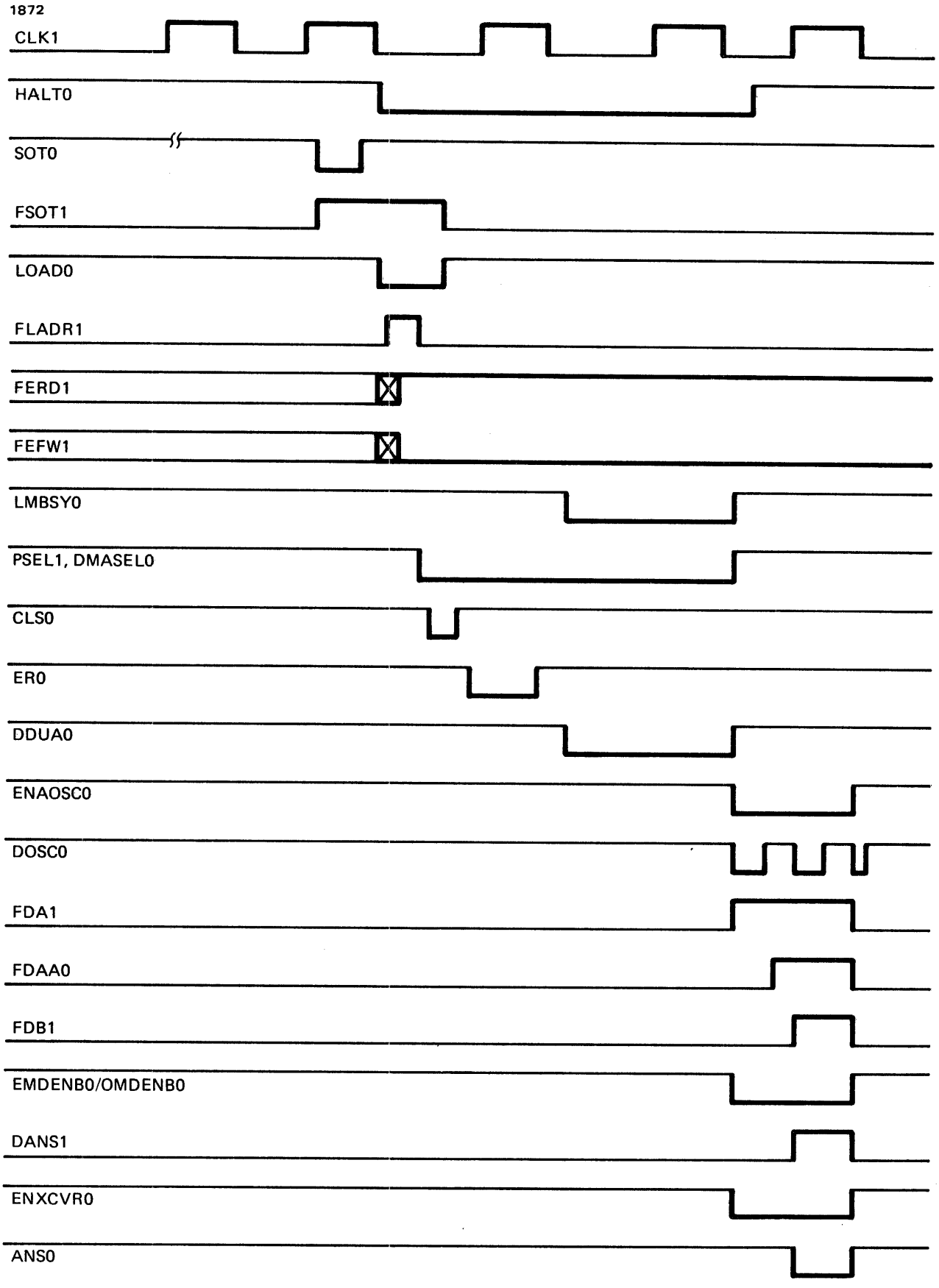


Figure 12-6 EDMA to Memory - Halfword Read

For a read operation, FERD1 and FERDOA (Sheets 17 and 18) steer the MDS. This data register is loaded on the trailing edge of CLK1D during DDUA1 (DMA Data Unavailable) via EEDCLKO and OEDCLKO (Sheet 7) lines to the EDMA MDR input.

CLSO is asserted immediately after DMASEL1 goes high by DMBZY1, FBO, and FSCLK1 (Sheet 2). CISO directly clears FMREQ, FSOT, and the LMRQO latch. This signal also gates CLADO (Clear Address and Data flip-flops) (Sheet 7) tc clear FLADR, FLDARA and FLDARB if a Burst Read (BRTRDO) is not being processed.

On an EDMA read, the memory to EDMA control logic (Sheet 5) (Figures 12-6 and 12-7) will transmit the readout to the EDMA device. The output of the 5-input NOR gate is normally low. It goes high for an EDMA read (FERD1) but not a burst mode (BRST1) during an active DDUAO. At this time (CLK1), the J-K flip-flop sets to generate ENOSCO (enable oscillator). The set state also removes the low clear on the 3-stage Johnson counter. ENAOSCO starts DOSCO (DMA Oscillator) (Sheet 3) and enables the transceiver via ENLANDO for ANSO. The state of the Johnson counter and the steering logic on Sheet 8 generate EMDENDBO (Even Data Enable), OMDENBO (Odd Data Enable), and DANS1 (DMA Answer). DANS1 drives the ANSO line of the transceiver. The transceivers that transmit the answer to the EDMA are enabled by ENXCVRO.

1688-1

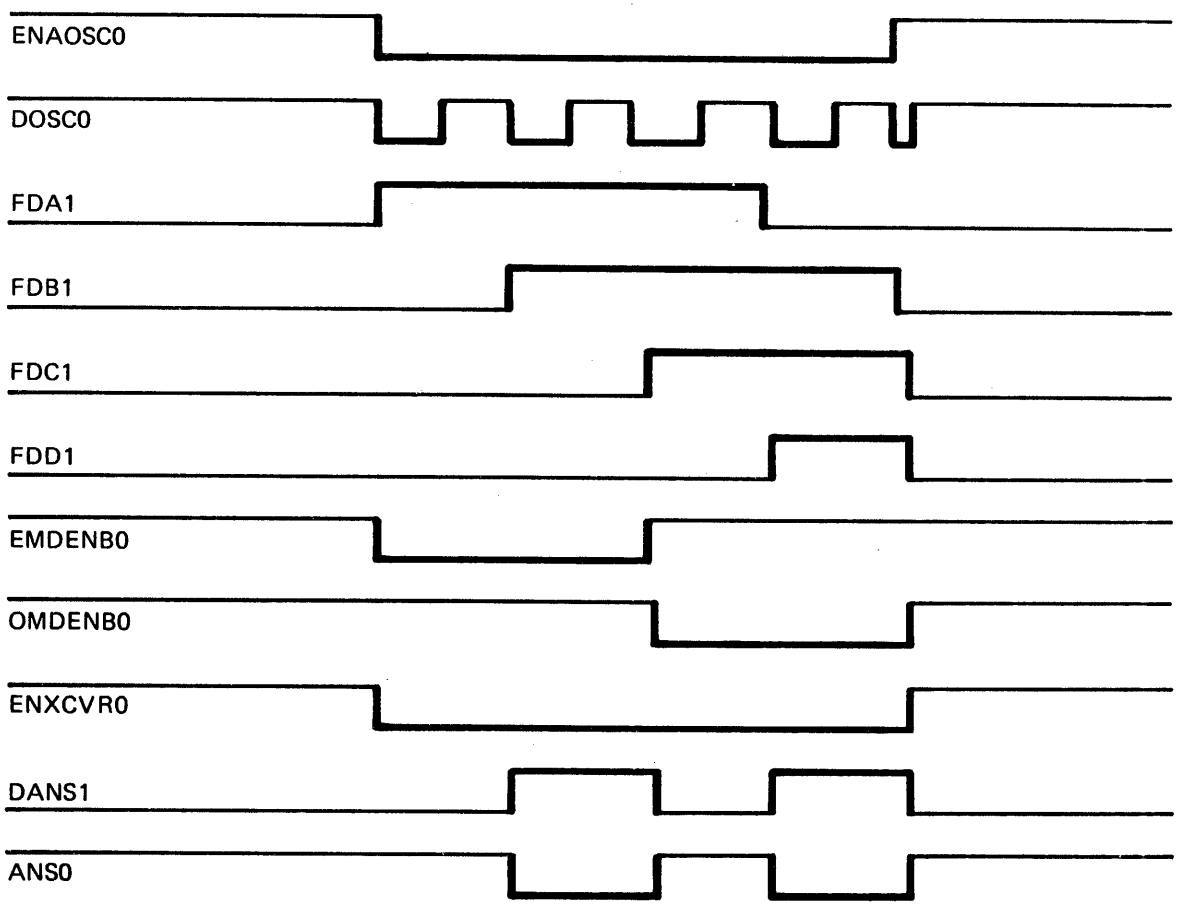


Figure 12-7 LM to EDMA Answer - Fullword Read

For a fullword read, EMDENBO is activated when FDA sets and DANS1 is activated by FDB1. These signals terminate when FDC sets; this enables OMDENBO. DANS1 is again enabled when FDA resets. Both OMDENBO and DANS1 are disabled when FDB clears.

For a halfword read from an even memory address boundary, EMDENBO outputs the data to the EDMA device. On a halfword read from an odd boundary, OMDENBO enables the data to the EDMA bus.

The oscillator is stopped by logic that examines the memory mode of operation and the state of the counter. For a halfword or fullword read, FNOSCO is driven high when the last ANSO pulse is disabled. The J-K flip-flop that disables ENOSCO clears the J-K that began the sequence. The reset state of this J-K initializes the counter and the last J-K is forced to the clear state.

A burst mode operation on the EDMA bus requires handshaking between the processor and the requesting device. This handshaking is performed over the LOADO and ANSO lines. The requesting device always sends LOADO and the processor sends ANSO.

In a burst read mode and in response to ANSO, the device transmits LOADO to the processor to indicate that the device is ready to receive another fullword. If the device requires no additional data, it then transmits EOT to signal the end of the burst read mode.

In a burst write mode, the processor transmits an ANSO to indicate that it can handle another fullword of data to store in memory. In response, the device transmits a fullword of data. With the last fullword to be written in memory, the device also sends EOT to signal the end of the burst write mode.

The first fullword write of a burst write operation begins as a normal EDMA fullword write to local memory. However, when ST1 pulses high because of CISO and BRWRT1 (the decode of the EDMA memory operation field) direct sets the J-K flip-flop to enable the oscillator (ENAOSCO), DOSCO toggles the Johnson counter and FDA1 gates DANS1 (Sheet 8) to output ANSO through the enabled transceiver. The device responds with two halfwords of data and two LOADOs. With BRWRTO and FEFW1 active, the LOADOs set FLDARA and FLDARB in turn and another EDMA to local memory request is synchronized to the processor timing. ENAOSCO is disabled after ANSO and the local memory to EDMA control logic is initialized reset. During the first fullword store of the burst write, DDUA1 and CLK1F toggle FBRWRT set. When the device transmits the last fullword of the burst write, it also sends EOT which, with BRWRT1, changes the memory control field from a burst write mode to a fullword write. The last fullword is then stored as a normal fullword write.

If a Burst Read (BRTRD) mode is decoded, CLADA0 is inhibited from being pulsed by ST1 (Sheet 7). As a result, FLDAR remains set, still synchronized to the processor timing. During the first fullword read of the burst read, DDUA1 and CLK1F toggle FBRTRD set. At the same time, ENAOSC0 is enabled to output the first fullword of data to the device. When FDA sets, CLADA0 is enabled to clear (FLADR) and disabled when FDAA sets. The fullword of data is transmitted to the device as for a normal EDMA fullword read. In response to ANS0, the device sends a LOAD0 to signal for another fullword read. If LOAD0 is not returned before the next memory cycle becomes available, due to the fact that FLADR resetting is delayed, FLADR1 is still stored in the quad-D register (Sheet 2). DMASEL remains active and the next fullword is read from memory. During this access, FDRDY gets set to indicate that valid data resides in the EDMA MDR. Whenever FLADR is toggled set by the handshaking LOAD0, ENAOSC0 is enabled by FBRTRD1oFLADR1oFDRDY1. On the last fullword transmission of a burst read, the device sends EOT which gets synchronized as FQEOT (Sheet 2) and changes the EDMA memory control field to a fullword read.

The EDMA memory address register is incremented (ILDMA0) during burst modes on the trailing edge of DDUA1 after FSOT is cleared (Sheet 7).

12.9 CLOCK STOPS

Clock stops are used to inhibit microprocessor clocks for an event requiring more than one clock period. There are three types of clock stops that suspend different levels of processor functions. Destination clock stops (DSTOP) inhibit the loading of data into a destination register. ROM clock stops (RSTOP) inhibit the loading of a new microword into the ROM data register and prevent the CSAR address from changing. Memory clock stops (MSTOP) stop all microprocessor functions. DSTOP and RSTOP are forced active by MSTOP. Refer to Sheet 9 of Functional Schematic 35-770D08 during the following breakdown of the signals causing DSTOP and RSTOP.

MFAULT0 — Memory fault causes DSTOP to inhibit the loading of destinations after a memory fault. This condition remains in effect until the memory fault is serviced.

BRANCH0 — Branch causes DSTOP to prevent the loading of random data into random registers.

OPTSTP0 — Option stop causes both DSTOP and RSTOP during operations with the High Performance Floating-Point Processor (HPFPP). Option stop remains active until the HPFPP operation is complete.

AFINRO	This signal causes DSTOP during the second half of the RX squared calculate address. This signal prevents the source string address contained in the shift register from being destroyed.
CMR2O	This signal causes DSTOP and RSTOP during the calculate address of the RX3 or RI2 formats.
IOSTOPO	I/O operation in process stop. Both DSTOP and RSTOP are made active until the I/O Sync is received.
2IRO	This signal is generated during the beginning of the second part of the RX squared format address calculation and causes DSTOP to save the shift register contents.
AMSTOPO/BMSTOPO	Memory contention signal that causes DSTOP and RSTOP during the period of contention.
RX2STPO	Stop generated during calculate address of an RX2 format instruction. This stop causes RSTOP and allows the location counter to be incremented to point to the next instruction.
RX3STPO	RX3 format calculate address stop that causes RSTOP to remain active.
CNTEOO	Counter not equal to zero. When the repeat counter is loaded, RSTOP remains active until the count is reduced to zero.
GMATSTOPO	This signal activates both DSTOP and RSTOP when the MAT needs to access memory.
COMSTPO	Communication stop asserts DSTOP and RSTOP for loading into the communication hardware assist board.
NOCNTO	Causes a DSTOP for one clock period if repeat counter is loaded with a zero value.

Memory Stop (MSTOP) occurs if a memory access is attempted by the processor (PMEM1) or the MAT (GENMAA1), and the desired memory is busy (LMBSY1/SMBSY1). MSTOP is also activated if the MDR is specified as a source (UMDR1) and a memory operation is in progress (PDUA1). In addition, the clock single-step control test feature causes FTIT1 as long as TRAPO remains active to control MSTOP. Depressing the advance pushbutton disables FTIT1 for one clock period. MSTOP also activates if the processor (PMEM1) is trying to activate a memory cycle but an EDMA port has won contention for the memory (HALT1).

12.10 INSTRUCTION REGISTER AND AUXILIARY INSTRUCTION REGISTER

The Instruction Register (IR) is a 16-bit register that is loaded with the user-level instruction to be emulated. The IR is broken into three major segments. An 8-bit operation code (OP CODE) defines the format (RR, RI, or RX) and an address location within the DROM on CPU-A. The DROM address extracts the microprogram address of the emulation sequence. Two 4-bit fields are called the user general register destination (YD) and the user general register source or index (YS). These 4-bit fields select one of 16 general registers on the CPU-B board.

The Auxiliary Instruction Register (AIR) is a 12-bit register used during the RX squared format instructions. (Refer to Sheet 12 of 35-770D08.) The first eight bits are the operation modifier code. The remaining four bits are used by the microprogram as a data constant. The AIR may be examined by unloading the YSI field of the IR after the calculate address of an RX squared format. After reading the contents of the AIR, it is cleared.

12.11 FORMAT DECODING

Format decoding controls the operation of the calculate address. There are four basic formats of user-level instructions, register-to-register (RR), immediate data-to-register (RI), memory data to register (RX), and string manipulation (RX squared). The format type is decoded from the OP CODE portion of the IR. The 8-bit OP CODE field is used to select a 4-bit word within the format ROM. The state of the four data outlines determines the format currently being executed. The RI1 format is implied by the default (all four outputs inactive) of the format ROM outputs. The format ROM output that indicates an RX format is further decoded into three RX formats: RX1, RX2, and RX3. The state of MDR bits 00, 01, and the RX format ROM output selects one of the three RX formats.

12.12 CALCULATE ADDRESS

The calculate address is initiated by a microprogram specified Instruction Read (IR). The calculate address logic resolves the Instruction Read (IR). The calculate address logic resolves the format requirements of the current user instruction being executed. At the conclusion of the calculate address, the following conditions exist, depending on the selected instruction format:

RR — The Shift Register and the MAR equal the contents of the general register specified by the YS field.

RI1 — The Shift Register and the MAR contain the 32-bit data resulting from the addition of the contents of the general register specified by the YS field and the sign extended least significant 16 MDR bits.

RI2 — The Shift Register (SR) and the MAR contain the 32-bit data resulting from the addition of the contents of the general register specified by the YS field and the full 32 bits of the MDR.

RX1 — The Memory Address Register (MAR) and the SR contain the program address of the second operand data contained in memory. This address is the result of adding the sign extended least significant 16 bits of the MDR and the data contained in the general register specified by the YS field.

RX2 — The MAR and the SR contain the program address of the second operand data contained in memory. The program address is the result of adding the contents of the general register specified by the YS field, the sign extended least significant 16 bits of the MDR, and the incremented contents of the location counter. Bits 0:19 of the SR are undefined.

RX3 — The MAR and the SR contain the program address of the second operand data contained in memory. The program address is the result of adding the contents of the general registers specified by the YS field and MDR bits 4:7 and the least significant 20 bits of MDR. Bits 0:19 of the SR are undefined.

RX Squared — The SR contains the program address of the source data string. This address is generated during the first half of the RX squared format in the same manner as defined by the RX1, RX2, or RX3 formats. The MAR contains the program address of the destination data string. This address is generated during the second half of the RX squared. The address contained in the MAR is the result of addition in the same method as RX1, RX2, or RX3.

The microword contained in the RD register during the calculate address is an Add operation. The SR is the destination. The general register specified by the YS field is the A bus source, and the MDR is the B bus source. Instruction Read and MDR sign extend are also specified. The MAR is forced to be a destination during calculate address.

Figures 12-8 through 12-15 are examples of the logic sequences during calculate address. All the figures show examples when there is no memory contention. The microprogram and the calculate address are suspended as required (MSTOP0). Refer to Sheets 10 and 11 of 35-770D08 during this description.

Figures 12-8 and 12-11 depict the sequence required for RR, RX1, or RI1 formats. Figure 12-12 differs in that the fullword instruction (RX1, RI1) starts on a halfword boundary and must therefore initiate two memory cycles to fetch the required 32 bits. GGDIR1 becomes active when the microword specifies an IR and if no repeat counter operation is in progress or no interrupts were queued during the previous instruction execution. The next CLK1 causes a memory read to the address specified by the Location Counter (LOC). The LOC is incremented (ILOC) at the trailing edge of CLK1. The ALIR1 flip-flop is direct set during CLK1. This allows the IR to be loaded when the memory data is available (DUA0). The FINR1 and CAP1 flip-flops are set at the trailing edge of CLK1. The format of the instruction is determined by the contents of the IR (if it is an RX format) and MDR bits 0 and 1. The instruction format determines if DISA0 or DISB0 is active. Disable the A Source (DISA0) is active on RX or RI formats if the YS field of the IR is zero. When the YS field is zero, no index value is to be added. When DISA0 is active, the A bus source data is forced to be inactive. This results in the MDR being added to zero. RR format instructions disable DISA0. The YS field equal to zero is a valid A bus source for RR instructions. Disable the B Source (DISB0) is made active by the RR instruction format. The MDR is specified by the microword to be the B source data. The MDR is invalid for RR instructions. DISB0 forces the B bus data to be inactive. The contents of the general register by YS are added to zero. The LOC is incremented (ILOC) on the first clock after CAP1 is set by FCP1 if the format is not RR. FCP1 ensures that ILOC occurs for only one clock period.

In Figure 12-11, in addition to the previous description, GSIR0 becomes active on the same CLK1 that FINR1 sets. GSIR0 indicates that a second read is initiated. The data contained in the MDR is not valid until the second read, when memory data is available. The calculate address is suspended until the MDR is valid. The GDIR0 signal is inhibited by the RR format decoding.

The final CLK1 of the calculate address loads the SR and MAR with the result of the microinstruction Add operation. The CSAR is loaded on the leading edge of CLK1 with an X'007' if a memory fault occurred during the calculate address or if the instruction in the op-code is not an exercised option; e.g., HPFPP. If no memory fault exists and if the instruction is legal, the D1 address vector, as selected by the op-code data, is loaded into the CSAR.

Figures 12-9 and 12-12 are examples of calculate address for the RX2 format. The RX2 format starts the same as RX1 and is decoded during FCP1 and causes RX2STP0. RX2STP0 keeps CAP1 from resetting on the next MCLK1A. This allows LOC to be incremented before it is added into the address calculation. The MDRE0 signal becomes active during CAP1 when the RX2 format is decoded. The MDRE0 causes the MDR data on the CPU-C to be added to the incremented LOC which is available on the output of the PA multiplexor. The MDR source data on the B bus reflects the results of the addition. The SR and MAR are loaded with the results of adding the contents of YS and the MDR adder output. Figure 12-12 shows the effect of GSIR0 on the RX2 format.

Figures 12-10 and 12-13 are examples of calculate address for 48-bit instructions, RX3 and RI2. RX3 and RI2 format instructions use the full 32-bit MDR to complete the calculate address. The calculate address for RX3 and RI2 formats is in two parts, defined by CAP1 and CAP2. During CAP1, the LOC is incremented, the format is decoded, and the contents of the general register specified by the YS field are loaded into SR and MAR. The B bus source data is disabled (DISB0) as it was during RR formats. RX3STP0 suspends the microprogram during the CAP1 cycle. CMR20 and CAP21 become active on the same MCLK1 that CAP1 resets. CMR20 causes a halfword memory read to fetch the remaining 16 bits for the least significant 16 bits of the MDR. CMR20 also causes the LOC to be incremented to reflect the 48-bit instruction length. The RI2 format causes the 32-bit MDR, when it is valid (DUA0), to be added to the contents of YS and is loaded into SR and MAR. The RX3 format causes MDRE0 to become active, enabling the MDR adder on the CPU-C. CAMA0 goes low when CMR20 is inactive and CAP2 is active. This selects the contents of the MAR on the outputs of the PA multiplexor of the CPU-C. During CAP2, with the RX3 format, X20 goes low, enabling MDR bits 4:7 to select the second level index general register. The final clock of the calculate address loads the added result of the contents of the general register specified by MDR bits 4:7 and the MDR adder output. The MDR adder output consists of the contents of the MDR and the contents of the general register specified by YS, which was loaded into the MAR during CAP1. The most significant 12 bits of the MDR adder output are undefined. Figure 12-13 shows the effect of GSIR0 on 48-bit formats. GSIR0 is caused by starting the instruction on a halfword boundary.

The RX squared instruction format requires two calculate address sequences. Each calculate address operation is essentially an RX format calculate address. The back-to-back calculate address sequences may each be RX1, RX2, or RX3 format. The result of the first calculate address is contained in the SR. The second result is loaded into the MAR. Figures 12-14 and 12-15 are examples of the RX squared format calculate address. Figure 12-14 shows the sequence for an RX1 followed by an RX1. Figure 12-15 shows an RX1 followed by an RX3. In either figure, there are few differences between the previously discussed RX format calculate address and the individual RX formats calculated in the RX squared. The MCLK1 that causes CAP1 to reset in the first calculate address loads the SR and MAR with the RX1 address data. 2IR0 becomes active because of the RX squared format. BLIR1 sets on the leading edge of MCIK1 and the memory read for the second RX format is started. ALIRCK0 enables the Auxiliary Instruction Register (AIR) and the YS field of the IR (Sheet 12 of 35-770D08) to be loaded when the memory data becomes available. DSTOP0 is held active by 2IR0 and AFINR1. This prevents the address data contained in the SR from being overwritten. MARSTP1 enables the MAR to be loaded when DSTOP is active.

The Length Counter (Sheet 11) is incremented each time the LOC is incremented. This provides an instruction length count at the conclusion of calculate address. The length counter is cleared at the beginning of each instruction read.

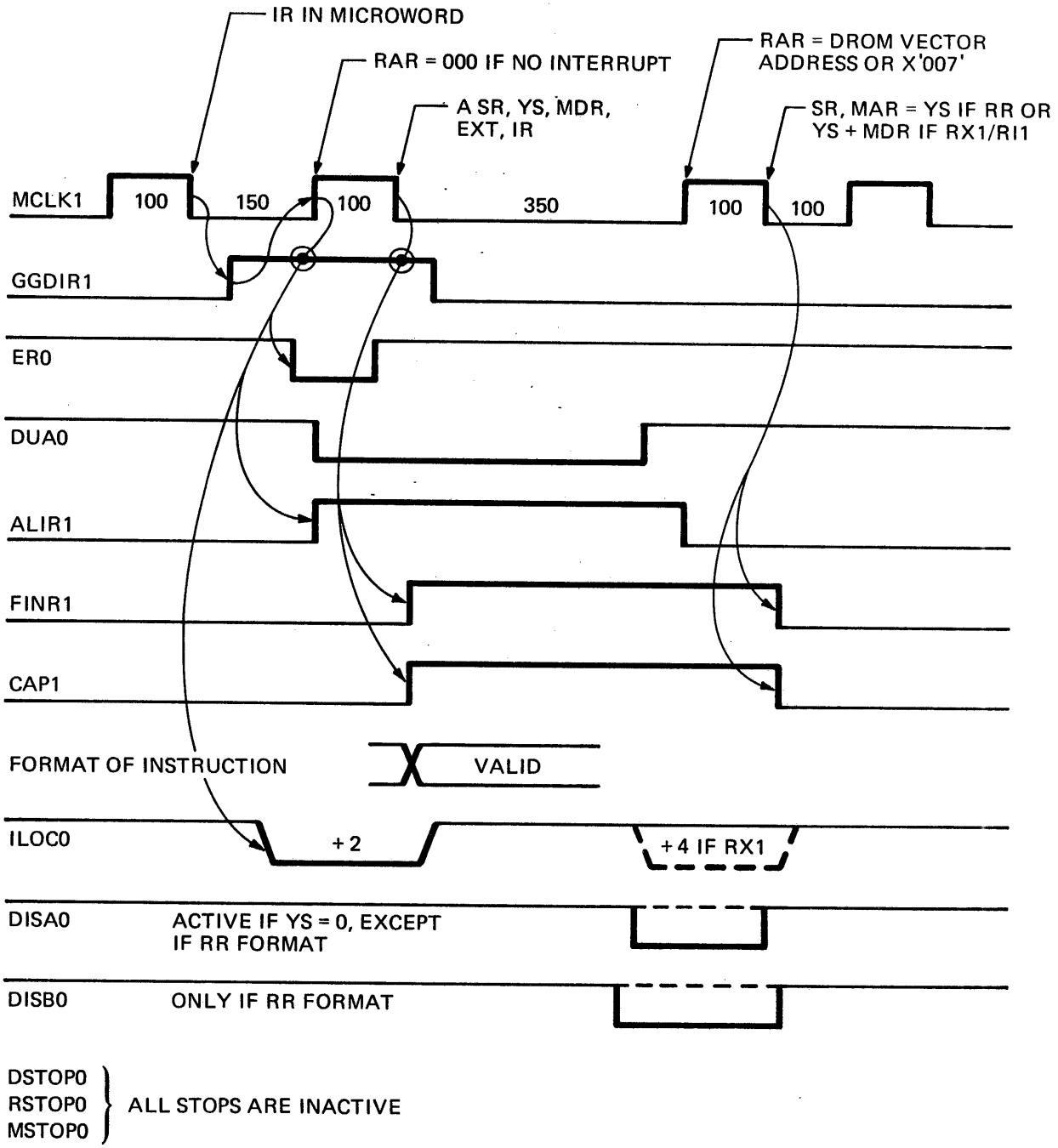


Figure 12-8 RR, RX1, or RI1 Format (Instruction on a Fullword Boundary)

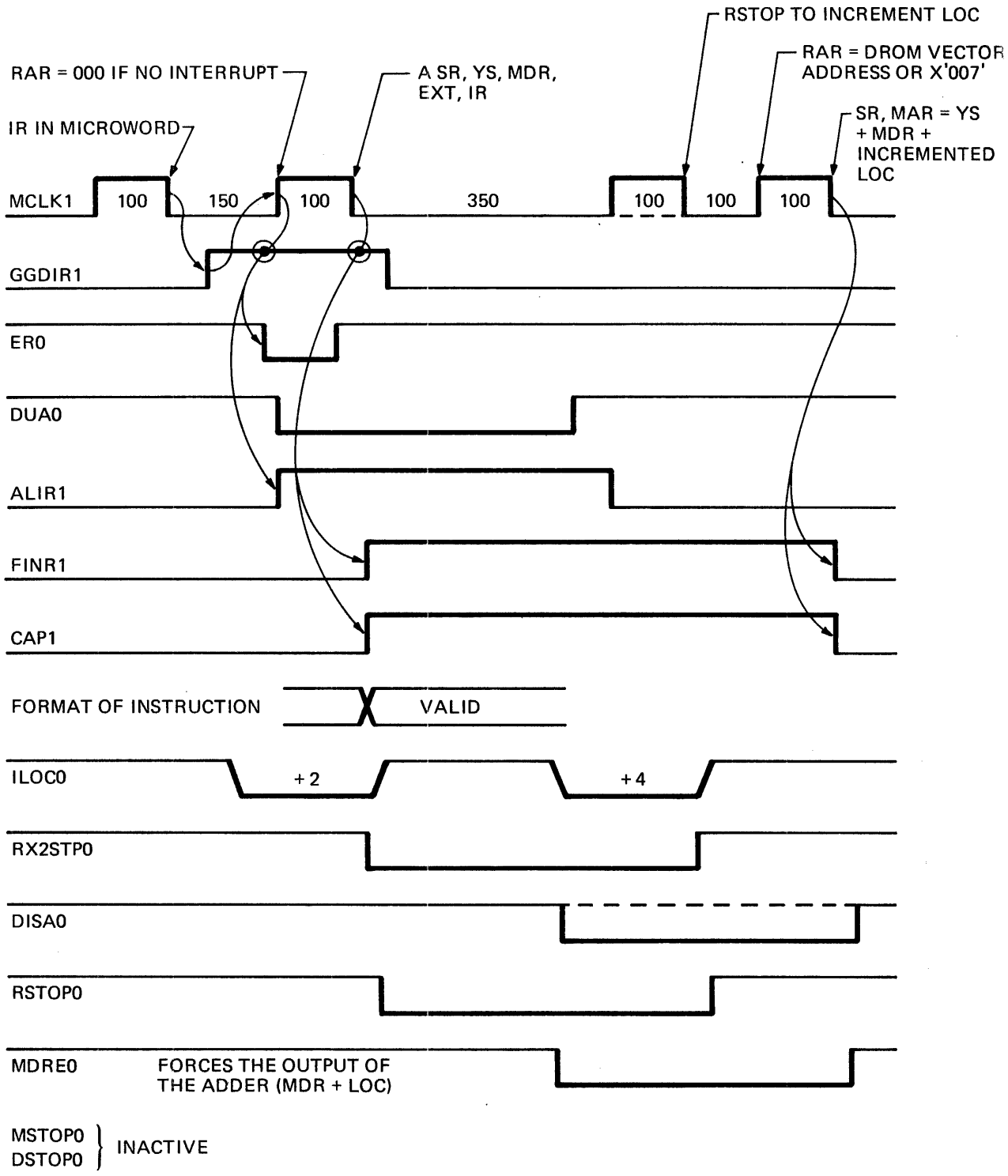


Figure 12-9 RX2 Format (Instruction on a Fullword Boundary)

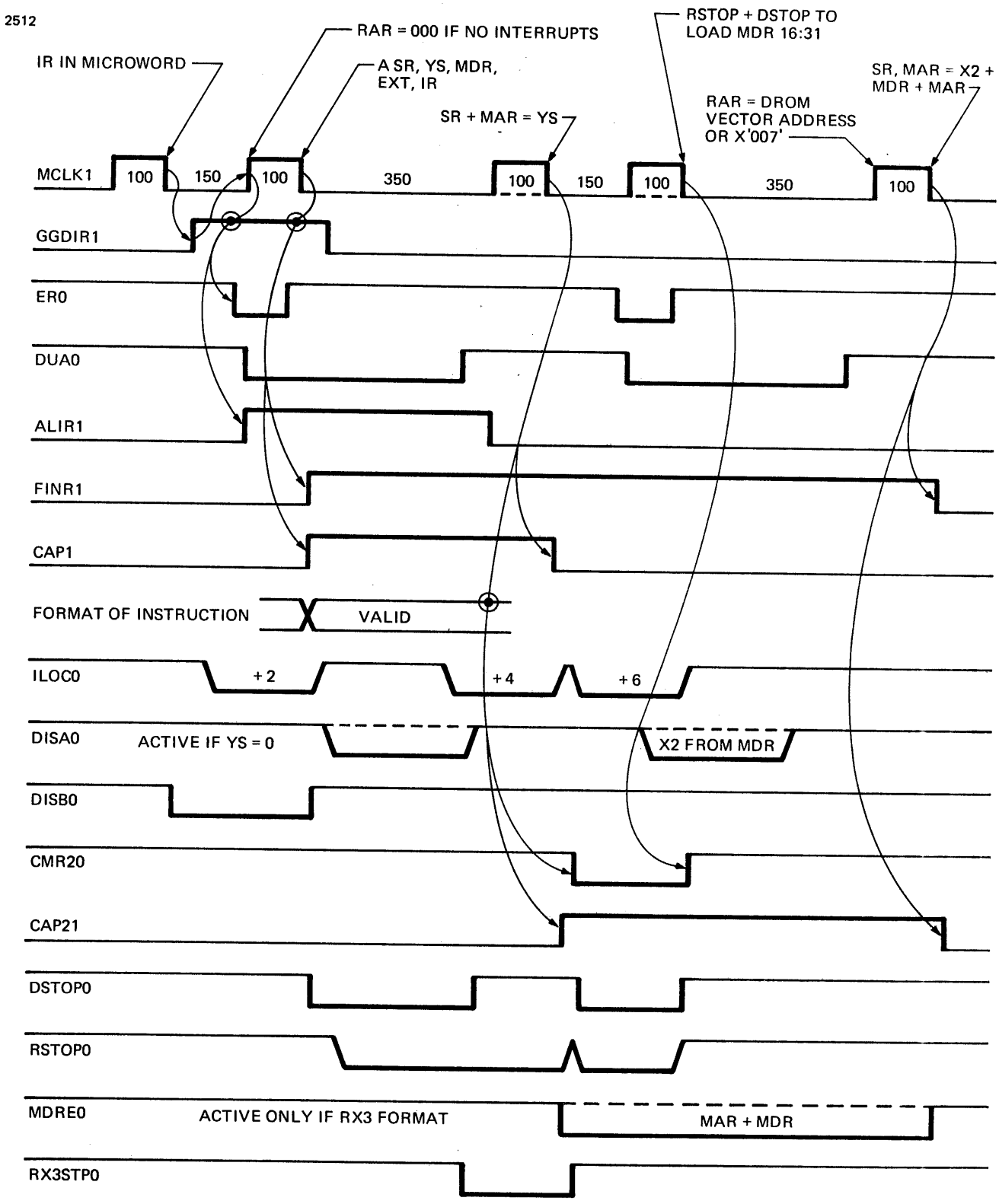


Figure 12-10 RX3 or RI2 Format (Instruction on a Fullword Boundary)

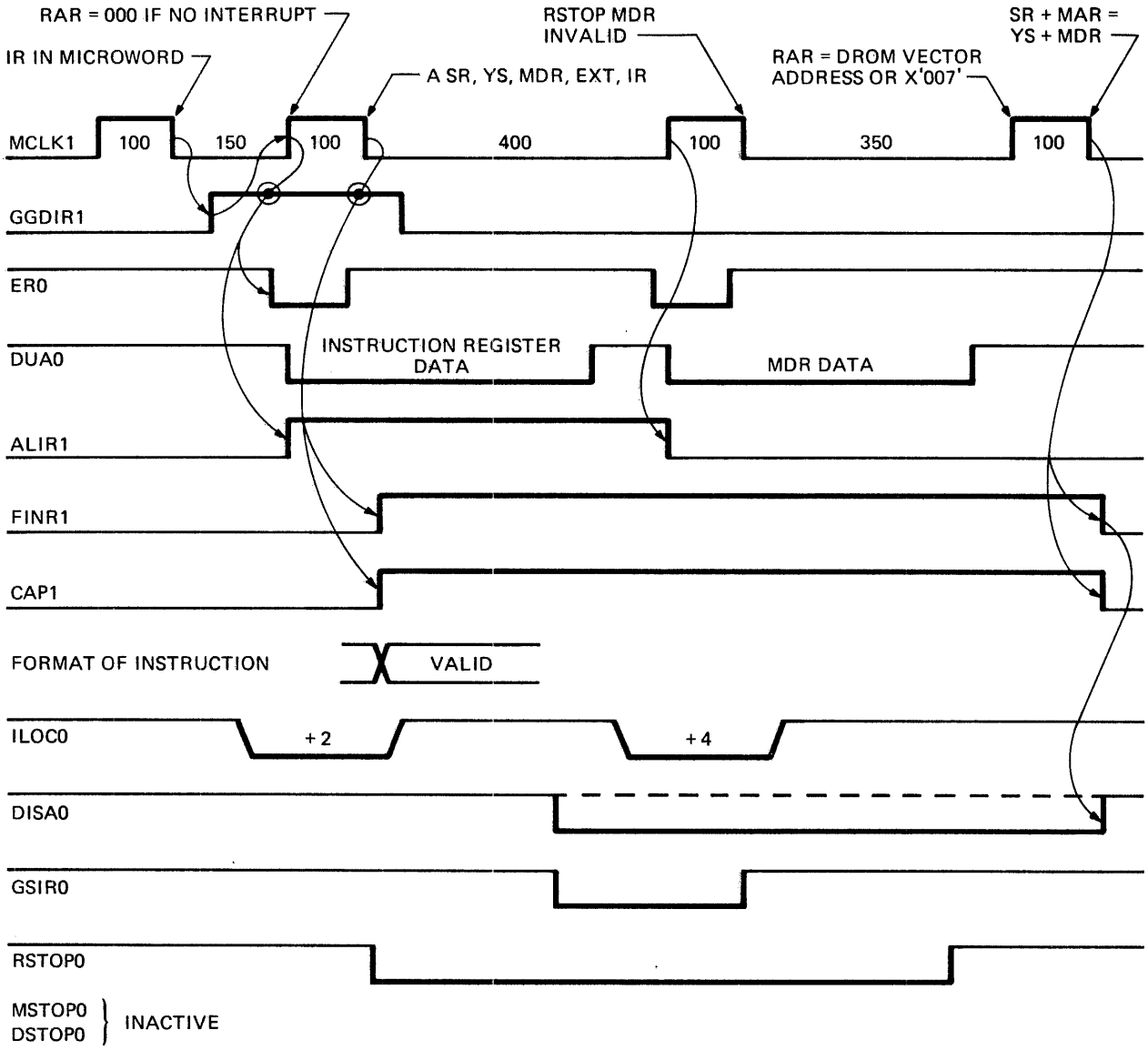


Figure 12-11 RI1 or RX1 Format (Instruction on a Halfword Boundary)

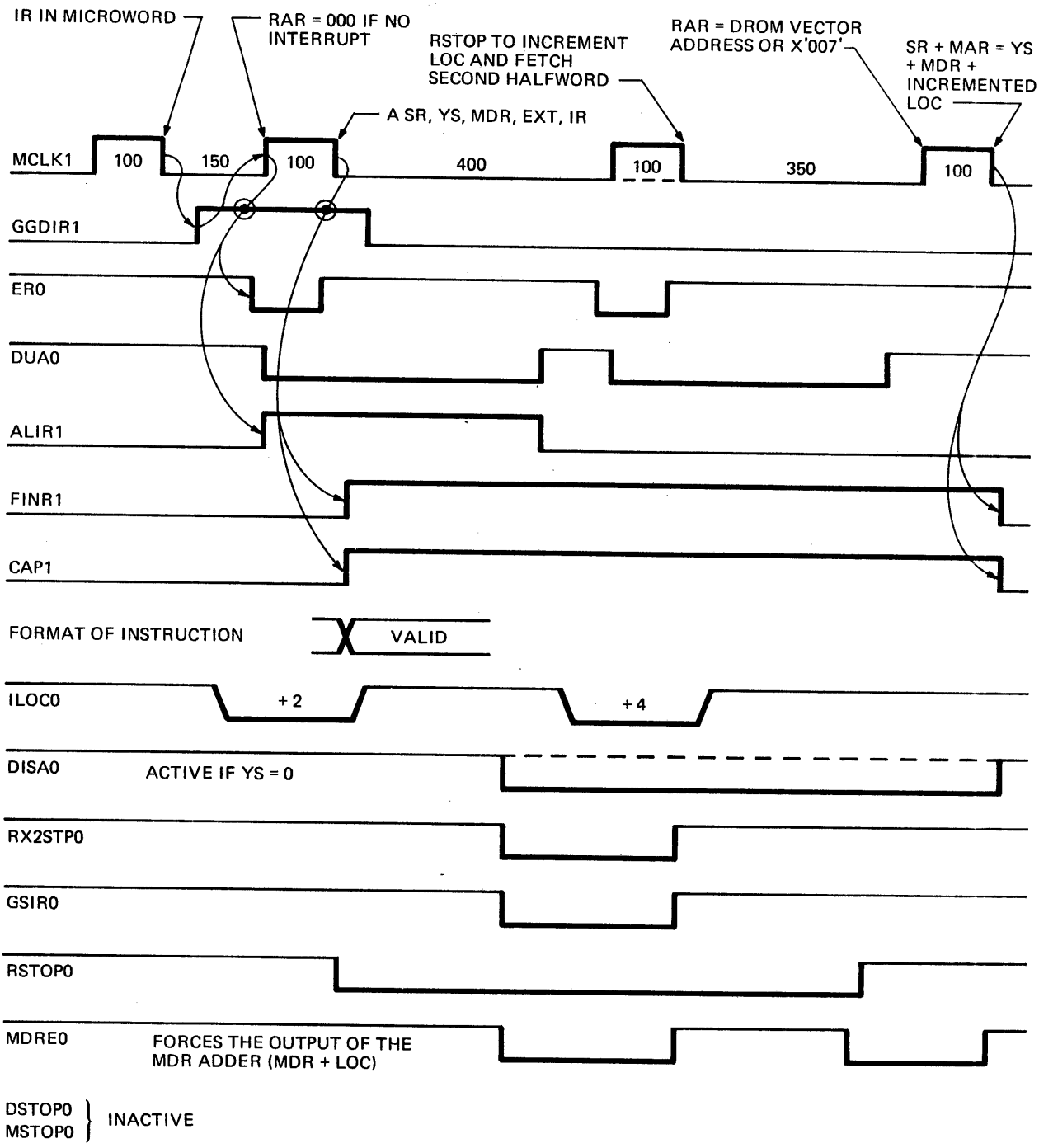


Figure 12-12 RX2 Format (Instruction on a Halfword Boundary)

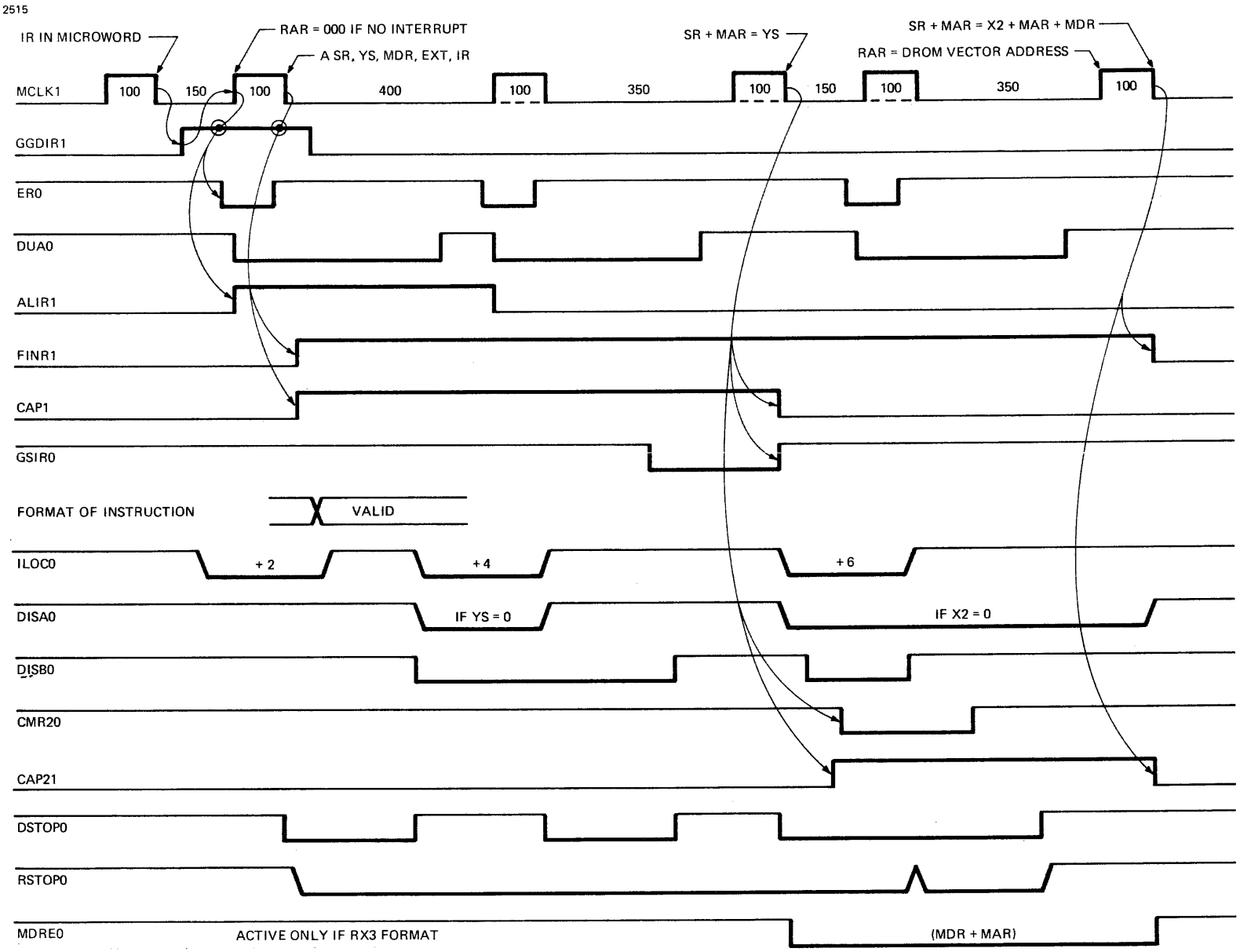


Figure 12-13 RX3 or RI2 Format (Instruction on a Halfword Boundary)

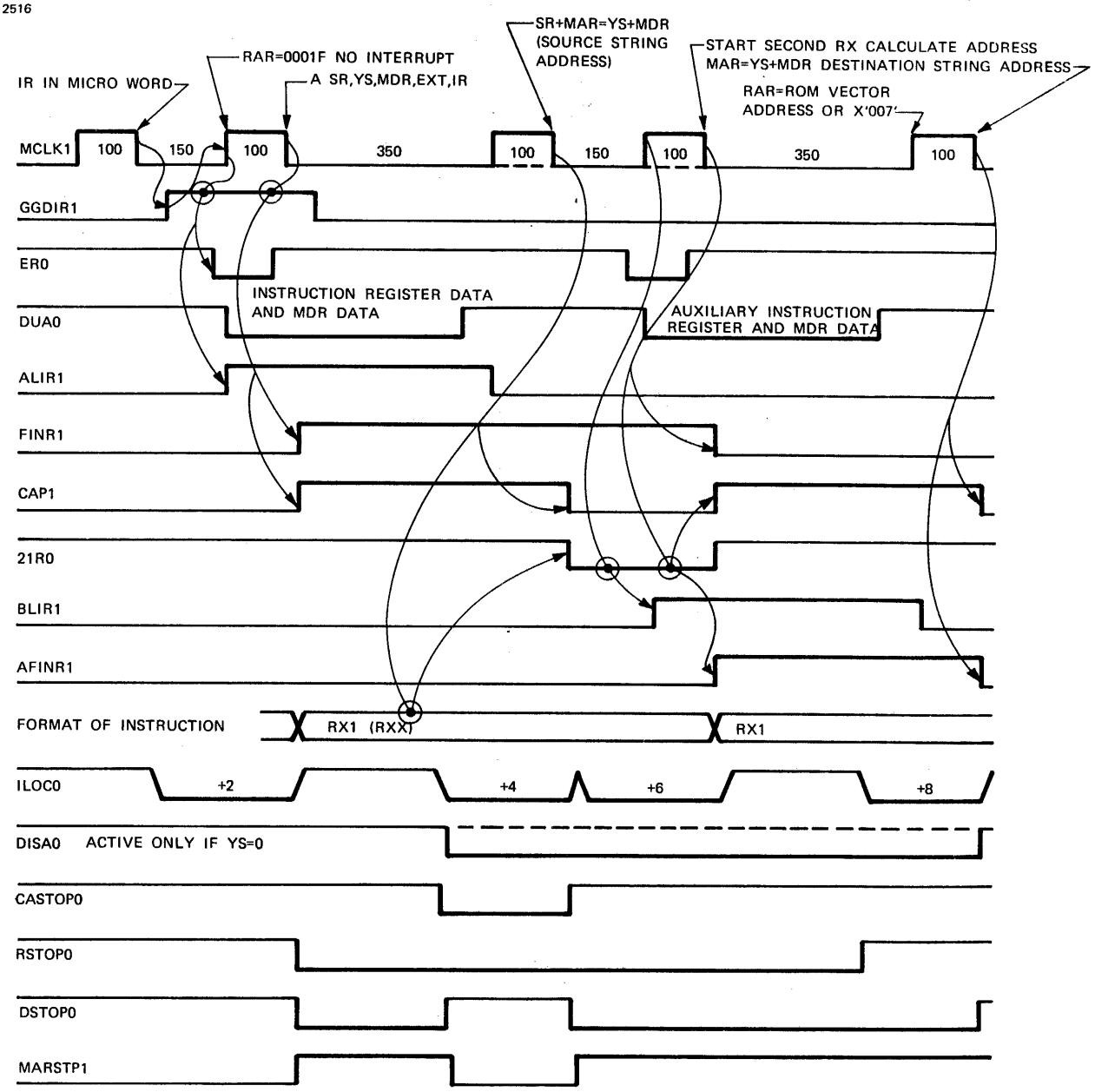


Figure 12-14 RX Squared (RXX) Format (RX1 Followed by RX1) (Instruction Starts on a Fullword Boundary)

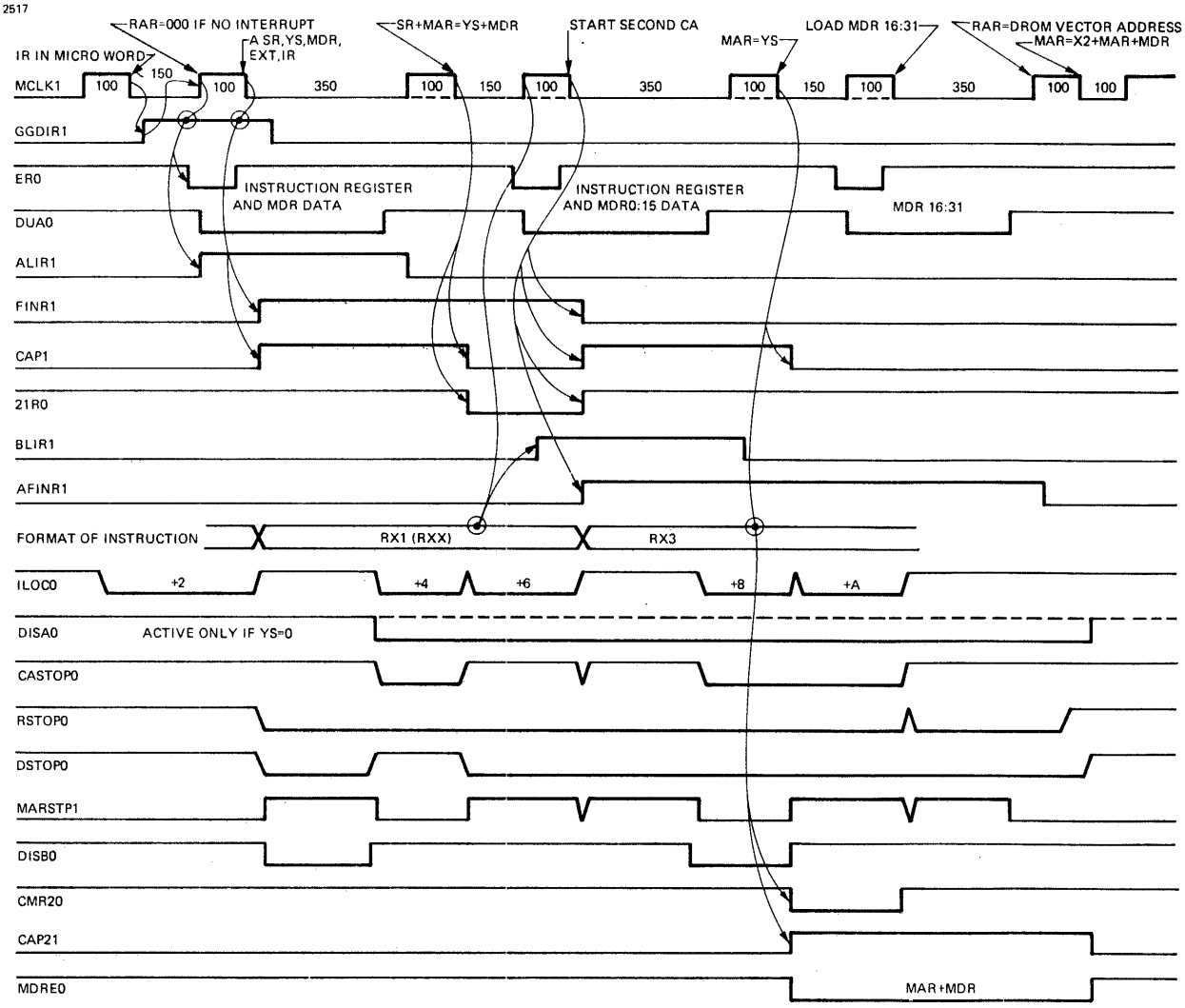


Figure 12-15 RX Squared (RXX) Format (RX1 Followed by RX3) (Instruction Starts on a Fullword Boundary)

12.13 REPEAT COUNTER

The repeat counter (Sheet 11) is a 6-bit down counter which provides the ability to repeat a microinstruction up to 64 times. This is accomplished by loading the counter with the complement of the data on the S bus. Once the counter is loaded, RSTOP0 is forced active by CNTE00 until the counter is empty. The counter's count is decremented by one for each CLK1F if MSTOP and OPSTOP0 are not active.

12.14 B BUS MULTIPLEXORS

The B bus multiplexors on the CPU-D (Sheet 14) provide the B source information when I/C, LENGTH, YSI, or YDI is specified by the microinstruction. The contents of the AIR and either LENGTH, YSI, or YDI are provided once after an RX squared format calculate address has occurred. After the AIR has been read, it is cleared and then provides the inactive data bits 16:27 for LENGTH, YSI, and YDI. The most significant 16 bits of the 32-bit CPU-D B bus source are supplied by the CPU-B board as inactive data bits.

12.15 I/O SYSTEM

The I/O system provides the ability for the microprocessor to communicate with devices external to the processor. These devices and their controllers are connected to the I/O multiplexor bus. Refer to Sheet 13 of 35-770D08 during this description. The I/O multiplexor bus consists of a 16-bit bidirectional data bus and nine control lines.

Figure 12-16 shows an example of an I/O output operation. This sequence applies to the device addressing (ADRS), transmission of data to the device (DA), and transmission of command data (CMD). When a microinstruction specifies I/O as a destination, IOSTOP0 becomes active. IOSTOP0 causes RSTOP0 (Sheet 9) which suspends the microprogram. This is necessary to hold the data on the I/O bus until the operation is complete. The trailing edge of the first MCLK1 causes FDAT0 to become active. FDAT0 enables the I/O data bus transceivers and the data on the S bus is placed on the I/O multiplexor bus. The next MCLK1 causes FCOUT to become active. FCOUT causes the I/O output control line, selected by RD bits 29, 30, and 31, to become active. When the I/O control line becomes active, the device, if selected, responds with SYN0. The first leading edge of MCLK1 after the receipt of SYN0 causes the BSYN0 (13K2) flip-flop to set. On the trailing edge of the MCLK1 causing BSYN0 to set, FSYN0 sets. When FSYN0 becomes active, IOSTOP0 becomes inactive, allowing the microprogram to continue. The trailing edge of the MCLK1 following the setting of FSYN0 causes FCOUT0 and FDAT0 to reset, completing the operation.

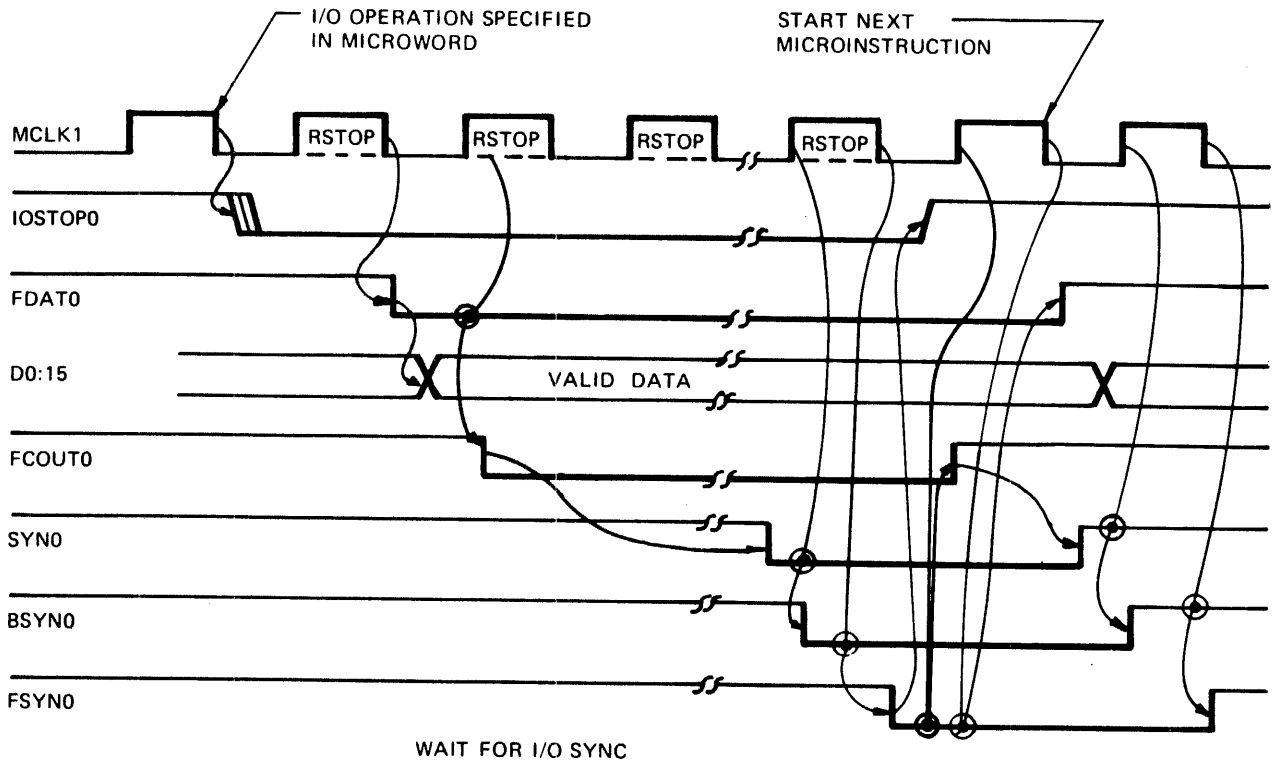


Figure 12-16 I/O Output Operation (ADRS, DA, CMD)

Figure 12-17 is an example of an I/O input operation. The sequence shown applies to request for device status (SR), request for data from the selected device (DR), and acknowledge interrupt (TACK). When a microinstruction specifies I/O as a source, IOSTOP0 becomes active suspending the microprogram until the data is received from the selected device. FCIN0 sets on the leading edge of MCLK1 after IOSTOP0 becomes active. FCIN0 enables the received data through the data transceivers. The selected device responds by causing SYN0 to be active. When SYN0 is active, the data from the device is valid on the I/O data bus. The leading edge of the MCLK1 following the receipt of SYN0 causes the BSYN0 flip-flop (13K2) to set. On the trailing edge of the MCLK1 after BSYN0 sets, FSYN0 sets. When FSYN0 becomes active, ISTOP0 becomes inactive, allowing the microprogram to continue. The clock following the setting cf FSYN0 becomes the destination clock for the input I/O operation.

The acknowledge interrupt control has four outputs. These are used for the four possible I/C interrupt priority levels. The TACK lines are controlled by PSW27 and PSW26. When COMM is the device to be acknowledged, TACK00 is forced regardless of the state of PSW27 and PSW26.

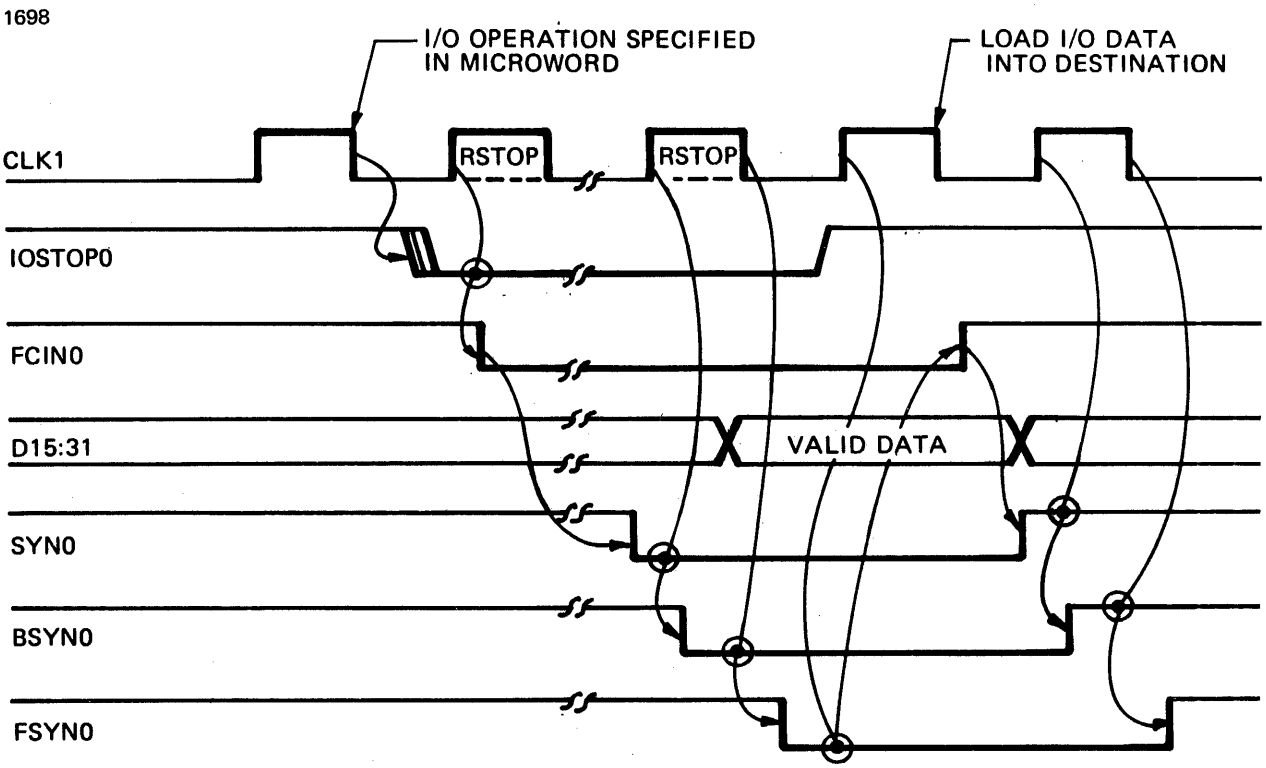


Figure 12-17 I/O Input Operation (SR, DR, TACK)

12.16 MNEMONICS

The following is a list of the mnemonics found on the CPU-D board. The 35-770D08 schematic location and a brief description of each signal are provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
ACLR0	A clear signal on power up or down	2H1
ADRS0	Address control line for I/O bus - selects specific I/O controller	13D6
ADV0	A device signal which defeats the RSTOP caused by TRAP0 from CPU-A Test Aid	9D1
AFINR	Auxiliary instruction read flip-flop - used during second RX format of RXRX instruction	10D2
AIR00:11	Auxiliary instruction register - bits 00:11 contain second RX format op-code and YD fields	Sheet 12

MNEMONIC	MEANING	SCHEMATIC LOCATION
AIRQ0	Auxiliary instruction register queue - allows AIR tc lcad seccnd RX informa-tion	10L4
ALIR0	A load instruction register flip-flop signal - defines the loading of IR as opposed tc the AIR	10M5
ALIRCK0	Auxiliary IR clock	10R5
AMDR001 AMDR011	Auxiliary MDR bits use no instruction decoding for calculate address	3M7 3M8
AMDRCK0	Auxiliary MDR clock for loading the YS field	7J5
AMSTOP0	A memory stop - inhibits MCLK, RCLK, DCLK	9F4
ANS0	Answer - EDMA bus control sequel generated when either local or shared memory is read from	8K7
ASEL1	Select line for CPU-D board B bus source data	14H9
A1B10	A timing pulse generated from CPU clock generator logic	9L4
A1B11	A timing pulse generated from CPU clock generator logic	9L4
A1B11A	A timing pulse generated from CPU clock generator logic	9L4
B161:311	B bus signals	Sheet 14
BCLR0	B clear signal on power up or down	2H2
BCNT0	Board control signal - use to load data into the communication option board.	13C6
BLIR	B load instruction register flip-flop - defines the lcad time for the AIR as opposed tc the IR	10M5
BMSTOP0	B memory stop signal inhibits MCLK, RCLK, DCLK	9F5
BRANCH0	Branch - decoded from microcode	9G1

MNEMONIC	MEANING	SCHEMATIC LOCATION
BRSTO	Burst mode deccded from EDMA bus - defines EDMA mcde of data transfer where more than one halfword is transferred	5N8
BRTD1	Burst read mcde decoded from EDMA bus	5J6
BWRT1	Burst write mode decoded from EDMA bus	5J7
CACLK1	Calculate address clock - allows either the exit from calculate address or the second RX fetch in RXRX format	10M7
CAIR	Clear auxiliary instruction register flip-flop - clears the AIR so that 4-bit sources dc not ccntinue to display the AIR	12K4
CAMAO	Calculate memory address - used by the CPU-C to cause the MDR adder to use the MAR rather than LCC	10G4
CAP1	Calculate address part 1 - used by all formats of instructions. Calculate address is ccmpleted on all 32-bit or less length instructions.	10G2
CAP2	Calculate address part 2 - used by 48-bit format instructions	10G4
CAR261	A carry line fcr the EDMA MAR	15J6
CASTOPO	Calculate address stop - while active, the processor is suspended in calculate address.	10M6
CCLRO	C clear signal on power up or down	2H2
CLADAO	Clear address and data registers for EDMA to memory	7H1
CLFLRO	Clear flag register	13H7
CLK1	Nonstoppable processcr clock	9N5
CLK1A:1F	Nonstoppable processor clock	Sheet 9
CLRDYO	Clear ready flip-flop	7E1
CLSO	Clear local memory request and start flip-flops	7D2

MNEMONIC	MEANING	SCHEMATIC LOCATION
CLSTA0	Clear MAT status register	7F8
CLST0	Clear FSOT	2M8
CMD0	Command control line for I/O bus - define when data on the I/O bus is for command information	13E6
CMR20	Calculate address memory read halfword - during calculate address of 48-bit formats, a third halfword must be fetched.	10G5
CNTE0	Count equal to zero - use to inhibit a specified instruction read until the microcode counter on the CPU-A has been completed	11R7
COMM0	Communication module - decode of E field. Data on the S bus is gated into the I/O bus and loaded into the communication hardware assist board.	12E4
COMSTP0	Communication stop - causes an RSTOP and inhibits the microprogram	13D2
CWR0	Change write memory to read memory	4G6
CYD0	Clear YD field of the instruction register - decoded from the E field of the microinstruction	12E3
D000:150	I/O data bus	Sheet 13
DA0	Data available control line for I/O bus - validates data on the I/O bus being sent to the devices	13E6
DANS1	Answer to EDMA bus	8H5
DAWT1	Data write into memory	6D3
DCLK0	Destination clock	9N8
DCLR0	D clear signal on power up or down	2H1
DDUA0	EDMA data unavailable	4N2
DISA0	Disable A source data - used during calculate address to inhibit A source data when YS is equal to zero	10G8

MNEMONIC	MEANING	SCHEMATIC LOCATION
DISB0	Disable B source data - used during calculate address to inhibit MDR data when it is incomplete or when an RR format is executing	10D5
DISEXT0	Disable sign extension - disable the MDR sign extension during calculate address	11H2
DL081:171 DL181:291 DL301	EDMA MAR output - after buffering, these drive the LMA bus.	Sheet 15 Sheet 16, 15B9
DMA000:030	EDMA bus lines	Sheet 15
DMA040:150	EDMA bus lines	Sheet 16
DMA160:170	EDMA bus lines	5A9
DMABZ1	DMA busy	2M7
DMAHW0	EDMA halfword mode	5H8
DMALM1	DMA to local memory	2K7
DMARS0	EDMA read and set - memory reads addressed location B EDMA and then restores the AW with the MSD bit set.	5H9
DMASEL	EDMA select flip-flop	2N6
DMASM1	DMA to shared memory	2K7
DMAWRT0	EDMA write	7R8
DMEM0	Decoded microinstruction memory operation	4F7
DMX080:150	EDMA bus lines	Sheet 15
DOIT0	Allows the MAR to be loaded during the calculate address of RXRX format instructions	10M7
DOSC0	EDMA oscillator for memory to EDMA control logic	5F1
DR0	Data request control line for I/O bus - validates data on the I/O bus to be loaded into the processor	13D6
DRFAULT0	Decoded reset fault	12E5

MNEMONIC	MEANING	SCHEMATIC LOCATION
DSTOP0	Destination stop - inhibits the system clock from loading a destination. DCLK is stopped.	9L1
DUA0	Data unavailable control line from local memory - while this signal is active, the data on the memory bus is invalid.	4B2
ED001:151	Tristate output of EDMA MDR and input to EDMA transceivers	Sheets 17,
EDAT1	Even data halfword memory operation	6D4
EEDCLK0	EDMA even data register clock signal	7N5
EFLDEN0	E field enable	14F9
EFWRT1	EDMA fullword data write	2N4
EMDENB0	Enable even half of EDMA data register	8G1
EMDR001:151 EMDR161	EDMA MDR outputs used for driving the MDS bus	Sheet 17, Sheet 18
ENAOSC0	Enable oscillator for memory to EDMA data transmission	5H3
ENCE1	Noncorrectable error from memory on an EDMA memory access	10D7
ENEXC0	Enable external oscillator - for maintenance purposes	9J7
ENMAA0	Enable MAT access	4G6
ENXCVR0	Enable transceivers for a processor-to-EDMA transceiver	8H2
ECT0	End of transmission control line in EDMA bus protocol	8H8
ERD1	EDMA read	5G7
EVDAT	Even memory data operation for CPU flip-flop	6G4
EXOSC0	External oscillator connection - for maintenance cnly	9F9

MNEMONIC	MEANING	SCHEMATIC LOCATION
FADV1	Advance flip-flop output in clock single-step control	9E2
FAULTO	Lights the FAULT lamp on the system control panel	12G5
FB	The B flip-flop of CPU clock generator	9J5
FBIR	Instruction read flip-flop indicating an instruction fetch on a fullword memory address boundary	6G1
FBRTRD	Burst read flip-flop	5M6
FBRWRT	Burst write flip-flop	5M8
FCIN	Input control flip-flop for I/O operation	13A5
FCOMM	Communication module flip-flop for I/O operation	13C3
FCOUT	Output control flip-flop for I/O operation	13H5
FDA	Flip-flop used for generating memory to EDMA bus signals	Sheet 5
FDAA	Flip-flop used for generating memory to EDMA bus signals operation	Sheet 5
FDAAO	Auxiliary FA used in the memory to EDMA control	5L2
FDAT	Data control flip-flop for I/O operations - data on the S bus is transmitted into the I/O bus.	13K4
FDB	Flip-flop used for generating memory to EDMA bus signals	Sheet 5
FDC	Flip-flop used for generating memory to EDMA bus signals	Sheet 5
FDECT	Detected end of transmission flip-flop used in burst read from local memory	2C9
FDRDY	Data ready flip-flop used for look-ahead in burst read from local memory	5L4
FDUA	Data (from local memory) unavailable flip-flop	4E2

MNEMONIC	MEANING	SCHEMATIC LOCATION
FDUSKF	Data unavailable skip flip-flop - causes an added 50 ns on the up time of CLK1	4E3
FEFW	EDMA fullword flip-flop	5G8
FEIR	Even address instruction read flip-flop - used when instruction read is started on a halfword boundary; suppressed on RR formats	6G2
FENCE	The flip-flop that stores state of ENCE1 on an EDMA access of memory	7N2
FFOT	End of transmission flip-flop	8K8
FER	Early read flip-flop	9J5
FERD	EDMA read flip-flop	5G6
FINR	Instruction read flip-flop	10G1
FLADR	Load EDMA address flip-flop	2J4
FLADRA	Load first halfword of EDMA data flip-flop	2M5
FLADRE	Load second halfword of EDMA data flip-flop	2N4
FLMRQ	Local memory request flip-flop	2G8
FMREQ	Memory request flip-flop	2D4
FNCEQ	Noncorrectable error flip-flop indicates a detected multiple error during a processor memory read	10G6
FOIR	Odd address instruction read flip-flop - used when an instruction read occurs on a halfword boundary. Second halfword is feteched when FEIR is set.	6G2
FPA FPB FPC FPD FPE FPF FPG	EDMA protocol generating flip-flops	Sheet 6

MNEMONIC	MEANING	SCHEMATIC LOCATION
FPPF0	Primary power fail - this signal is generated on the CPU-A board and is used to generate an I/O device status bit during sense status.	13G6
FQEOT	EOT queued for burst read to memory	2G7
FRD	Memory read operation flip-flop	6G2
FSCLK1	Skew clock flip-flop	9F6
FSOT	Start of transmission flip-flop for EDMA to local memory	2F4
FSYN	SYNC flip-flop for I/O operations	13L5
FTIT1	When active, causes an MSTOP in order to provide the ability to single step through the microprogram	9G3
FW1	Fullword memory operation flip-flop	6H1
GBRANCH0	Gated branch	9G1
GDAT0	Gate data from S bus to I/O bus	13K7
GDIR0	Gated decoded instruction read - this signal is generated on the CPU-A. When active, it indicates the attempt to initiate an instruction read cycle.	10A1
GENMAA1	Gated enable MAT access	4J6
GEOT	Gated EOT signal	8M8
GGDIR1	GDIR0 is inhibited if the repeat microinstruction counter is not zero.	10D1
GMATSTOP0	Gated MAT stop	4J4
GRD0	Gated memory read	6L3
GSIR0	Gated second instruction read - queueing of the requirement for a second memory read when the instruction fetch is on a halfwrod boundary	6N2
HALT0	Halt honoring processor memory request	2K5
HOST1	Hold EDMA protocol oscillator stopped	8N2

MNEMONIC	MEANING	SCHEMATIC LOCATION
I40	Increment MAR by 4 - an E field decode	12E3
ILDMA0	Increment or load EDMA MAR	7N4
ILOC0	Increment LOC - this signal occurs during the calculate address sequence.	10C7
IMAR	Increment MAR by 4.	12J8
INHFS0	Inhibit false SYNC test point - disables the generation of the I/O false SYNC escape	13N1
IO161:311	IO data bits received from multiplexor bus	Sheet 13
IOP1	I/O operation has been specified by the microinstruction.	13K5
IOSTOP0	IO stop to inhibit RCLK - prevents the microinstruction from changing during I/O operations	13L6
IRD001:151	Instruction register input data lines that represent the OP CODE, YD, and YS fields	Sheets 3, 12
IRXX0	Used in the calculate address logic to inhibit the end of the calculate address sequence on the first format completion of an RXRX format instruction	10N2
LDCTR0	Load repeat counter	12N8
LDIO0	Load I/O	12N9
LDMAL0	Load EDMA MAR	7M3
LEN271:301	Length register bits	11N2
LER0	Local memory early read	4N8
LFLR0	Load flag register	12L7
LHWRT0	Enables multiplexor to output MDR16:31 to MDS00:15 for a write even halfword	7N9
LINC1	Length increment for length register	10M9
LIR1	Load instruction register	10R5

MNEMONIC	MEANING	SCHEMATIC LOCATION
LIRCK1	IR clock to load op-code	10A3
LMA080:310	Memory address bus lines	Sheet 15
LMBSY0	Local memory busy	4J2
LMDR1	Load memory data register	12N9
LMREQ0	Local memory request	2A4
LOAD0	EDMA bus load signal for address or data	8K7
LPSTD0	Load process segment table descriptor	12E1
LSSTD0	Load shared segment table descriptor	12E1
LWRT0	Load write - enables the multiplexors to drive MDS000:310 to local memory	7N8
LYDI0	Load YD immediate - RD decoding of the destination field that implies that the YD portion of the IR is loaded	12M9
LYSI0	Load YD immediate - RD decoding of the E field that causes the YS field of the IR to be loaded from the least significant 4 bits of the S bus. The register specified in the destination field of the microinstruction is also loaded.	12E5
MARSTP1	Memory address register stop	9L1
MATSTOP0	MAT stop	4G4
MCLK0	Memory clock	9M8
MDHCLK0	MDR clock for MDR00:15	7J4
MDHSA1	Memory data register high (even) select line for inputting to the MDR	7E3
MDLCK0	MDR clock for MDR16:31	7J6
MDLSA1	Memory data register low (odd) select line for inputting to the MDR	7E3
MDRE0	Memory data register adder enable - generated for the CPU-C board during calculate address	11J7
MDS000:150 MDS160:310	Memory data bus	Sheet 17 Sheet 18

MNEMONIC	MEANING	SCHEMATIC LOCATION
MDSBO	Memory data register select line for inputting to the MDR	7E2
MFAULTO	Memory fault indicates that a MAT, NCE, or alignment fault interrupt is pending. DSTOP is forced active until the interrupt is serviced.	9G1
MOPCLK1	MSTOP or OPSTOP clock	11K8
MREAD1	Memory read	6D2
MSBCO	MAT to shared bank controller	4G7
MSTOPO	Memory stop	9H4
NCEO	Noncorrectable error from memory	10A6
NOCNTO	No repeat counter operation	11R4
OEDCLKO	Odd EDMA MDR clock	7N7
OMDENBO	Odd EDMA MDR enable to EDMA bus	8F2
OPTSTPO	Option stop - this signal is generated by either the WCS or HPFPP options to inhibit the microprogram during their operations.	9H3
OSCO	Oscillator - buffered output of the 20 MHz crystal or the external oscillator divider flop	9L8
PA301	Program address bit 30	4B6
PDUA1	Processor data unavailable	4N1
PMEM1	Processor attempt to initiate a memory cycle	4D8
PROSC1	Protocol oscillator	6M9
PSBCO	Processor to shared bank controller	4G7
PSEL1A	Processor selected for memory operation	2N5
PSW181	Program status bits 18, 26, 27	10A7

MNEMONIC	MEANING	SCHEMATIC LOCATION
PSW261	Program status bits 18, 26, 27	13B5
PSW271	Program status bits 18, 26, 27	13B5
QUE0	Queue control line of EDMA protocol	6N5
RCLK0	ROM clock - this clock is inhibited by RSTOP and, when stopped, the microprogram stops.	9N8
RD001	ROM data register data bits forming the microinstruction	6A2
RD011	ROM data register data bits forming the microinstruction	4B5
RD021	ROM data register data bits forming the microinstruction	4B6
RD031	ROM data register data bits forming the microinstruction	12A7
RD041	ROM data register data bits forming the microinstruction	9G1
RD051	ROM data register data bits forming the microinstruction	9G1
RD121	ROM data register data bits forming the microinstruction	12J9
RD131	ROM data register data bits forming the microinstruction	12J7
RD141	ROM data register data bits forming the microinstruction	12J7
RD150	ROM data register data bits forming the microinstruction	12J7
RD161	ROM data register data bits forming the microinstruction	14D8
RD240	ROM data register data bits forming the microinstruction	14D8
RD251	ROM data register data bits forming the microinstruction	12E7, 12E8
RD261	ROM data register data bits forming the microinstruction	14D7

MNEMONIC	MEANING	SCHEMATIC LOCATION
RD271	ROM data register data bits forming the microinstruction	14D7
RD281:311	ROM data register data bits forming the microinstruction	12A6, 12A7
RDAX081:151 RDAT001:151 RDAT161:171	Received data lines from EDMA transceivers	Sheet 15 Sheets 15, 5A9
RDFW0	Read fullword	6M2
RESC0	Reset C flip-flop of EDMA protocol logic	8F6
RFAULT0	Reset memory fault interrupts	12H6
RI20	Format ROM output that indicates that the current op-code in the IR is a 48-bit immediate instruction	11F3
RI2RX31	Format decoded signal that indicates that a 48-bit format instruction is being processed (RI2 or RX3)	11H5
RMSR1	Read MAT status register	7C6
RR1	Register-to-register user instruction	11H1
RSTOP0	ROM stop	9L3
RX21	RX2 user instruction format	11H5
RX2STP0	RX2 user instruction stop - this stop allows the LOC to be incremented for the calculate address.	10N1
RX31	RX3 user instruction format	11H4
RXXSTOP0	RX squared format instruction stop	11H3
S161:311	S bus bits 16:31	Sheet 14
SAFINR1	Set A instruction read flip-flop	10A2
SB291	Set bit 29 - this signal, when active, causes bit 29 of the sensed I/O status to be set.	13F7
SCAP11	Set calculate address part 1 - causes the CAP1 flip-flop to be set	10D3

MNEMONIC	MEANING	SCHEMATIC LOCATION
SCLK1	Skew clock - delayed system clock. This clock starts 50 ns after CLK1. While CLK1 is stretched during its up time, SCLK1 is stretched during its down time.	9N6
SCLR0	System clear	2D2
SDFF1	Set data flip-flop	13K2
SER0	Shared memory early read	4N9
SMBSY1	Shared memory busy	2G8
SOT0	Start of transmission control line of EDMA protocol	6R7
SR0	Status control line for I/O	13C6
SRXX1	Set RX squared format instruction - causes the calculate address logic to be queued for RX squared format	11H1
STB1	Strobe	14J9
SV0	Set overflow caused by the I/O system when a false SYNC timeout occurs	13N6
SYN0	SYNC control line of I/O - response from selected device to any I/O control line activation	13M1
TACK000	Transmit acknowledge level 0	13A9
TACK010	Transmit acknowledge level 1	13A9
TACK020	Transmit acknowledge level 2	13B9
TACK030	Transmit acknowledge level 3	13B9
TPC0	Transmit priority chain line of EDMA protocol	6N6
TRAP0	Signal generated by the CPU-A on board test aid - this signal causes MSTOP which stops the microprogram.	9A3
ULIO0	Unload I/O decoded from the destination field of RD	14G6
ULYSJ0	Unload YSI	14H8

MNEMONIC	MEANING	SCHEMATIC LOCATION
UMDR1	Unload processcr MDR decoded from the destination field of the micro-instruction	14H7
WRT	Write in memcry line	4M3
X20	This signal is generated during the calculate address of an RX3 format and defines the second level index MDR data rather than the YS field of the IR.	10H3
XREQC	Request line of EDMA protocol	6B6
YD081	User destination register select bits 8, 9, 10, and 11	3M2
YD091	User destinatcn register select bits 8, 9, 10, and 11	3M2
YD101	User destinatcn register select bits 8, 9, 10, and 11	3M2
YD111	User destination register select bits 8, 9, 10, and 11	3M2
YDCLK0	Clock to increment, decrement, or load the YD field of the instruction register	3D4
YDM10	Decrement the YD field of the IR by one - this is decoded from the E field of the microinstruction.	12E3
YDP10	Increment the YD field of the IR by one - this is decoded from the E field of the microinstruction.	11E8
YS01	User source select bits 0, 1, 2 and 3	3M3
YS11	User source select bits 0, 1, 2 and 3	3M4
YS21	User source select bits 0, 1, 2 and 3	3M4
YS31	User source select bits 0, 1, 2 and 3	3M4

CHAPTER 13
4 MEGABYTE (4 MB) LCCAL BANK CONTROLLER (LBC)

13.1 INTRODUCTION

13.1.1 General

The memory system consists of 1 LBC and up to 2 Storage Modules (STMs) with a maximum main memory capacity of 4 Mb. The LBC used is the 35-771F04.

13.1.2 Power Requirements

Table 13-1 provides the power requirements for the LBC board.

TABLE 13-1 POWER REQUIREMENTS

VOLTAGE SYMBOL	NOMINAL VOLTAGE	MAXIMUM CURRENT DRAIN (AMPS)		
		CPERATING (SELECTED)	OPERATING (UNSELECTED)	BATTERY MODE
P5	+5.0 V	13.7A	13.7A	13.7A*
P5U	+5.0 V	1.8A	1.8A	1.8A

*P5 supply may be depowered in the battery mode.

13.1.3 Strapping and Test Point Information

The following test points are located on the front edge of the 35-771F04 LBC Board:

1. ECC Disable (TP1 and TP2, Sheet 5)

   Strapping TP1 to TP2 disables the Error Check and Correction (ECC) circuit, thereby preventing correction or detection of data errors. The error logger cannot be updated with the ECC disabled.

For normal ECC and error logger operation, TP1 and TP2 should be left unstrapped.

2. TP3-TP4 Strap

   TP3-TP4 must always be strapped for this system.

3. P5U Monitor (TP6, Sheet 13)

   The P5U supply voltage (+5.0 V + 1%) may be monitored at TP6 using TP1, TP3, or TP7 for the ground reference.

4. MB1 Monitor (TP5, Sheet 13)

   The MB1 flip-flop may be monitored at this point using TP1, TP3, TP7, TP10, or TP12 for the ground reference.

5. TP7-TP8 Strap

   TP7-TP8 must always be left unstrapped for this system.

6. TP9-TP10 Strap

   TP9 and TP10 must always be strapped for this system.

7. UCE Lamp Reset (TP11 and TP12, Sheet 7)

   The UCE lamp may be reset by momentarily shorting TP11 and TP12. This feature must be used only by trained personnel.

13.1.4 LBC LED Indicator Information

The following LED indicators are located on the front edge of the 35-771F04 LBC board:

1. P5U Indicator

   The P5U indicator lights whenever the P5U supply is active. The P5U supply remains active at all times unless the REMOTE POWER switch (X5) or the MAINTENANCE RESET switch is placed to the OFF position. Before removing the LBC board or STMs, verify that the P5U LED is extinguished and that the KEY switch on the System Control Panel (SCP) is in the OFF position.

2. Uncorrectable Error (UCE) and Module Identification Indicators

   The Uncorrectable Error (UCE) indicator lights whenever a Storage Module (STM) outputs a data word containing a detectable multiple bit error. When the UCE indicator is lit, the module ID indicators contain the 256 kb module address where the last Read error occurred.

The UCE indicator remains lit until the SCP INITIALIZE switch is depressed, until the KEY switch is placed in the OFF position, until an REL instruction is executed, until a Read is executed to nonpresent memory, or until TP11 and TP12 are shorted. When the UCE indicator is off and the module ID indicators are on, they indicate a memory access was made to the module specified by the lamps, but the system is not equipped with that module.

13.2 FUNCTIONAL ANALYSIS

13.2.1 Refresh

Refer to Figures 13-1 and 13-2 for refresh timing information. The Storage Modules (STMs) utilize MOS dynamic Random Access Memories (RAMs) which require periodic refresh cycles at each of the 128 row address locaticns every two milliseconds. This is accomplished by executing a single refresh cycle every 16 microseconds (cycle steal mode) or a 128 refresh cycle burst every two milliseconds (burst mode). During any refresh cycle, every memory chip within the system is selected and refreshed at the same row location.

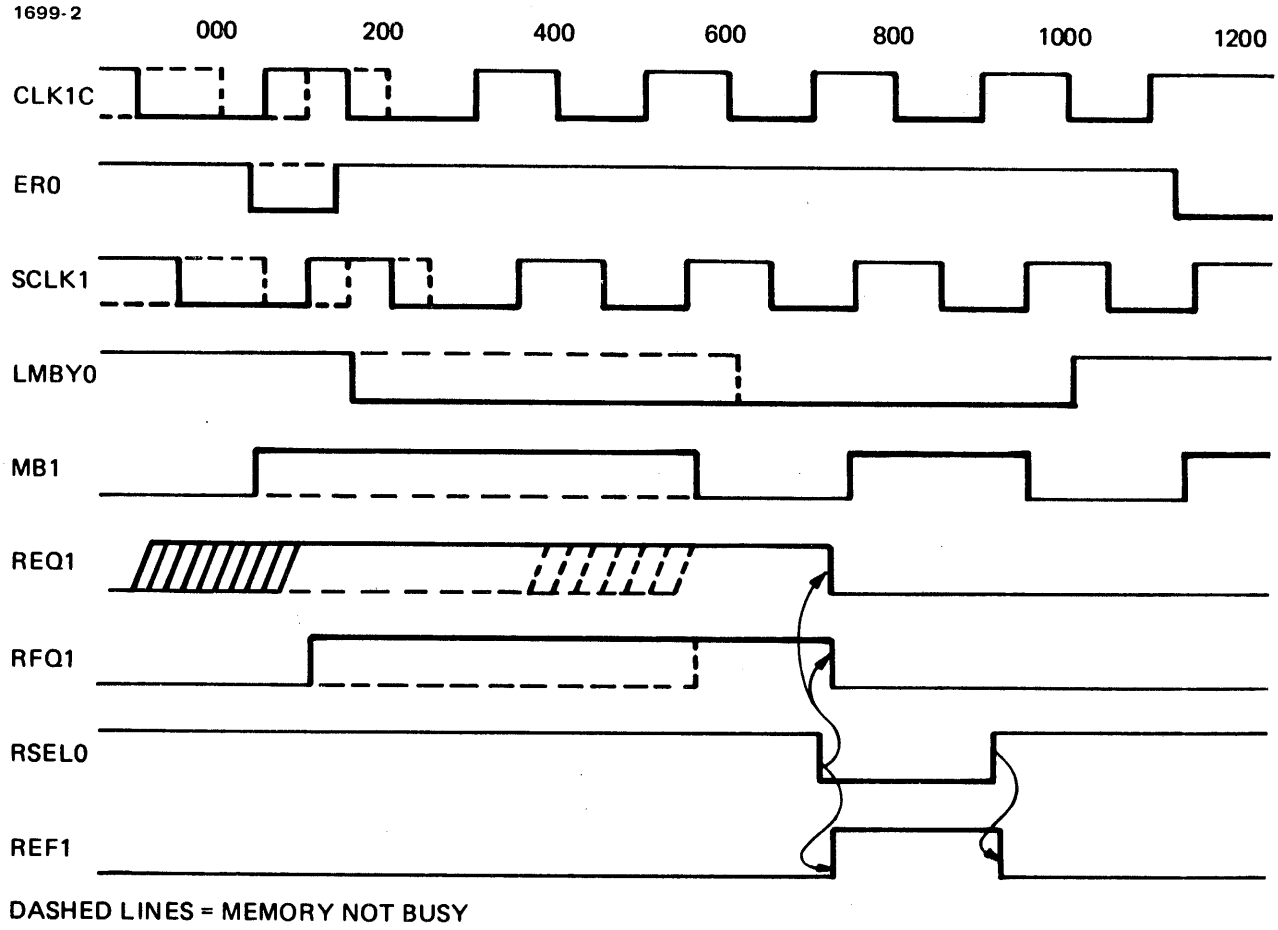


Figure 13-1 Refresh Cycle Steal Timing

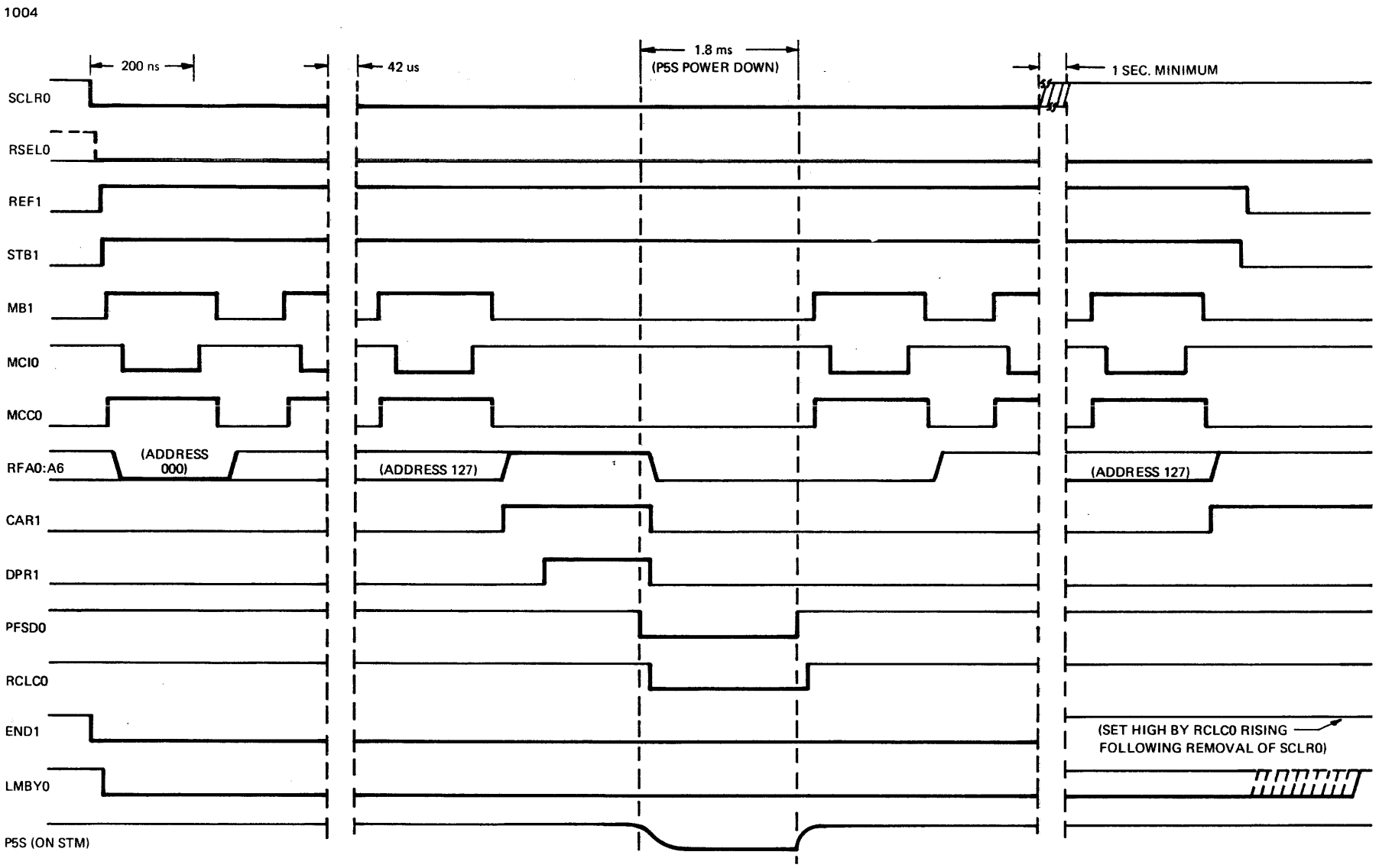


Figure 13-2 Burst Refresh Timing (128 Cycles)

13.2.1.1 Burst Mode

The burst mode is entered whenever the consolette INITIALIZE switch is depressed or the KEY switch is placed to the OFF position, causing the System Clear (SCLR0) line to go active. SCLR0 (13C3) causes REF1 (13C3) to go active, enabling the refresh address driver 11C (3M2) and setting the MB1 flip-flop. MB0 sets the TA001 flip-flop (16B6), starting the TA timer, which causes MCI0 (16S5) to go active and initiate the refresh cycle to the STM(s). With MREF0 (9G5) active, all STMs in the system are enabled to perform the refresh cycle (refer to the chapter on the STM for a detailed description).

When TA201 (13G8) goes high, the refresh counter (13J5 and 13M5) is advanced and the MB1 flip-flop (13K7) is cleared. This causes MCC0 (9G2) to go active, ending the first refresh cycle. When TA181 (13G8) goes low, the MB1 flip-flop (13K7) is directly set, starting the next refresh cycle. This mode of operation continues for 256 cycles allowing the DPR1 flip-flop (13J2) to be clocked set and PFSD (13N2) to be activated. PFSD0 (9R4) going active causes the STM(s) P5S regulator to shut down, placing it into a low power standby mode and activating RCLC0 (9N5). RCLC1 (13E4) causes the refresh counter (13J5 and 13M5) and the DPR1 flip-flop (13J2) to be cleared, allowing the 1.8 ms one-shot (13M2) to time out and deactivate PFSD1. PFSD0 (9R4) going inactive causes the STM(s) P5S regulator to turn on, deactivating RCLC0 (9N5), thereby setting the MB1 flip-flop (13K7) and initiating a 128 cycle burst. A 128 cycle burst is then performed every 1.8 msec.

This mode of operation continues until SCLR0 is brought high by returning the System Control Panel KEY switch to the ON position and timing out the initialize function. This causes the END1 flip-flop (13F5) to be clocked set after completing a 256-cycle burst, allowing the STB1 flip-flop (13H1) to be clocked reset at the end of that burst. STB1 going low causes REF1 (13K3) and REF0 (13L3) to go inactive, allowing LMBY0 (15N8) to be returned high, indicating to the processor that the memory is ready to accept a command. Memory refreshing is continued by performing a single refresh cycle steal every 16 microseconds.

13.2.1.2 Cycle Steal Refresh

A refresh cycle steal is initiated whenever the free-running 16 microsecond oscillator (13B2) clocks the REQ1 flip-flop (13D2) set, thereby allowing the RFQ1 flip-flop (15K7) to queue up this request. Flip-flop 07A (13E2) and the RSEL0 flip-flop (13F2) are used to further synchronize the start and end of the refresh cycle to prevent overlapping of memory operations. Operation in the refresh cycle steal mode is identical to the burst refresh cycle, with the exception that only one cycle is executed and the DPR1 flip-flop (13J2) is never activated.

13.2.2 LBC Operating Modes

The LBC operates in a number of different modes (refer to Table 13-2) as determined by the states of ROM data lines RD011:031 (3E7), WRT0 (3A6), DMAHW0 (3A6), PSEL1 (3A6) and LMA190 (3A5) at the time ERO (13G7) goes active. These signals are loaded into transparent latches whose outputs drive the mode selector logic consisting of one of eight decoders 20F (14C3) and 20J (14C5) and miscellaneous gate functions (left half of Sheet 14). For any given operation, certain mode decoder outputs go active (refer to Table 13-2), setting up the control logic for the specific data manipulation required.

TABLE 13-2 LBC OPERATING MODES

1873-1

MATRSD0	MATRSR0	DRST0	PSELIA	WRT0	RD 011	RD 021	RD 031	PROCESSOR OPERATIONS	MODE DECODER OUTPUTS ACTIVE (See Sheet 14 35-771D08)
1	1	1	1	0	0	0	0	No Memory Operation	
1	1	1	1	0	0	0	1	Store Byte	SBY1, SPW1, SPW0
1	1	1	1	0	0	1	0	Store Halfword (Privileged)*	SHW1, SPW1, SPW0
1	1	1	1	0	0	1	1	Store Halfword (Data)*	SHW1, SPW1, SPW0
1	1	1	1	0	1	0	0	Test Error Logger (Store Byte)	TEL0, TEL1, SBY1
1	1	1	1	0	1	0	1	No Memory Operation	
1	1	1	1	0	1	1	0	Store Fullword (Privileged)*	SFW1, SFW0
1	1	1	1	0	1	1	1	Store Fullword (Data)*	SFW1, SFW0
1	1	1	1	1	0	0	0	No Memory Operation	
1	1	1	1	1	0	0	1	Read and Set Halfword	RST0, RST1, SPW1, ROAST1
1	1	1	1	1	0	1	0	Read Halfword (Privileged)* (Fullword Operation)	PRFW0, PRFW1, RFW1, ROAST1
1	1	1	1	1	0	1	1	Read Halfword (Data)* (Fullword Operation)	PRFW0, PRFW1, RFW1, ROAST1
1	1	1	1	1	1	0	0	Read Error Logger	EL0, REL1 (active with LMA190 high), ELST1 (active with LMA190 low)
1	1	1	1	1	1	0	1	Read Fullword (Instruction Read)*	PRFW0, PRFW1, RFW1, ROAST1
1	1	1	1	1	1	1	0	Read Fullword (Privileged)*	PRFW0, PRFW1, RFW1, ROAST1
1	1	1	1	1	1	1	1	Read Fullword (Data)*	PRFW0, PRFW1, RFW1, ROAST1
			PSELIA	WRT0	DMAHW0			DMA Operations	
1	1	1	0	0	0			Store Halfword	SHW1, SPW1, SPW0
1	1	1	0	0	1			Store Fullword	SFW1, SFW0
1	1	1	0	1	0			Read Halfword (Fullword Operation)	DRFW0, DRFW1, RFW1, ROAST1
1	1	1	0	1	1			Read Fullword (Fullword Operation)	DRFW0, DRFW1, RFW1, ROAST1
1	1	0						DMA Read and Set	DRST0
1	0	1						MAT Read and Set Reference Bit	MATRSR0
0	1	1						MAT Read and Set Dirty Bit	MATRSD0

*LBC does not differentiate between privileged and data instruction.

There are five basic functional modes used by the LBC to service all operations. They are:

1. Store Fullword (Figure 13-3)
2. Store Partial Word (Figure 13-4) including:
   - store byte
   - store halfword
   - read and set
   - test error logger
3. Read Fullword or DMA read (Figure 13-5)
4. Read Error Logger Status (LMA190 low) (Figure 13-6B)
5. Read Error Logger (LMA190 high)

   (Refer to Figure 13-6A)

NOTE

All read halfword operations are decoded as read fullword operations by the LBC. Data steering for halfword operations is performed on the CPU-C board.

1701-2

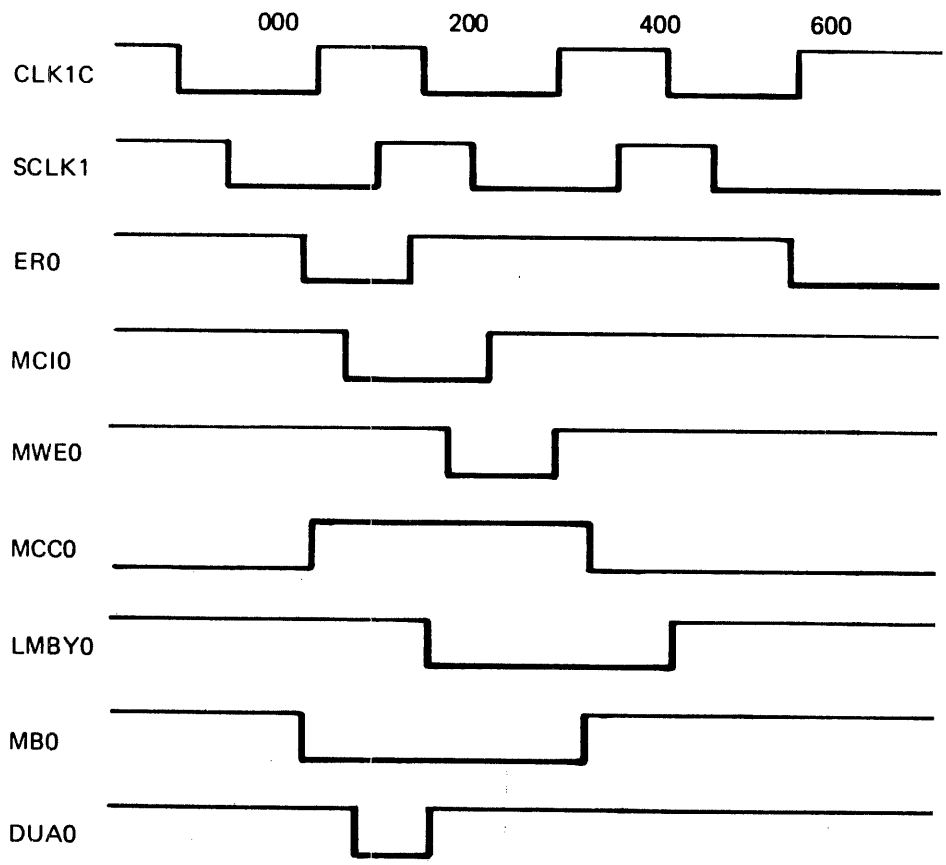


Figure 13-3 Store Fullword

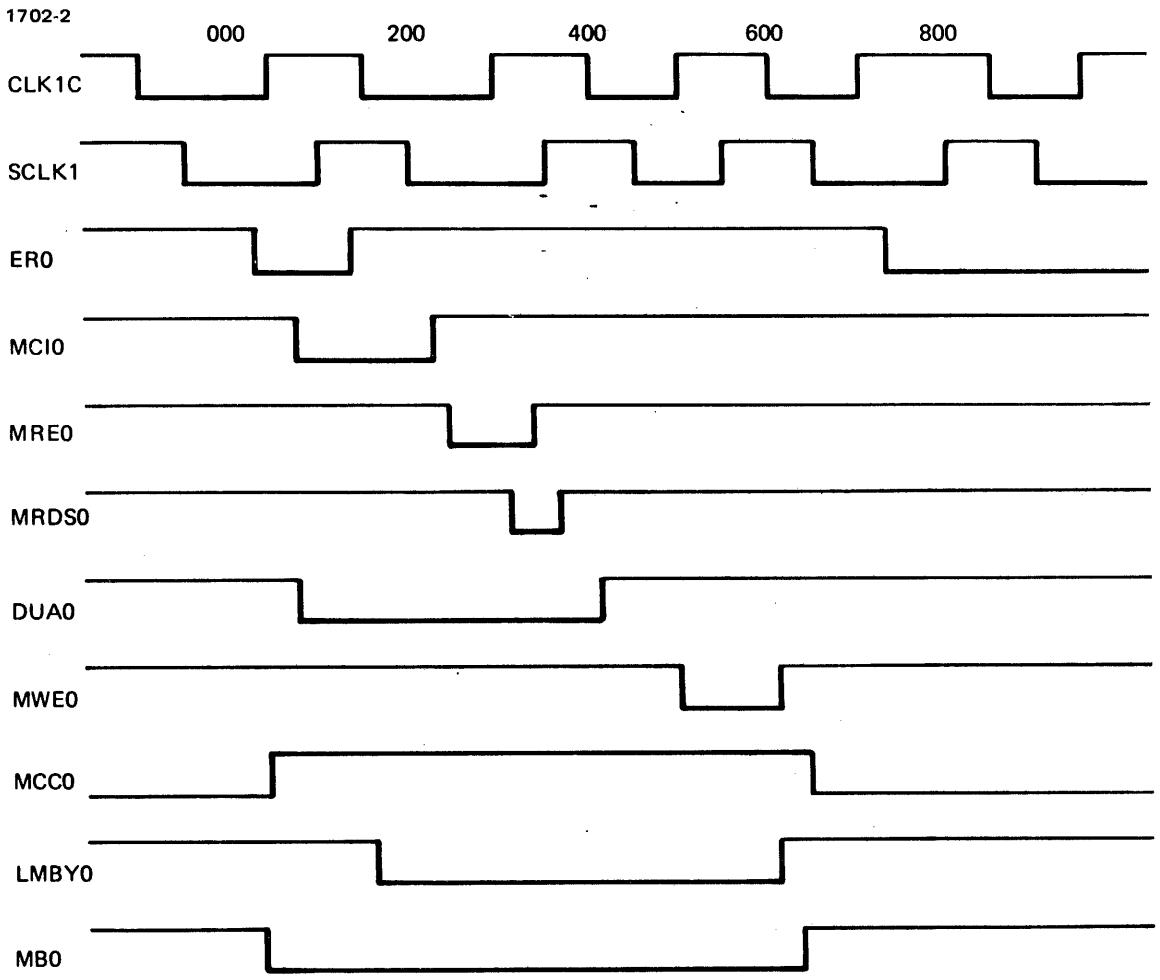


Figure 13-4 Store Partial Word

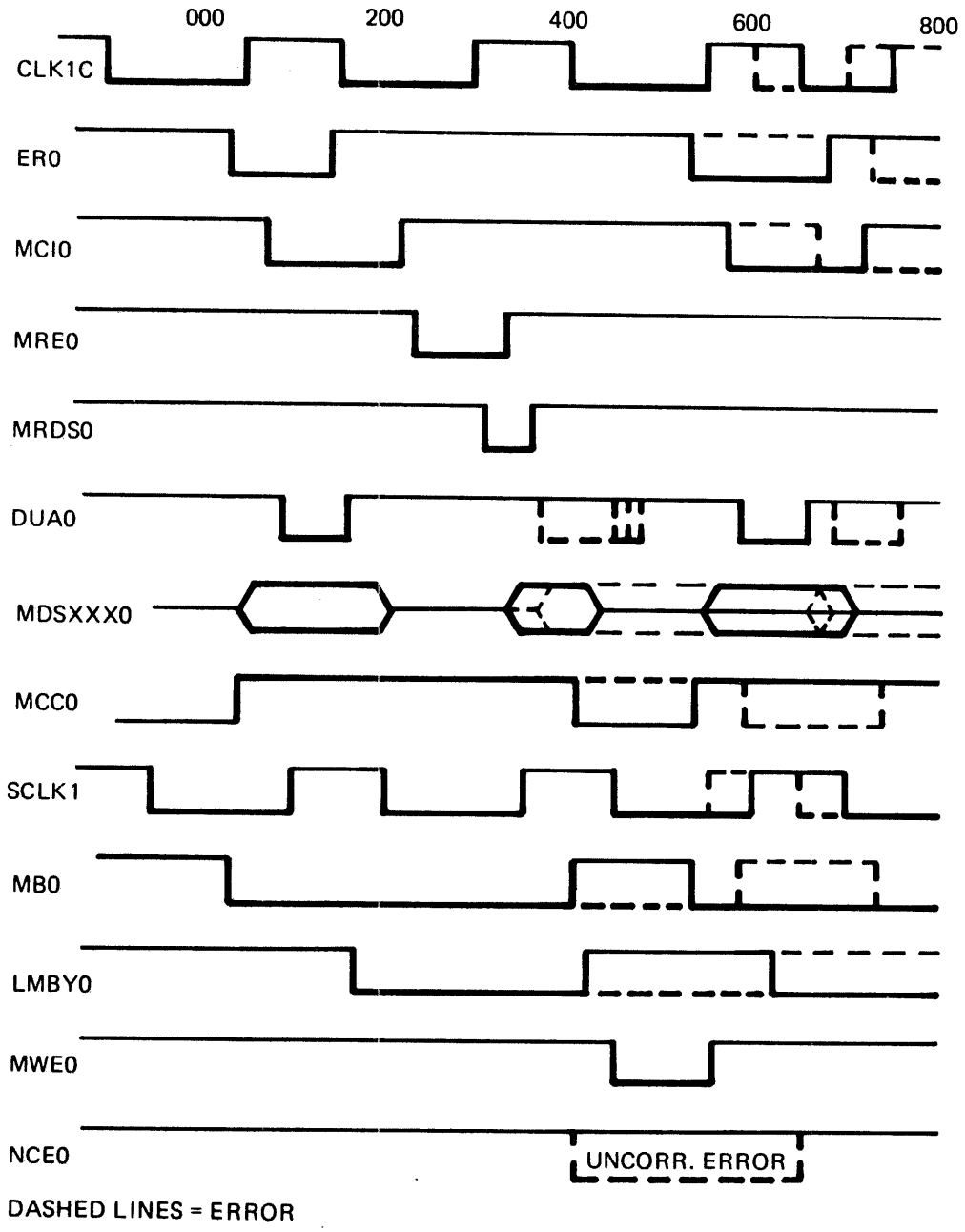
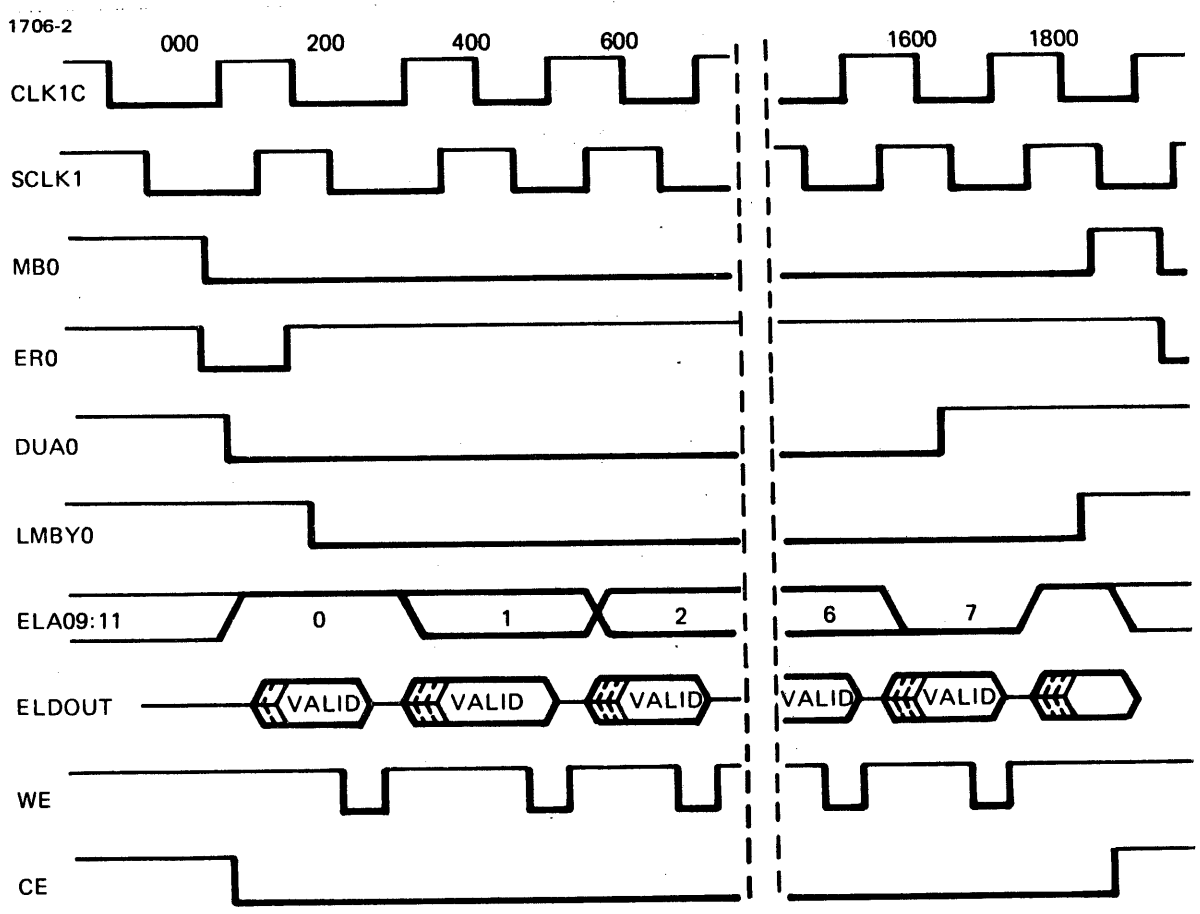
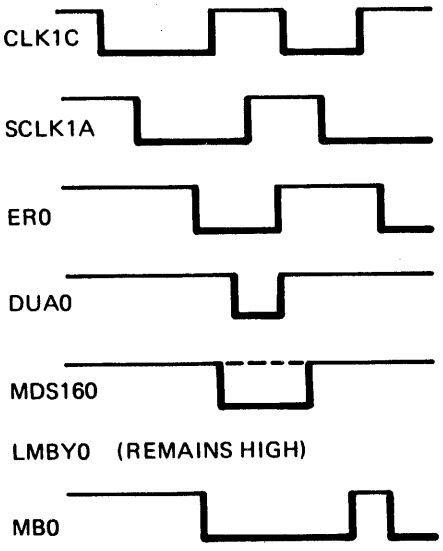


Figure 13-5 Read Fullword



A. Read Error Logger



B. Read Error Logger Status

Figure 13-6 Read Error Logger Status

Timing diagrams for the A and B timers are provided in Figures 13-7 and 13-8. Table 13-3 provides data and address bus alignment information. The subsequent sections describe each of the five basic functional modes.

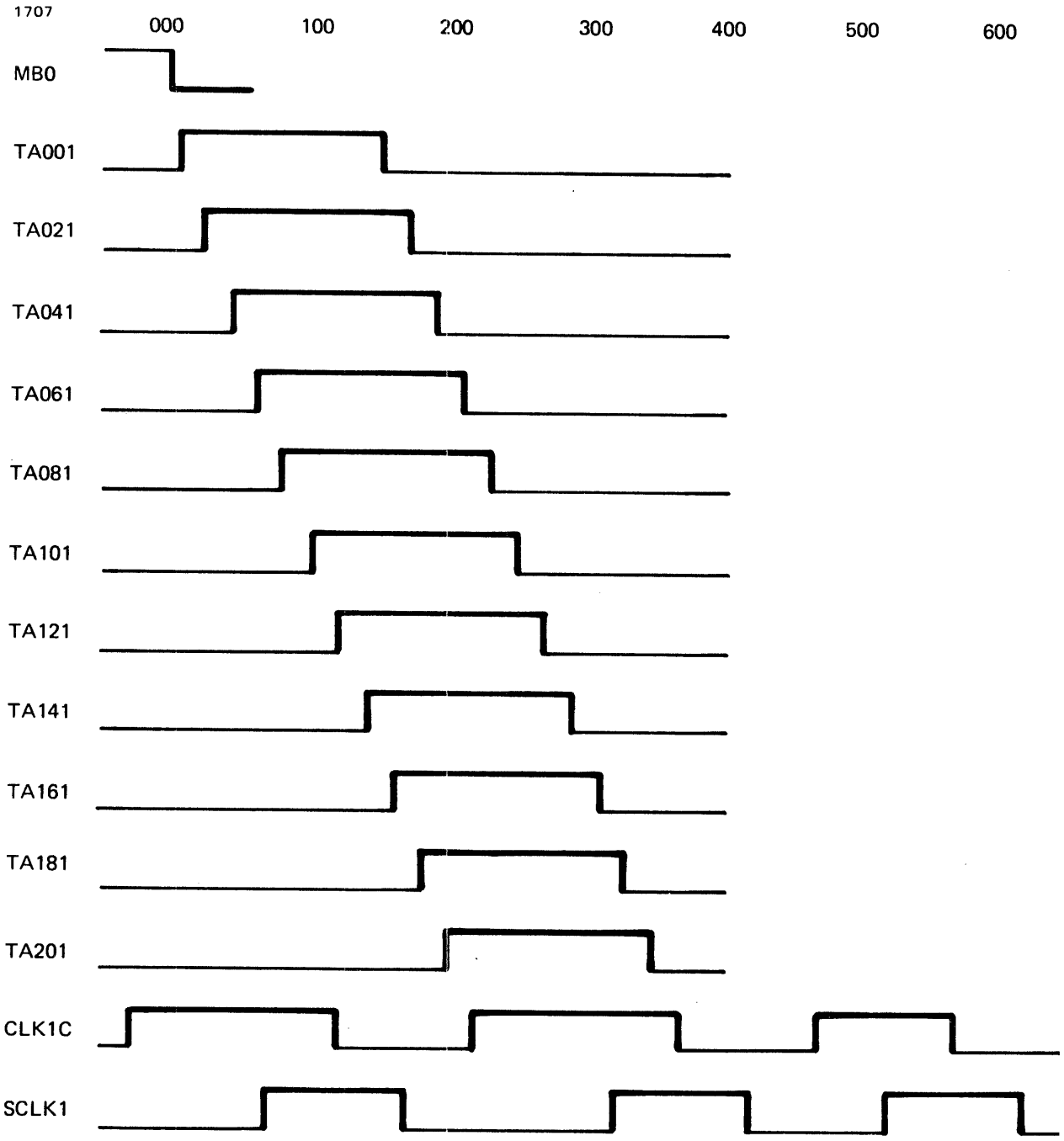


Figure 13-7 A Timer

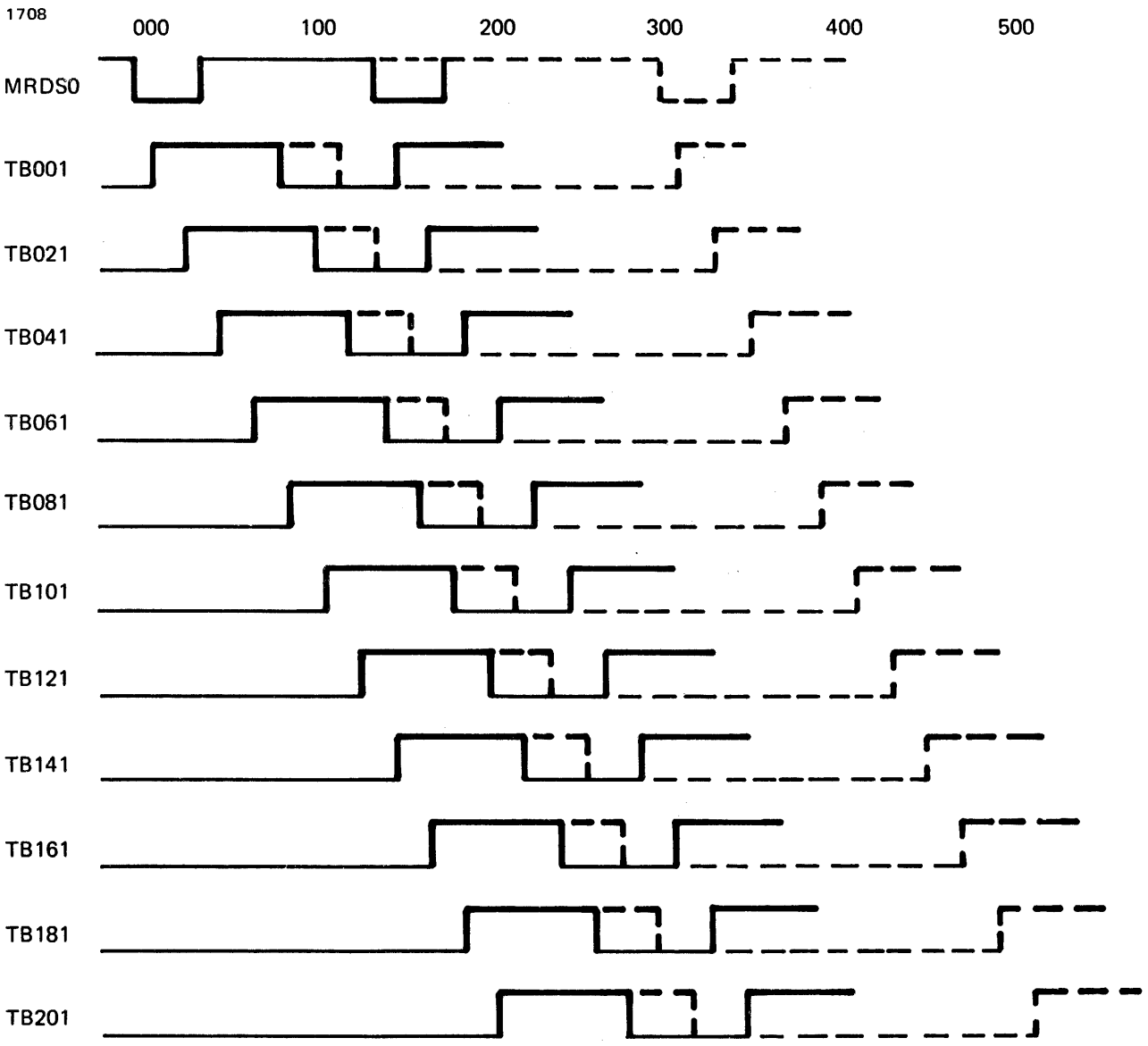


Figure 13-8 B Timer

TABLE 13-3 MEMORY SYSTEM DATA AND ADDRESS BUS ALIGNMENT

1874-1

LMA	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	DATA
LMB							00 REF0	01 1	02 2	03 3	04 4	05 5	06 6	07	08	09	10	11	12	13	14	15			16 → 31 32 → 38
							← REFRESH ADDRESS →																		
35-764F02 (STM)			MEA0	1	2	BLK															MWA 000	MWA 010			
ERROR LOG ADDRESS & STATUS BIT			0	1	2	3	4	5	6	7	8														
			MOD. NO./BLK				WORD COLUMN LMA 28	LMA 29	S0	S1	S2	ST. BIT													
A BUS	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
MDS							0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15			16 → 31
ERROR LOG DATA																									16 → 31
ERROR LOG STATUS BIT																									ST. BIT
ELA ADDRESS BUS			A 10	A 11	A 12	A 13	ELA 04	ELA 05	ELA 06	ELA 07	ELA 08	ELA 09	ELA 10	ELA 11	ELA CE										
EL WRITE ADDRESS			A 10	A 11	A 12	A 13	WA 0	WA 1	S 0	S 1	S 2	S 3	S 4	S 5	S 6										
EL READ ADDRESS			A 10	A 11	A 12	A 13	A 14	A 15	A 16	A 17	A 18	A 19	AD 2	AD 1	AD 0										

13.2.2.1 Store Fullword

A store fullword cycle is initiated at the processor by setting up the write data lines MDS000:310 (2A4), address lines LMA080:310 (3A1-3A9), write control line WRT0 (3A6), and mode control lines DMAHW0 (3A6), PSEL1, and RD011:031 (3A7). After these lines are set up, the processor generates an ER0 (13G7), clocking the MB1 flip-flop set, thereby starting the memory cycle. MB1 going active causes write data to be latched in the input data register (2G8), addresses to be latched in the address register (3A), and the control lines in their respective registers (3A6). MB0 having set the TA timer flip-flop (16B6) causes MCI0 (16S5) to go active, latching up the address presented on LMB001:151 (3E5,3K2) into the STM selected by lines MEA030:000 (9G). After satisfying the STM address hold time, the EA0 flip-flop (16R5) is set, thereby tristating the LMB001:151 address drivers (3E5,3K2). TA101 (2R4 and 15B2) going active enables the input data register (2G8) and the data bus drivers (Sheets 8 and 9), placing the word to be written onto lines D000:310 and LMB000:310. Lines D000:310 are input to the parity generators (4C5,4F5), whose outputs P000:060 propagate through the write parity register (7F7) onto lines GP000:060. This causes the parity data to be placed onto lines LMB321:381 by the parity data drivers (9E8). TAA121 (15A4) causes WE0 to go low, activating MWE0 (9G3), allowing the data present on lines LMB001:381 to be written into the selected STM. Following the removal of WE1 (14J3), NCLR1 (14R4) goes active, clearing the MB1 flip-flop (13K7) which enables MCC0 (9G2). With MCC0 activated, the write cycle is completed and CLK0D (15M9) causes LMBY0 to go high, signaling to the processor that the memory is no longer busy.

13.2.2.2 Store Partial Word

A store partial word cycle is initiated in the same way as described in the store fullword description. The cycles differ in that the word to be modified must be read from the STM before performing the write. This is necessary to allow new parity data to be generated from the modified word. The following description continues from the point just prior to enabling the input data register, as described in the store fullword operation.

WDEN0 (2R4) going active enables the input data register (2G8), placing the byte (store byte operation or test error log operation) or halfword (store halfword operation) of write data onto data lines D000:310. WDEN0 (14K9) also activates LDBY01:31, causing D000:310 to be loaded into the Good Data Registers (GDR) (Sheet 6).

NOTE

WDEN0 does not go active during a read and set operation.

TA161 (15G1) going active sets the RE1 flip-flop (15J3) which, in turn, activates the Uncorrected Data Register (UDR) (Sheets 8 and 9) and MRE0 (9G1). The STM responds in 240 nanoseconds by activating MRDS0 (9G6), signaling that lines LMB001:381 have been loaded with the read data. RDS0 causes the RE1 flip-flop (15J3) to be reset, removing MRE0 (9G1), latching the UDR (Sheets 8 and 9) and starting the TB timer (16B2). Data lines D000:310 and UP000:060 propagate through the parity checkers (Sheets 4 and 5), generating the Error Check and Correction (ECC) syndrome code on lines P000:060. If no data bit errors are generated, the syndrome code lines are all low deactivating MER0 (5N2). If a single data bit is in error, MER0 goes low along with one output from the DC error decoder (5J8) and one output from the DA or DB error decoder. One of the correction lines EB000:310 (Sheet 6) or EPB000:060 (7C4) goes high, causing the data bit in error to be input to the GDR (Sheet 6) or Good Parity Register (GPR) (7F4) to be corrected (inverted). If any two data bits are in error, MER0 goes low, correction lines EB000:310 and EPB000:060 remain low (no correction), and the uncorrectable error decoder (7M5) goes low allowing the UCE0 flip-flop (7N4) to be activated. UCE0 at AOI gate 20K (15B2) prevents activating ED1 and ED0 when the modified word is written back into the STM, causing all logical ones to be stored in the STM. This is necessary because the new parity data generated could otherwise make the data appear error free on subsequent reads from this location. TB021 (14G9) going active causes LDGP1 (read and set or test error logger operation only) and select LDBY01:31 lines (14M7) to go active, thereby loading the part of the word not to be modified into the GDRs (Sheet 6). TB080 (14G9) going low deactivates LDBY01:31 and UDD0 (15L4) and activates GDD1 (15N4), placing the modified word onto lines D000:310 (Sheet 6). New parity data is generated from this word and appears on lines P000:060 (Sheets 4 and 5) which are loaded into the write parity register (7F7) and output on lines GP000:060.

NOTE

A test error logger operation does not store away new parity data, but it uses the old parity by enabling the GPR (7F4) onto lines GP000:060.

A read and set operation differs from the above description in that the entire word from the STM is loaded into the GDR and, in turn, output to the processor from the output data register (see read fullword operation for description). Additionally, the most significant bit of the halfword D000 or D160 (15G6), as addressed by LMA140, is set on write data line D000A or D160A (15K6) if MATRS0, DMARS0, or RST0 are activated. D020A is set on write data line D020A if MATRSD0 is activated.

TBB141 (15A2) activates ED1 and ED0, placing the modified word data and parity data onto lines LMB001:381 (Sheets 8 and 9). TB161 (15A4) causes WE0 and MWE0 (9G3) to go active, placing the

STM in the write mode. WE1 (14J3) going inactive causes NCLR1 (13G9) to reset the MB1 flip-flop (13K7), enabling MCC0 (9G2). LMBY0 (15N8), having gone high at the previous edge of CLK0D, signals to the processor that the cycle is complete and the memory is no longer busy.

A DMA read and set and MAT read and set operation is similar to a regular read and set operation, except that only bit 0 is set.

A MAT read and set dirty bit is also similar to a regular read and set operation except that bit 2 is set.

13.2.2.3 Read Fullword

A read fullword operation begins with the processor setting up the address bus and control lines to their appropriate states followed by the initiation of the cycle with ER0 (13G7) being activated. ER0 sets the MB1 flip-flop (13K7), causing the address register (3B) and control registers (3B, 3E) to be latched and the TA timer flip-flop (16B6) to be set. Lines MX011:031, LMB001:151, and MEA000:030 (Sheet 9) are presented with the address which is latched into the selected STM by MCI0 (16S5). After satisfying the STM address hold time, EA0 (16S4) going active tristates the address drivers (3E5,3J3,9K9).

TA161 (15G1) going active sets the RE1 flip-flop (15J3) which, in turn, activates the UDR (Sheets 8 and 9) and MRE0 (9G1). The STM responds in 240 nanoseconds by activating MRDS0 (9G6) signaling that lines LMB001:381 have been loaded with the read data. RDS0 causes the RE1 flip-flop (15J3) to be reset, removing MRE0 (9G1), latching the UDR (Sheets 8 and 9) and starting the TB timer (16B2). Data lines D000:310 and UP000:060 propagate through the parity checkers (Sheets 4 and 5), generating the Error Check and Correction (ECC) syndrome code on lines P000:060. If no data bit errors are generated, the syndrome code lines are all low deactivating MER0 (5N2). If a single data bit is in error, MER0 goes low along with one output from the DC error decoder (5J8) and one output from the DA or DB error decoders. One of the correction lines EB000:310 (Sheet 6) or EPB000:060 (7C4) goes high, causing the data bit input to the GDR (Sheet 6) or GPR (7F4) to be corrected (inverted). If any two data bits are in error, MER0 goes low, correction lines EB000:310 and EPB000:060 remain low (no correction), and the uncorrectable error decoder (7M5) goes low, allowing the UCE0 flip-flop (7N4) to be activated.

TB080 causes lines LDBY01:31 and LDGP1 (14M6) to load and enable the GDRs (Sheet 6) and the GPR (7F3), placing the data (corrected) onto lines D000:310 and GP000:060. 0DD1 (16N3) going active places this data onto the MDS000:310 lines (2A5) for the processor. If an error has been detected, TBB101 (15A1) activates ED1 and ED0 enabling the write data drivers (Sheets 8 and 9) onto LMB001:381; TEB121 (15A3) activates WE0, enabling MWE0 (9G4); and WE0 (14J3) going inactive causes NCLR1 (13G9) to reset the MB1 flip-flop (13K7). If no errors were detected, NE1

(14J2) going active causes NCLR1 (13G9) to reset the MB1 flip-flop (13K7). CLK0D (15M9) going active with DUA0 inactive raises the LMBY0 line, signaling to the processor that the memory is no longer busy.

13.2.3 Read Error Logger (Including ECC Description)

The error logger consists of a 16k x 1 (four 4k x 1 RAMs) buffer (10L8), an address multiplexor (10E1), a 16-bit shift register (10K1 and 10G2), a shift address generator (10B3), a syndrome code register (10C8), two Error Status flip-flops (10K4), and control circuitry (Sheet 10).

13.2.3.1 ECC Circuit Description

The Error Check and Correction (ECC) circuitry (Sheets 4 through 7) consists of parity/syndrome generators P000:060 (Sheets 4 and 5); error detector MER0 (5M3); first-level error decoders DA0:7, DB0:7, and DC0:7 (5J7); correction bit decoders EB000:160 (Sheet 6) and EPB000:060; uncorrectable error detector (UCE0) with LED display indicator (7M5 and 7R7); and Exclusive-OR bit correction gates (Sheets 6 and 7). The ECC code implemented provides detection and correction of all single-bit errors and detection of all double-bit error combinations.

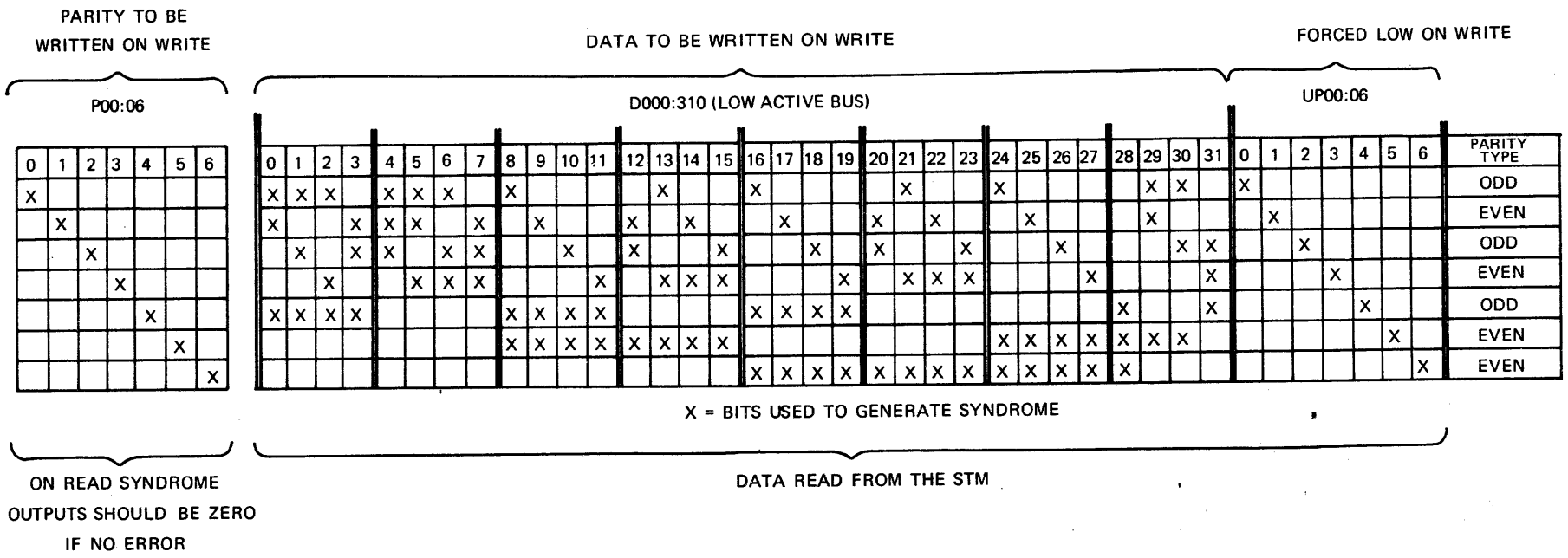
The Error Correction Code (ECC) logic is used to generate the proper parity bits (P00:P06) when writing into the STM (LMB32:LMB37) or to check the 39-bit data word read from the STM.

When writing into memory, the data to be written is available on D00:D31. The seven parity bits (UP00:UP06) are forced low. The resulting parity bit (P00:P06) outputs, along with the 32-bit data word, are written to the STM. (Refer to Table 13-4.)

Reading from the STM fetches a 39-bit data word, which is provided on the inputs of the ECC logic (D00:D31 and P00:06). The syndrome output should be all zero if there is no error. (Refer to Table 13-5.) The syndrome output bits (P00:P06) are decoded to correct any single-bit error. Refer to Table 13-5 for decoding the syndrome bits after a read operation.

TABLE 13-4 ERROR CORRECTION CODE (ECC) LOGIC TABLE

1003



EXAMPLE: DATA TO BE WRITTEN = X'00000000' PARITY GENERATED = 1001000
DATA READ AFTER WRITE = X'80000000' PARITY READ = 1001000 SYNDROME RESULT = 1100100 DATA BIT 0 ERROR (SEE TABLE 13-4)

TABLE 13-5 ECC SYNDROME CODE

S000	S010	S020	S030	S040	S050	S060	ERROR	LOCATION	
0	0	0	0	0	0	0	NE	0	
0	0	0	0	0	0	1	PB6	1	
0	0	0	0	0	1	0	PB5	2	
0	0	0	0	0	1	1	ME	3	
0	0	0	0	1	0	0	PB4	4	
0	0	0	0	1	0	1	ME	5	
0	0	0	0	1	1	0	ME	6	
0	0	0	0	1	1	1	DB28	7	0
0	0	0	1	0	0	0	PB3	8	
0	0	0	1	0	0	1	ME	9	
0	0	0	1	0	1	0	ME	10	
0	0	0	1	0	1	1	DB27	11	
0	0	0	1	1	0	0	ME	12	
0	0	0	1	1	0	1	DB19	13	
0	0	0	1	1	1	0	DB11	14	
0	0	0	1	1	1	1	ME	15	
0	0	1	0	0	0	0	PB2	16	
0	0	1	0	0	0	1	ME	17	
0	0	1	0	0	1	0	ME	18	
0	0	1	0	0	1	1	DB26	19	
0	0	1	0	1	0	0	ME	20	
0	0	1	0	1	0	1	DB18	21	
0	0	1	0	1	1	0	DB10	22	1
0	0	1	0	1	1	1	ME	23	
0	0	1	1	0	0	0	ME	24	
0	0	1	1	0	0	1	DB23	25	
0	0	1	1	0	1	0	DB15	26	
0	0	1	1	0	1	1	ME	27	
0	0	1	1	1	0	0	DB31	28	
0	0	1	1	1	0	1	ME	29	
0	0	1	1	1	1	0	ME	30	
0	0	1	1	1	1	1	ME	31	
0	1	0	0	0	0	0	PB1	32	
0	1	0	0	0	0	1	ME	33	
0	1	0	0	0	1	0	ME	34	
0	1	0	0	0	1	1	DB25	35	
0	1	0	0	1	0	0	ME	36	
0	1	0	0	1	0	1	DB17	37	
0	1	0	0	1	1	0	DB9	38	
0	1	0	0	1	1	1	ME	39	2
0	1	0	1	0	0	0	ME	40	
0	1	0	1	0	0	1	DB22	41	
0	1	0	1	0	1	0	DB14	42	
0	1	0	1	0	1	1	ME	43	
0	1	0	1	1	0	0	ME	44	
0	1	0	1	1	0	1	ME	45	
0	1	0	1	1	1	0	ME	46	
0	1	0	1	1	1	1	ME	47	

TABLE 13-5 ECC SYNDROME CODE (Continued)

S000	S010	S020	S030	S040	S050	S060	ERRCR	LCCATION
0	1	1	0	0	0	0	ME	48
0	1	1	0	0	0	1	DB20	49
0	1	1	0	0	1	0	DB12	50
0	1	1	0	0	1	1	ME	51
0	1	1	0	1	0	0	DB3	52
0	1	1	0	1	0	1	ME	53
0	1	1	0	1	1	0	ME	54
0	1	1	0	1	1	1	ME	55
0	1	1	1	0	0	0	DB7	56
0	1	1	1	0	0	1	ME	57
0	1	1	1	0	1	0	ME	58
0	1	1	1	0	1	1	ME	59
0	1	1	1	1	0	0	ME	60
0	1	1	1	1	0	1	ME	61
0	1	1	1	1	1	0	ME	62
0	1	1	1	1	1	1	ME	63
1	0	0	0	0	0	0	PB0	64
1	0	0	0	0	0	1	ME	65
1	0	0	0	0	1	0	ME	66
1	0	0	0	0	1	1	DB24	67
1	0	0	0	1	0	0	ME	68
1	0	0	0	1	0	1	DB16	69
1	0	0	0	1	1	0	DB8	70
1	0	0	0	1	1	1	ME	71
1	0	0	1	0	0	0	ME	72
1	0	0	1	0	0	1	DB21	73
1	0	0	1	0	1	0	DB13	74
1	0	0	1	0	1	1	ME	75
1	0	0	1	1	0	0	DB2	76
1	0	0	1	1	0	1	ME	77
1	0	0	1	1	1	0	ME	78
1	0	0	1	1	1	1	ME	79
1	0	1	0	0	0	0	ME	80
1	0	1	0	0	0	1	ME	81
1	0	1	0	0	1	0	DB30	32
1	0	1	0	0	1	1	ME	83
1	0	1	0	1	0	0	DB1	84
1	0	1	0	1	0	1	ME	85
1	0	1	0	1	1	0	ME	86
1	0	1	0	1	1	1	ME	87
1	0	1	1	0	0	0	DB6	88
1	0	1	1	0	0	1	ME	89
1	0	1	1	0	1	0	ME	90
1	0	1	1	0	1	1	ME	91
1	0	1	1	1	0	0	ME	92
1	0	1	1	1	0	1	ME	93
1	0	1	1	1	1	0	ME	94
1	0	1	1	1	1	1	ME	95

TABLE 13-5 ECC SYNDROME CODE (Continued)

S000	S010	S020	S030	S040	S050	S060	ERROR	LOCATION	
1	1	0	0	0	0	0	ME	96	
1	1	0	0	0	0	1	ME	97	
1	1	0	0	0	1	0	DB29	98	
1	1	0	0	0	1	1	ME	99	
1	1	0	0	1	0	0	DB0	100	
1	1	0	0	1	0	1	ME	101	
1	1	0	0	1	1	0	ME	102	
1	1	0	0	1	1	1	ME	103	6
1	1	0	1	0	0	0	DB5	104	
1	1	0	1	0	0	1	ME	105	
1	1	0	1	0	1	0	ME	106	
1	1	0	1	0	1	1	ME	107	
1	1	0	1	1	0	0	ME	108	
1	1	0	1	1	0	1	ME	109	
1	1	0	1	1	1	0	ME	110	
1	1	0	1	1	1	1	ME	111	
1	1	1	0	0	0	0	DB4	112	
1	1	1	0	0	0	1	ME	113	
1	1	1	0	0	1	0	ME	114	
1	1	1	0	0	1	1	ME	115	
1	1	1	0	1	0	0	ME	116	
1	1	1	0	1	0	1	ME	117	
1	1	1	0	1	1	0	ME	118	
1	1	1	0	1	1	1	ME	119	7
1	1	1	1	0	0	0	ME	120	
1	1	1	1	0	0	1	ME	121	
1	1	1	1	0	1	0	ME	122	
1	1	1	1	0	1	1	ME	123	
1	1	1	1	1	0	0	ME	124	
1	1	1	1	1	0	1	ME	125	
1	1	1	1	1	1	0	ME	126	
1	1	1	1	1	1	1	ME	127	

NOTE

PB = Parity Bit
DB = Data Bit
ME = Multiple Bit Error

During a faulty read operation, data from the STM is input to the parity check generators causing one or more parity/syndrome lines P000:060 to go high and activating MERO (5N2). These lines are also input to the first level decoders (5J5-5J8), whose outputs are further decoded by the correction bit generators (Sheet 6 and 7C3). If a single-bit error is detected, one correction line EB000:160 or EPB000:060 goes high (active), correcting the bit in error. If the error detected was not a single bit error, lines EB000:160 and EPB000:060 remain low (no correction) causing UCE0 (7N3) to go active and latching the address (1 of 4) of the faulty STM in the uncorrected error display (7R7).

13.2.3.2 Error Logger Description

The error logger records all detectable single and multiple bit memory errors. (Refer to Table 13-5). The error logger is divided in two, with the first half covering the lower 4 Mbs of memory and the other half covering the upper 4 Mbs of memory. The system only uses the first half of the error logger since there can only be 4 Mbs maximum. An error can be detected down to the 16k level.

Errors are recorded as follows: parity/syndrome lines P000:060 are latched in the syndrome register (10C8) whose outputs S001:061 are steered onto error logger address lines ELA04:11, along with the word address lines WA000 and 010, via the address multiplexors (10D1 and 10D3). Line S061 is used, along with BA09, as the error log RAM chip enable (CE) decode. BA09 selects between the lower 4 Mb 4k x 1 RAMS, 17k and 14k (10J6 and 10M6), and the upper 4 Mb 4k x 1 RAMS, 16k and 15k (10J8 and 10M8). S061 selects between the two RAMs selected by BA09, placing all even errors (refer to Table 18-6) into 4k x 1 RAM 17k or 16k, and all odd errors into 4k x 1 RAM 14k or 15k. STM module select lines ELMA11:31 and ERLA01 (10J6, 10J8, 10L6, and 10L8) are input directly to the 4k x 1 RAMs as most significant addresses. ME1 (10H4) and ME0 (10N6), having gone active, cause a low to be written into the address location of the selected RAM, and set either flip-flop 02M (10K4) upper half of the error logger or flip-flop 05K (10K5), lower half of the error logger. These two flip-flops represent the status of their respective error logger halves.

There are two operations provided for obtaining error logger information, read error logger status, and read error logger. Both operations are initiated by sending the read error logger code on lines RD011:31 and setting address bit LMA190 for a read error logger status or resetting address bit LMA190 for a read error logger operation.

A read error logger status operation responds with line MDS160 being set if the error logger contains error information, or reset if no errors have been stored. LMA090 is used to select between the status for each error logger half; if LMA090 is reset, MDS160 returns status for the lower half of the error logger, and if LMA090 is set, MDS160 returns status for the upper

After loading the shift registers, their contents are enabled onto lines D160:310, which output onto lines MDS 160:310 by the output data register (Sheet 2). AD31 (14J2) going active causes NCLR1 (13G9) to reset the MB1 flip-flop (13K7), readying it to accept the next ER0. RCAR0 (10M3), having gone active, allows the ELDUA1 flip-flop to be reset, removing DUA0 (15M8) and causing LMBY0 (15N8) to be deactivated on the next transition of CLK0D.

13.3 MNEMONICS

The following is a list of the mnemonics used on the LBC board. The meaning and 35-771D08 schematic source of each signal are provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
A080:A310	Internal address bus lines	Sheet 3
AD01:AD31	Shift counter bits	10E6
BMCI0	Buffered memory cycle initiate	9R6
BSCLR0	Buffered system clear	9R4
CAR1	Refresh counter carry	13H5
CB011:CB031	Control bits	3G8
CLK0D	Buffered processor clock	10D4
CLK1C	Processor clock	9N8
CLK1D	Buffered processor clock	9S8
CLR0	Cycle steal clear	13D2
CLR0B	Clear DU circuit	15E7
CLTB1	TB timer feedback	16A1
CPER1	Buffered cache parity detect	16R8
CVF1	Clear voltage fail detector	14E8
D000:D310	Internal data bus lines	Sheets 2,6,8, 9,10,11
D000A	Test and set bit	15K5
D160A	Test and set bit	15K6
DA0:DA7	First-level error decode bits	5K6,5K7
DB0:DB7	First-level error decode bits	5K5,5K6
DC0:DC7	First-level error decode bits	5K8,5K9
DERR0	Disable error correction line	5G6
DHW0	Buffered DMA halfword line	3D6
DMAHW0	DMA halfwcrd line	3A6
DPR1	Depower line	13K2
DRFW0/1	DMA read fullword	14E7
DRST0	DMA read and set	14D1
DSFW0	DMA store fullword	14D4
DSHW0	DMA store halfword	14D3
DUA0/1	Data unavailable	15N7

MNEMONIC	MEANING	SCHEMATIC LOCATION
EA0/1	Enable address flip-flop	16S4
EB000:EB310	Data bit correction lines	Sheet 6
ED0/1	Enable data lines	15G1
ELMA00:30	Module address to error logger	3G2,3G3
EL0	Error logger select line	14H5
ELA04:ELA11	Error logger address lines	Sheet 10
ELDUA0/1	Error logger data unavailable	10N4
ELST1	Error logger status select line	14H5
END1	Standby end flip-flop	13F5
EPB000:EPB310	Parity bit correction lines	Sheet 7
ER0	Memory cycle start	13G7
EWE1	End write enable flip-flop	15F3
FNPM0/1	Nonpresent memory flip-flop	14S5
GDD1	Good data disable flip-flop	15N4
GP000:GP060	Good parity lines	7H2,7H4
LD01	Error logger RAM output	10L8
LD02	Error logger RAM output	10R8
LDBY01:LDBY31	Load byte	Sheet 14
LDGP1	Load good parity line	14M5
LDOD1	Load output data register	16K9
LMA080:310	Local memory address lines	Sheet 3
LMB001:381	Local memory bus lines	Sheets 3,8,9
LMBY0/1	Local memory busy flip-flop	15N8
MATRSD0	MAT read and set dirty bit	14D1
MATRSR0	MAT read and set reference bit	14D1
MB0/1	Memory busy flip-flop	13K8
MB0A	Buffered memory busy lines	13N7
MB1A	Buffered memory busy lines	13N7
MB1B	Buffered memory busy lines	13N8
MB1C	Buffered memory busy lines	13N8
MCC0	Memory cycle complete line	9G2
MCI0	Memory cycle initiate line	16R5
MDS000:MDS310	Processor data bus lines	Sheet 2
ME0/1	Memory error flip-flop	15L2
MEA000:MEA030	Memory expansion address lines	9G1,4
MER0	Memory error detect line	15N1,5N2
MER1	Memory error detect line	15F8,5N6
MRDS0	Memory read data strobe	9G6
MRE0	Memory read enable control line	9G1
MREF0	Memory refresh line	9G5
MVF0	Memory voltage fail	9N8
MWA001	Memory word address line	9G3
MWA011	Memory word address line	9G5
MWE0	Memory write enable control line	9G3

MNEMONIC	MEANING	SCHEMATIC LOCATION
NCE0	Noncorrectable error line	9S8
NCLR1	Normal clear line	14R4
NE0/1	No error flip-flop	15N2
NPM0	Nonpresent memory line	14R4
NVAL1	Valid RAM data output	12N3
ODD1	Output data disable	16N3
P000:P060	Parity/syndrome bits	Sheets 4,5
PFSD0/1	P5 shutdown lines	9R4
PRFW0/1	Processor read fullword line	14H5
PSBY0	Processor store byte line	14D2
PSEL1	Processor select line	3A6
PSEL1A	Buffered prccessor select line	3D6
PSFW0	Processor store fullword line	14D4
PSHW0	Processor store halfword line	14D3
PUI0	Power-up initialize line	13F4
QWE0	Quadword enable line	16S7
QWM0/1	Quadword mode lines	16S8
RCAR0	Ripple carry line	10L3
RCLC0/1	STM refresh clear lines	9N5
RCLR0	Internal refresh clear line	13F5,13H4
RCT0/1	Refresh clear time select lines	13G9,13L4
RD011	ROM data line	3E7
RD021	ROM data line	3E7
RD031	ROM data line	3E7
RDS0/1	Buffered memory read data strobe lines	9R5
RE0/1	Read enable flip-flop	15K3
REF0/1	Refresh mode control lines	13N3
REF0A	Buffered refresh mode control line	13J3
REL1	Read error logger line	14H5
REQ1	Cycle steal request flip-flop	13D2
RFA0:RFA7	Refresh address bus	13N5
RFQ1	Refresh queue flip-flop	15L6
RFW1	Read fullword control line	14G6
ROAST1	Read and/or set control line	14H6
RSEL0	Refresh cycle steal select line	13G4
RST0/1	Read and set control lines	14H2
RURE1	Data bus control line	14M7
S000:S060	Syndrome bit lines	10D8,10D9
SBY1	Store byte control line	14H2
SCLK0A	Buffered processor shift clock	10D4
SCLK1	Processor shift clock	9N8
SCLK1A	Buffered processor shift clock	9S7

MNEMONIC	MEANING	SCHEMATIC LOCATION
SCLR0	Systems clear relay contact	13A3
SCLR0A	Systems clear line	13A3
SCLR0B	Buffered systems clear line	13G4
SCLR0C	Buffered systems clear line	13A4
SCLR1B	Buffered systems clear line	13A3
SFW0/1	Store fullword lines	14H4
SHIFT1	Shift register advance line	10L2
SHW1	Store halfword line	14H4
SPW0/1	Store partial word line	14H2
STB0/1	Standby mode flip-flop	13H2
TA001:TA201	TA timer outputs	Sheet 16
TB001:TB161	TB timer outputs	Sheet 16
TEL0/1	Test error logger control lines	14H2
UCE0/1	Uncorrectable error flip-flop	7R4
UDD0/1	Uncorrectable data disable flip-flop	15L3
UFP1	P5U pullup	13F1
UP000:UP060	Uncorrected parity bit lines	9J8
VAL0/1	Valid bit data input	12H1
VF1	Voltage fail flip-flop	13N4
WA000/1	Word address counter bits	3S5
WA010/1	Word address counter bits	3S5
WC0	Word counter carry	3S8
WCC0/1	Word counter carry	3S7
WDEN0	Write data enable line	14M9
WE0/1	Write enable lines	15E3
WRT0	Write control line	13J1
WRT0A	Buffered write control line	3M1
WRT1	Buffered write control line	14A3
XRP1	P5 pullup	15N3
XRP2	P5 pullup	14K3
XRP3	P5 pullup	3S7
XRP4	P5 pullup	10N4

CHAPTER 14
STORAGE MODULE (STM)

14.1 INTRODUCTION

The STM is a random access memory (RAM) using either 16 k or 64 k dynamic MOS RAM chips as the storage element. Depending on the STM's functional variation, the total memory per STM is either 256 kb (F01), 512 kb (F02), 1.024 Mb (F03), or 2.048 Mb (F04). The STM has on-board 4-way interleaving capability. The 39-bit data field is broken into 32 data bits and 7 parity bits. An organization list of the STM variations is shown in Table 14-1. A block diagram of the STM is provided on Sheet 1 of 35-764D08. A description of each block is given in the following sections.

TABLE 14-1 FUNCTIONAL VARIATIONS

PART NO.	VARIATION	MEMORY CAPACITY	ORGANIZATION	STORAGE ELEMENT
35-764	F01	256 kb	64 k x 39	16 k x 1
	F02	512 kb	128 k x 39	16 k x 1
	F03	1.024 Mb	256 k x 39	64 k x 1
	F04	2.048 Mb	512 k x 39	64 k x 1

14.1.1 Module Select

Each STM contains a set of binary coded switches that permit proper selection of that STM when placed in the system. Figure 14-1 shows a component block layout of the STM. Figure 14-2 shows the binary coded switches (module select switches) in more detail. The actual switch settings depend on the memory configuration. Tables 14-2 and 14-3 show the module select switch settings for all possible memory configurations.

14.1.2 Memory Configurations

The basic system contains one LBC and one STM. The single STM can be either a 256 kb (F01), 512 kb (F02), a 1 Mb (F03), or a 2 Mb (F04) module. Referring to Figure 14-1, the only difference

between the four versions of the STM is the number and type of dynamic RAMs placed on the board. The 512 kb (F02) modules contain 16 k, 5 V only RAMs in blocks A, B, C, and D. The 1 Mb (F03) modules contain 64 k, 5 V only RAMs in blocks A and B only. Two (2) Mb (F04) modules contain 64 k, 5 V only RAMs in blocks A, B, C, and D.

Many memory expansions are possible, up to 4 Mb. Tables 14-2 and 14-3 list all the possible combinations of STMs for the memory system.

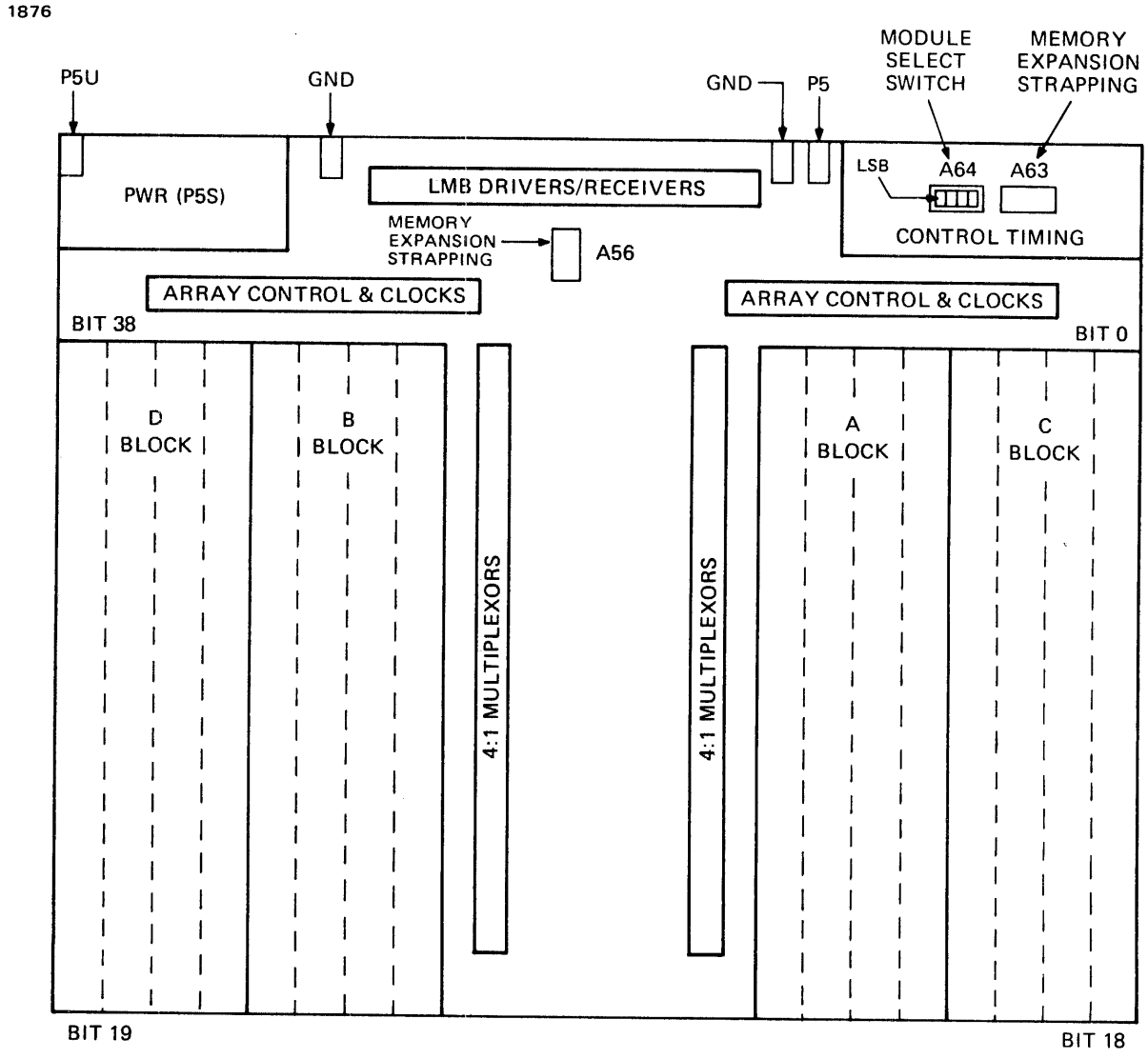
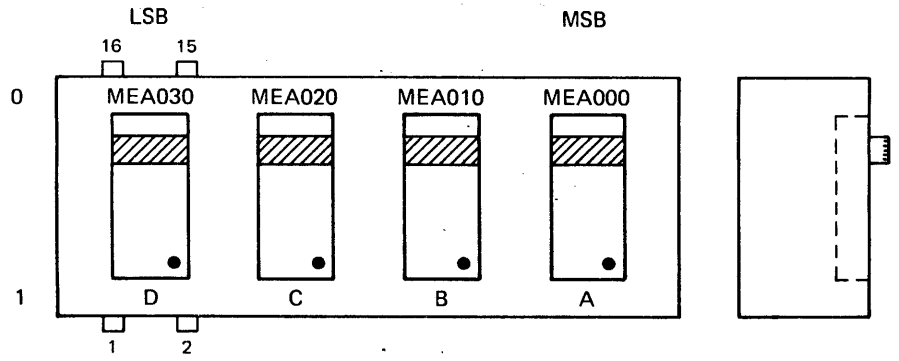


Figure 14-1 STM Component Block Layout

1710-1



NOTE

SWITCH POSITION IS CLOSED ON THE SIDE ON WHICH THE DOT APPEARS.

Figure 14-2 Module Selection Switches

TABLE 14-2 MEMORY CONFIGURATIONS (35-771 LBC)

	CHASSIS SLOT	STM TYPE	MEA030	MEA020	MEA010	MEA000	STORAGE CAPACITY
BASIC SYSTEMS	SLOT 14	F01	0	0	0	0	256 kb
	SLOT 15	(none)	-	-	-	-	
	SLOT 14	F02	X	0	0	0	512 kb
	SLOT 15	(none)	-	-	-	-	
	SLOT 14	F03	X	X	0	0	1,024 kb
	SLOT 15	(none)	-	-	-	-	
	SLOT 14	F04	X	X	X	0	2,048 kb
	SLOT 15	(none)	-	-	-	-	
POSSIBLE EXPANSIONS	SLOT 14	F01	0	0	0	0	512 kb
	SLOT 15	F01	1	0	0	0	
	SLOT 14	F02	X	0	0	0	768 kb
	SLOT 15	F01	0	1	0	0	
	SLOT 14	F02	X	0	0	0	1,024 kb
	SLOT 15	F02	X	1	0	0	
	SLOT 14	F03	X	X	0	0	1,280 kb
	SLOT 15	F01	0	0	1	0	
	SLOT 14	F03	X	X	0	0	1,536 kb
	SLOT 15	F02	X	0	1	0	
	SLOT 14	F03	X	X	0	0	2,048 kb
	SLOT 15	F03	X	X	1	0	
	SLOT 14	F04	X	X	X	0	2,304 kb
	SLOT 15	F01	0	0	0	1	
	SLOT 14	F04	X	X	X	0	2,560 kb
	SLOT 15	F02	X	0	0	1	
	SLOT 14	F04	X	X	X	0	3,072 kb
	SLOT 15	F03	X	X	0	1	
	SLOT 14	F04	X	X	X	0	4,096 kb
	SLOT 15	F04	X	X	X	1	

X means "Don't Care"

TABLE 14-3 MEMORY CONFIGURATIONS (35-806F02 LBC*)

	CHASSIS SLOT	STM TYPE	MEA030	MEA020	MEA010	MEA000	STORAGE CAPACITY
BASIC SYSTEMS	SLOT 14	F02	0	0	0	0	512 kb
	SLOT 15	(none)	-	-	-	-	
	SLOT 14	F03	X	0	0	0	1,024 kb
	SLOT 15	(none)	-	-	-	-	
	SLOT 14	F04	X	X	0	0	2,048 kb
	SLOT 15	(none)	-	-	-	-	
POSSIBLE EXPANSIONS	SLOT 14	F02	0	0	0	0	1,024 kb
	SLOT 15	F02	1	0	0	0	
	SLOT 14	F03	X	0	0	0	1,536 kb
	SLOT 15	F02	0	1	0	0	
	SLOT 14	F03	X	0	0	0	2,048 kb
	SLOT 15	F03	X	1	0	0	
	SLOT 14	F04	X	X	0	0	2,560 kb
	SLOT 15	F02	0	0	1	0	
	SLOT 14	F04	X	X	0	0	3,072 kb
	SLOT 15	F03	X	0	1	0	
	SLOT 14	F04	X	X	0	0	4,096 kb
	SLOT 15	F04	X	X	1	0	

X means "Don't Care"

*The 256 kb (F01) STM cannot be used with the 35-806F02 LBC

14.1.3 Memory Cycle Start/End

The memory cycle is initiated by the negative going edge of Memory Cycle Initiate (MCIO) and is disabled by Memory Cycle Complete (MCCO), terminating all memory operations. This block also initiates timing for the row and column address strobes.

14.1.4 LMB Description

14.1.4.1 LMB 001:381

LMB lines 001:381 carry the address, read/write data, to and from memory. During the address time, LMB lines 001:131 carry the row and column address to the RAMs. During the read/write time, LMB lines 001:381 carry the RAM data. Table 14-4 lists the function of each bus line.

TABLE 14-4 BUS LINE FUNCTIONS

LMB	R/W MODE ADDRESS	NAME	REFRESH MODE ADDRESS	R/W DATA
001	Row Add	AC	Ref Address	Data Bit 0
011	Row Add	A1	Ref Address	1
021	Row Add	A2	Ref Address	2
031	Row Add	A3	Ref Address	3
041	Row Add	A4	Ref Address	4
051	Row Add	A5	Ref Address	5
061	Row Add	A6	Ref Address	6
071	Column Add	A7		7
081	Column Add	A8	-	8
091	Column Add	A9		9
101	Column Add	A10		10
111	Column Add	A11		11
121	Column Add	A12		12
131	Column Add	A13		13
141	Chip Row Access (MS)	A14		14
151	Chip Row Access (LS)	A15		15
161	Quad Word Enable	QWE0		16
171	Data			17
181	↓			18
191				19
201				20
211				21
221				22
231				23
241				24
251				25
261				26
271				27
281				28
291				29
301				30
311	↓			31
321	Check Bits			Check Bit 00
331	↓			01
341				02
351				03
361				04
371				05
381	↓			06

MX021 Memory Expansion *Column Address
MX031 Memory Expansion *Row Address

* Expanded address lines for F03, F04 STMs using 64 k RAM chips

14.1.4.2 LMB 001:061

During the address time of the bus function, LMB lines 0:6 contain the address of one of the 128-cell rows within each RAM chip in the array. This address is latched by the STM.

14.1.4.3 LMB 071:131

During address time of the bus function, LMB lines 071:131 contain the address of one of the 128-cell columns within each RAM chip in the array. This address is latched by the STM.

14.1.4.4 LMB 141:161

During the address time of the bus function, LMB lines 141:151 enable access to one of the 4-word rows in either the A or B array. LMB line 161, when low (inactive), enables access to all four rows (quadword) in either array.

14.1.5 I/O Transceiver

The I/O transceiver carries data to and from the array on 39 bidirectional lines. The transceiver is controlled by the mode control circuitry via the Data Out Enable (DOE0) and Data In Enable (DIE0) signals.

14.1.6 Mode Control

The mode control receives Memory Write Enable (MWE0) or Memory Read Enable (MRE0) signals from the LBC and generates Read, Data Out Enable (DOE), or Write, Data In Enable (DIE) signals to the I/O transceiver.

14.1.7 Memory Read Data Strobe

The Memory Read Data Strobe (MRDS0) signal indicates availability of the read data on the LMB lines.

14.1.8 Word Access Decoder

Lines MWA001:011 enable access to one of the 4-word rows in either the A or B array. These lines must agree with LMB lines 141:151.

14.1.9 Strobe Clock Drivers

The address drivers access the storage cell within the selected RAM chip. The Row Address Strobe (RAS) and Column Address Strobe (CAS) clock drivers facilitate the R/W operation of the selected word in either the A or B array.

14.1.10 RAM Chip Array

The RAM chip array is configured in a horseshoe arrangement as shown in Figure 14-3, with one inner 39-bit quadword labeled A array which is divided into two blocks: block A, which consists of bits 0:18, and block B, which has bits 19:38. A complementary outer 39-bit quadword labeled B array is also divided into two blocks: block C, consisting of bits 0:18, and block D, consisting of bits 19:38.

1877

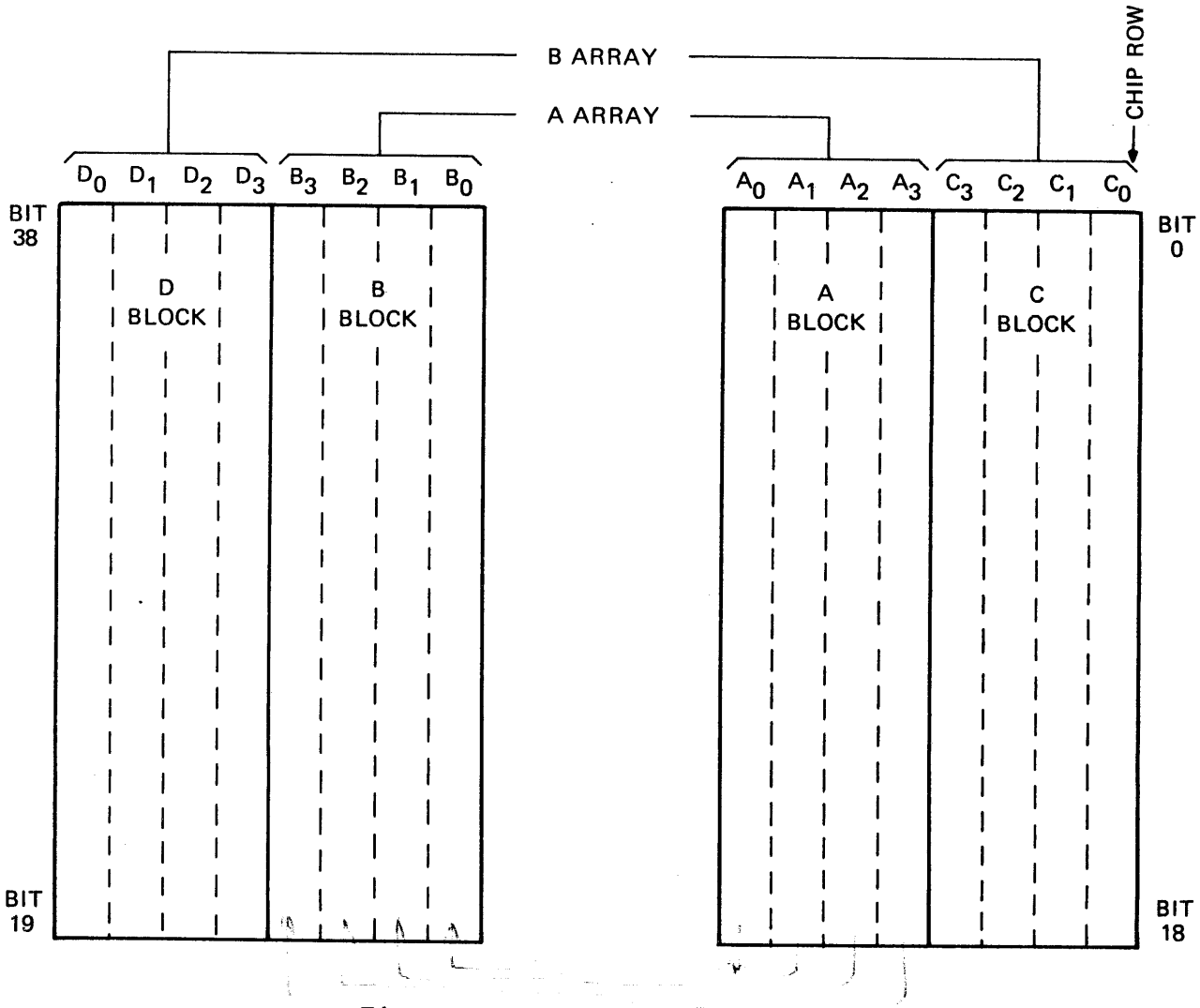


Figure 14-3 RAM Chip Array

14.2 STORAGE MODULE OPERATION

The module select switches and memory expansion straps enable selection of one of the possible 2 STMs. When a module is selected, a high level is generated on (MS1), Sheet 2 (H5). Figure 14-4 depicts module selection and Tables 14-5 and 14-6 contain memory strapping information.

TABLE 14-5 MEMORY EXPANSION STRAPPING (35-771 LBC)

35-764	A56 LCCATION	A63 LOCATION
F01 .256 Mb		12-6
F02 .512 Mb	6-11	12-6 8-9 11-14
F03 1.0 Mb	14-11 10-13	12-6 10-7 8-9
F04 2.0 Mb	14-11 10-13 2-15	8-9 10-7 6-13 11-5

TABLE 14-6 MEMORY EXPANSION STRAPPING (35-806F02 LBC*)

35-764	A56 LOCATION	A63 LOCATION
F02 .512 Mb	12-11	12-6 11-14
F03 1.0 Mb	14-11 10-13	12-6 8-9
F04 2.0 Mb	14-11 10-13 4-15	12-6 8-9 10-7 11-5

* The 256 kb (F01) STM cannot be used with the 35-806F02 LBC.

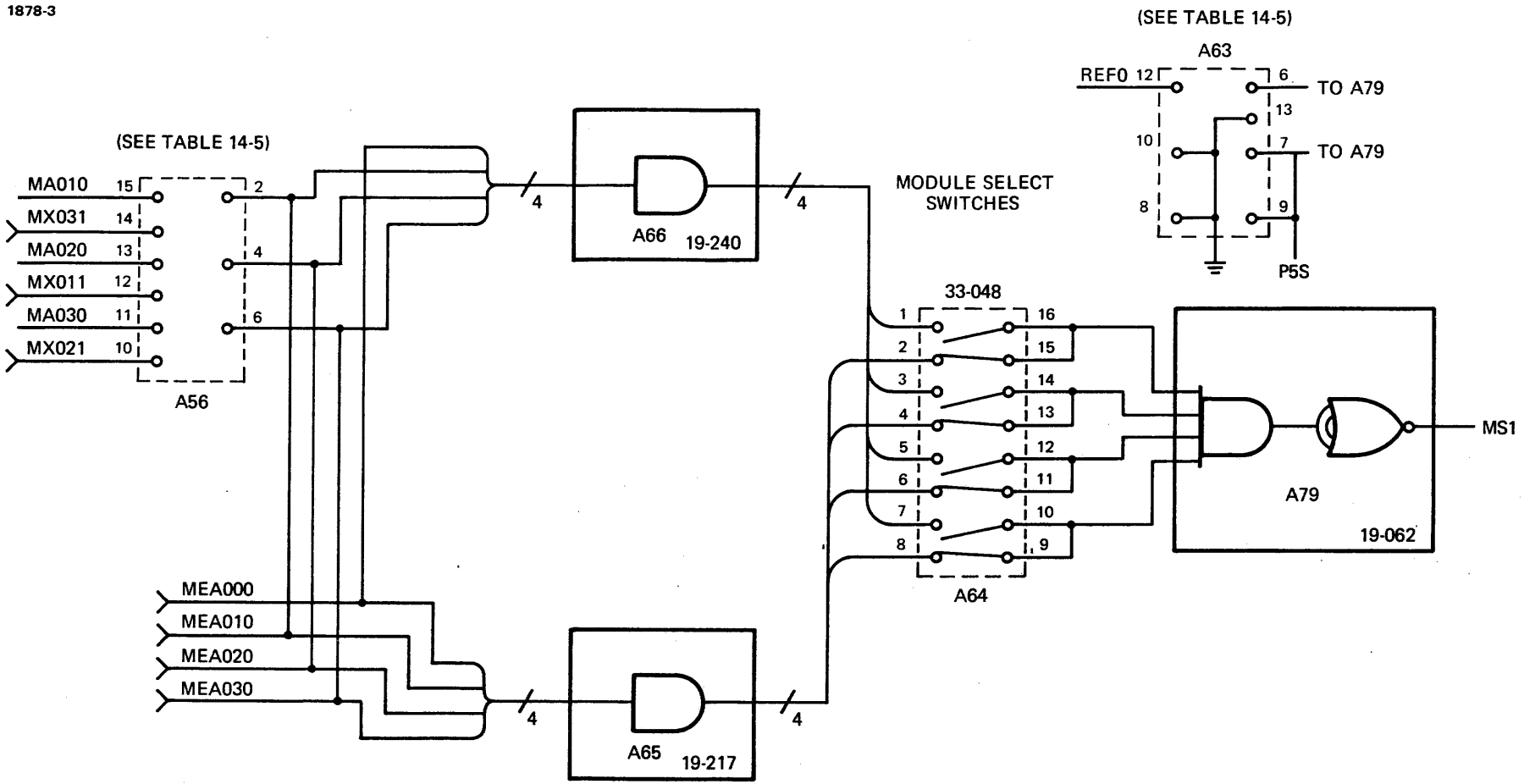


Figure 14-4 Module Select Circuit

14.2.1 Timing

14.2.1.1 Start of Memory Cycle

A memory cycle starts upon arrival of the negative-going edge of (MCI0) as shown in Figure 14-5. Noting that the module has been selected (MS1 is high), MCI0 clocks the memory busy flip-flop (A49) and generates (MB0), which latches the LMB lines 0:16 on the F02 version, as well as MX021 and MX031 on the F03 and F04 versions (3A4). Also generated by the memory busy flip-flop is MB1, which passes through a delay line (A62) and generates the row (RAS) and column (CAS) strobe timing, RAST1 and CAST1.

14.2.1.2 End of Memory Cycle

Every memory cycle ends on the low-going edge of the Memory Cycle Complete (MCC0). MCC0 resets the memory busy flip-flop which disables RAST1 and CAST1, thus completing the memory cycle.

14.2.1.3 Address Latches and Drivers

Upon arrival of MCI0, MB0 goes low and enables the address latches and expansion address (depending on the functional variation of the board) to latch in the row and column addresses (refer to Figure 14-6). LMB lines 141:151 (3A7), which select one of the 4-chip (word) rows (0-3) if a single fullword is desired, are also latched. During the address time, LMB line 161 determines if a quadword is desired. If low, all four rows (words) in the array are enabled, and lines LMB 141:151 are ignored. When the row and column address are propagated through the driving circuitry, the single memory cell in the row or rows is selected.

14.2.1.4 RAS Drivers

The leading edge of MCI0 clocks the Memory Busy flip-flop (A49). MB1 is then passed through a delay line and also propagated through complementary AND gates (A50, A51), which generate RAS timing for both A and B arrays (RASTA1, RASTB1). (Refer to Figure 14-5.) The RAS timing strobes are then propagated through the word row decoding circuitry with the selected word row or rows depending upon the state of A141, A151, and QWE0 at location 3A9. The output of the RAS drivers enables the selected rows of RAMs. All RAS drivers are selected simultaneously during a refresh cycle.

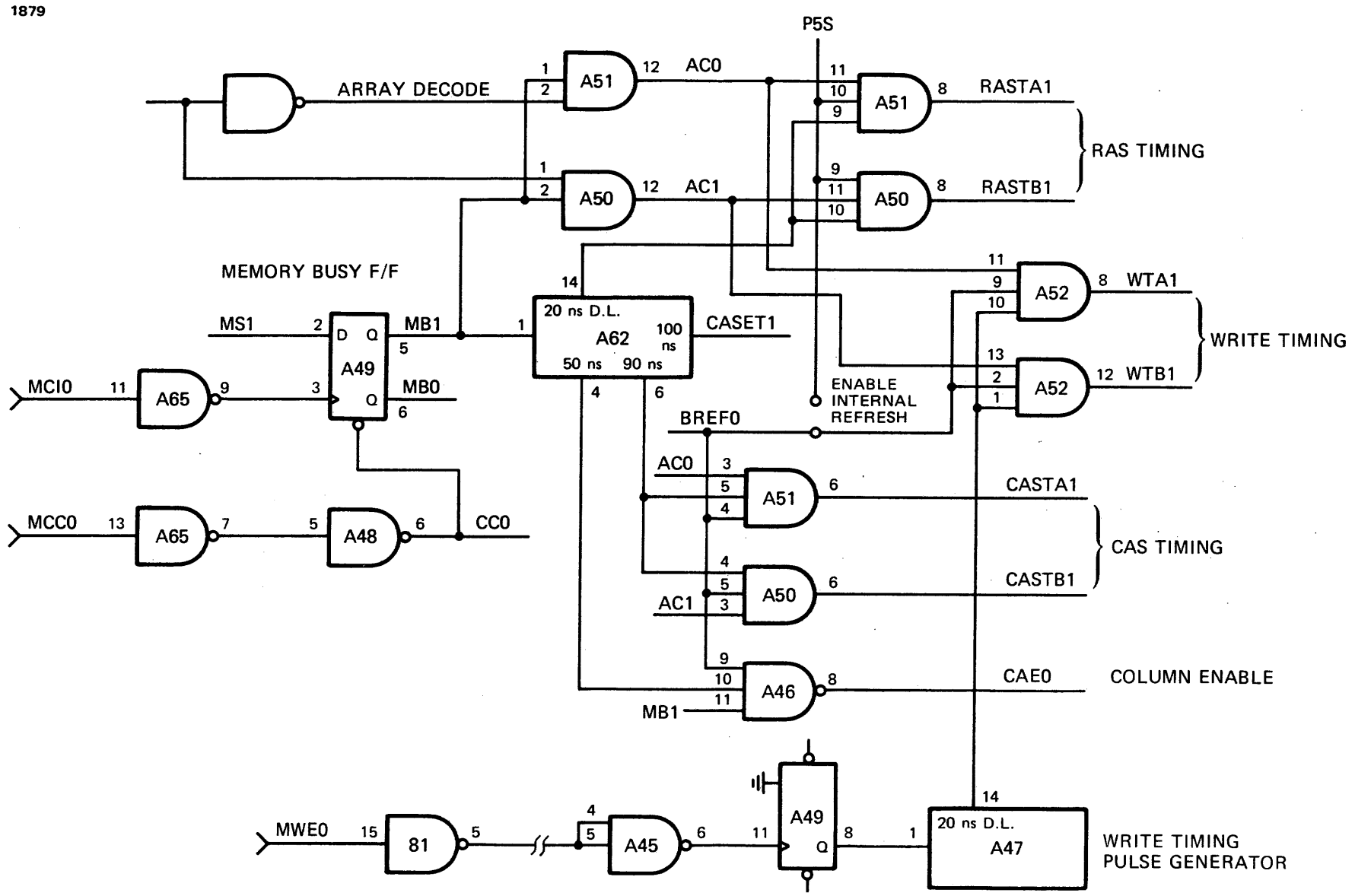


Figure 14-5 Timing Control

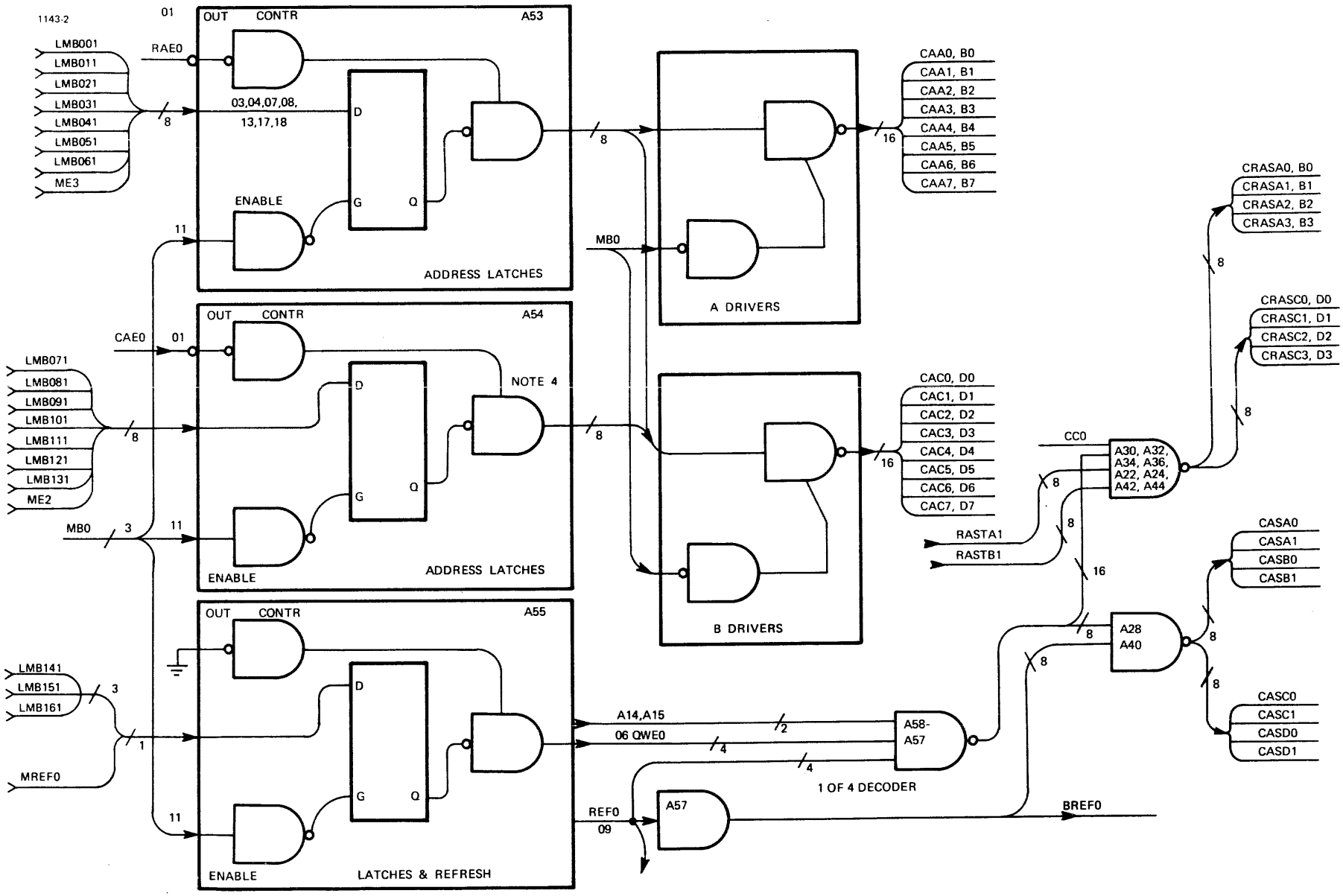


Figure 14-6 Address Latches and Decoder

14.2.1.5 Memory Word Access Decode

Refer to Table 14-7 during this discussion. The Memory Word Access (MWA001:011) lines are similar in function to LMB lines 141:151, which are discussed in the section on address latches and drivers. The lines in the decoder provide access to one of the 4-word rows in the A or B array. The MWA lines generate (WA0) and (WA1). These lines are used to steer the RAST1 and WT1 decoding to one of the 4-word rows during the Read-Modify-Write operation. (Refer to Figure 14-7.)

TABLE 14-7 BLOCK AND ROW DECODE TABLE

STM TYPE	LMB 141	LMB 151	*MX011 **MEA030	*MEA020 **MEA010	BLOCK DECODED	ROW DECODED
***	0	0	X	X		0
	0	1	X	X		1
F01	1	0	X	X	A/B	2
	1	1	X	X		3
	0	0	0	X		0
	0	1	0	X	C/D	1
	1	0	0	X		2
F02	1	1	0	X		3
	0	0	1	X		0
	0	1	1	X	A/B	1
	1	0	1	X		2
	1	1	1	X		3
	0	0	x	x		0
	0	1	X	X	A/B	1
F03	1	0	X	X		2
	1	1	X	X		3
	0	0	X	0		0
	0	1	X	0	C/D	1
	1	0	X	0		2
F04	1	1	X	0		3
	0	0	X	1		0
	0	1	X	1	A/B	1
	1	0	X	1		2
	1	1	X	1		3

* Use MX011 and MEA020 for the 35-806F02 LBC.
** Use MEA030 and MEA010 for the 35-771 LBC.
*** F01 STMs can only be used with the 35-771 LBC.

NOTE

Zero indicates low level (<.8 V at connector).

14.2.1.6 Write Clock Drivers

The MWA lines are used to steer the write timing pulse WTA1 and WTB1 for selection of the appropriate word row to be written into. The word row is selected by the decoding of these strobes and by word select lines WA0 and WA1 and their inverse, which generate a low (active) pulse on the selected CWE line. (Refer to Figure 14-8.)

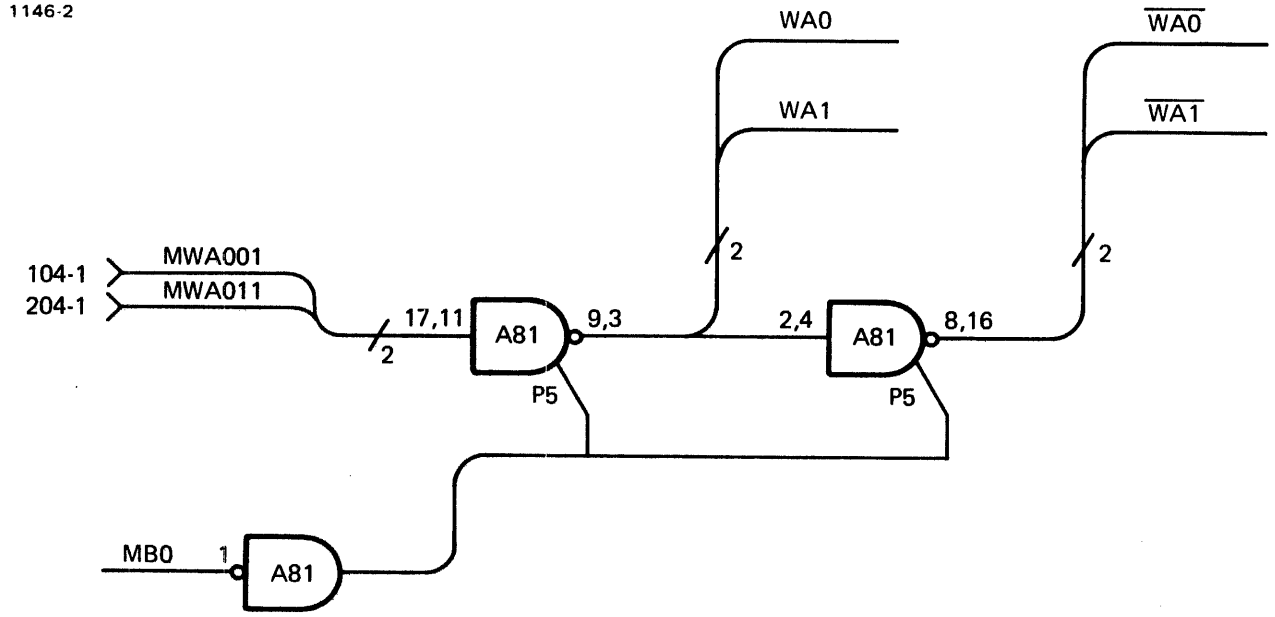


Figure 14-7 Word Access Decode

1880

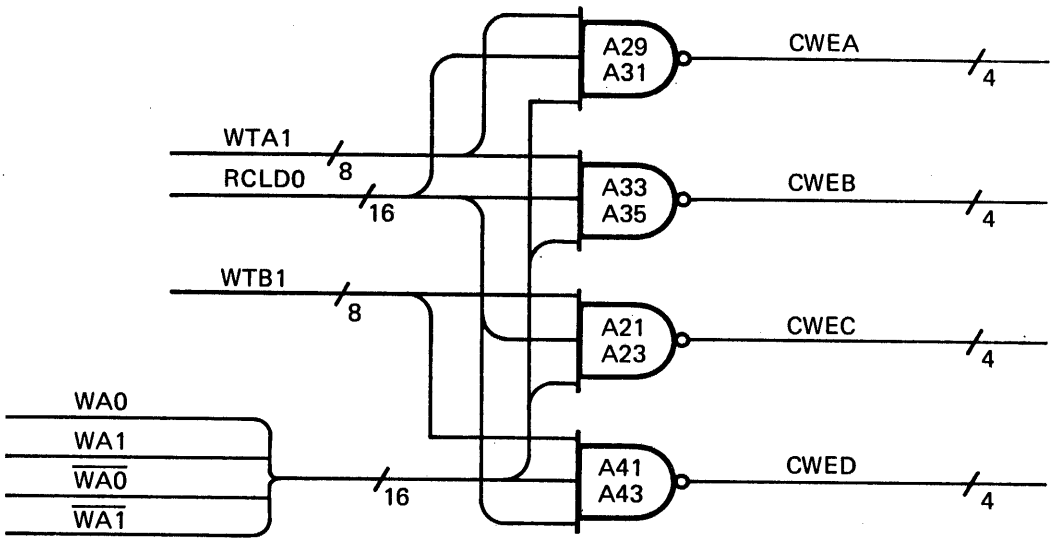


Figure 14-8 Write Clock Drivers

14.2.1.7 Write Mode

A write to memory occurs upon arrival of Memory Write Enable (MWE0) going low (active). The output generates a high (inactive) level on the output of A66, Pin 7 (RE0). This signal disables the 4:1 multiplexors and thus enables the write data to be placed onto the internal bidirectional data bus. The Data Input Enable (DIE0) going low (active) activates I/O receivers which place the write data into the RAM chip's D input, as shown in Figure 14-9. Simultaneously, the Write Timing flip-flop (A49) is clocked and, along with single-shot pulse generator (A47), produces Write Timing Pulse WTA1 or WTB1. (Refer to Figure 14-6.) The presence of Chip Write Enable (CWE) (4B1) at both A and B arrays stores the data into the RAM location determined by LMB lines 001:131 during the address time. Figure 14-10 shows the timing during a write operation.

14.2.1.8 Read Mode

A read from memory occurs when the selected STM receives Memory Read Enable (MRE0). This low-active signal generates the signal Data Out Enable (DOE0). Since MWE0 is high (inactive) during this time, as shown in Figure 14-11, RE0 is low (active). This enables the 4:1 multiplexors to receive data from the RAMs. In addition, DOE0 is propagated through a delay (typically 12 ns) to

an input of NAND gate A81 and is coupled with a delayed (typically 100 ns) CASET1 to generate a Memory Read Data Strobe (MRDS0) signal. (Refer to Figure 14-12.) The MWA lines then select one of four channels of the multiplexor which places the read data onto the internal bidirectional bus. The first MRDS0 (first word in the quadword mode) is delayed by CASET1 and delay line A77 (typically 100 ns), to insure proper setup and access time of the RAM data. The second, third, and fourth MRDS0s (in quadmode operation) are delayed by the RC circuit and propagation delay of the gates between A81, pin 8 (DOE0) and A81, pin 14 (MRDS0) (typically 20 ns).

1881

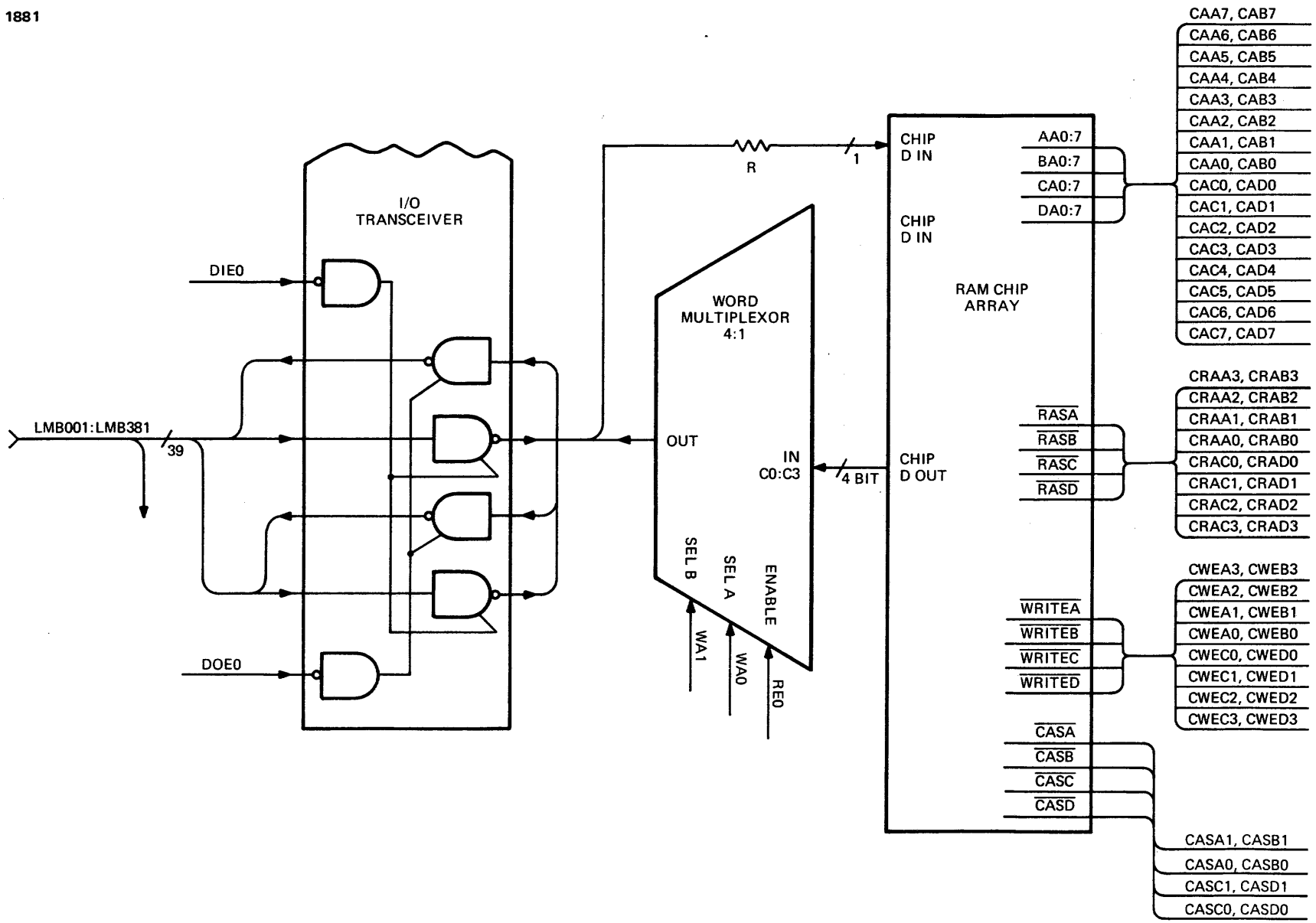


Figure 14-9 Data I/O

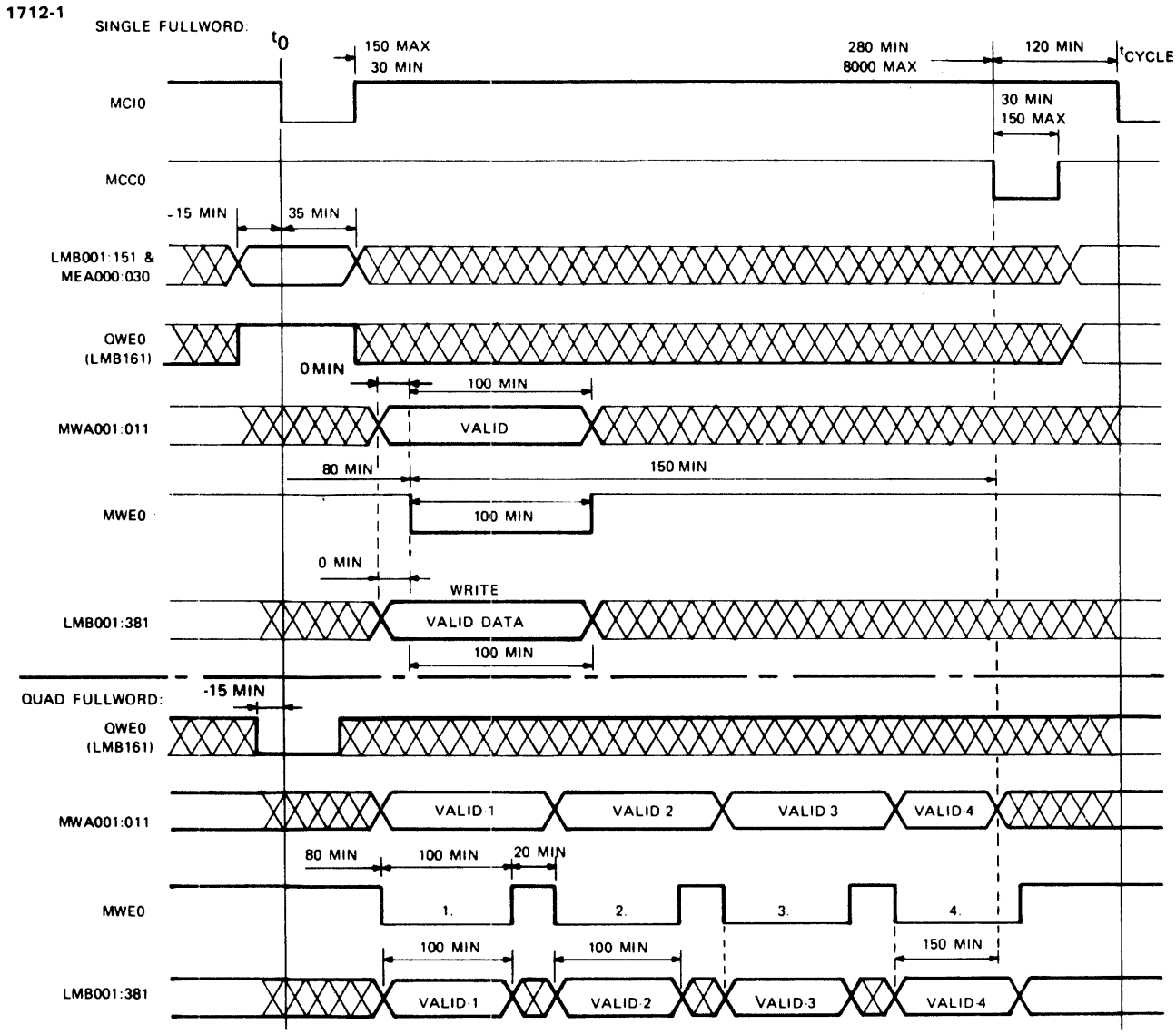


Figure 14-10 STM Write Mode Timing Diagram

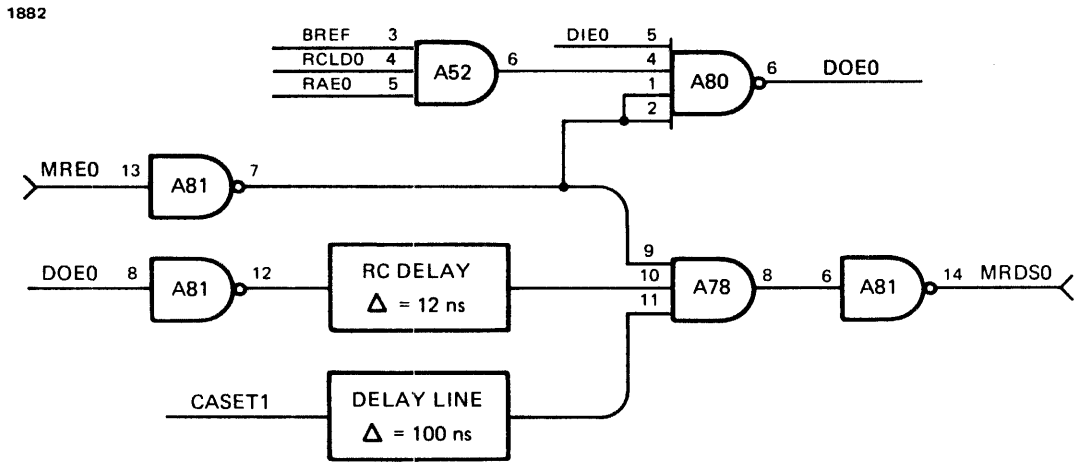


Figure 14-11 Read Control

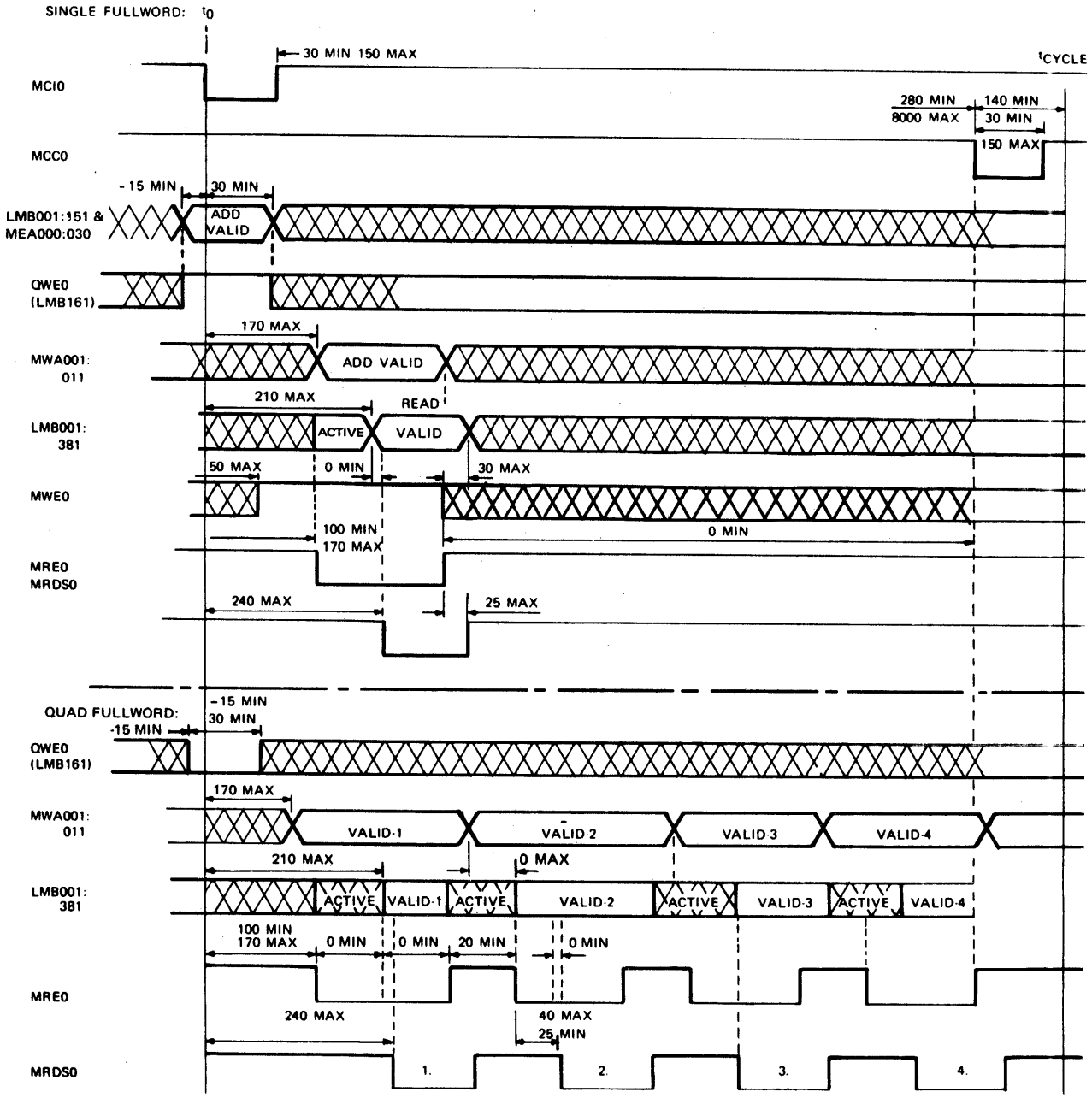


Figure 14-12 STM Read Mode Timing Diagram

14.2.1.9 Refresh

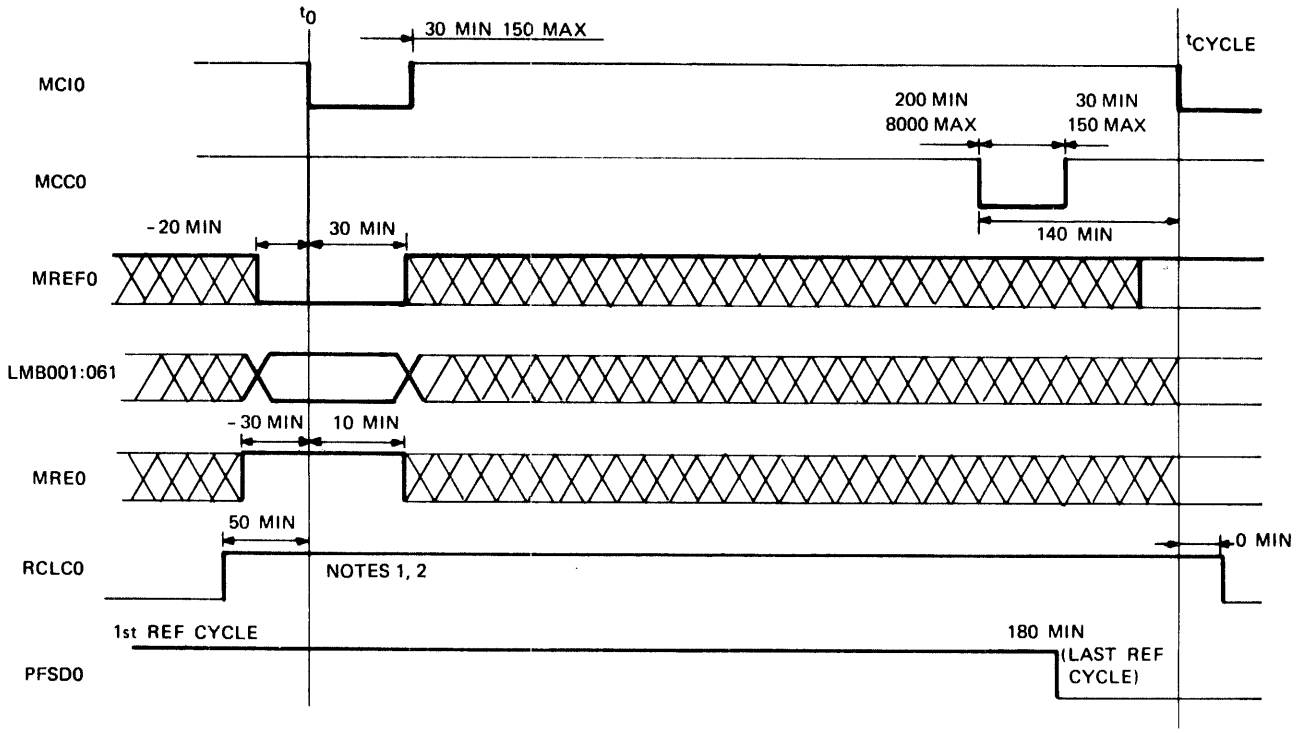
The dynamic nature of the RAM chips requires periodic refreshment of stored data every 2.0 ms. (Refer to Figure 14-13.) Refresh is accomplished when the STM receives the MREF0 signal. This signal sets the STM into the refresh mode, prevents write operations, and enables all RAS drivers to produce RAS clock to all RAMs.

Refresh (row) address lines are latched by arrival of MCI0 and clocked by RAS into the RAMs. The STM operates in two refresh modes: cycle steal mode, and burst (battery backup) mode.

Cycle steal - 128 refresh cycles are generated every 2 ms in between read or write operations.

Burst (battery backup) - 128 refresh cycles are generated in one burst every 2 ms. In between the bursts, the P5S is shut down, thus reducing the current drain on P5U which is battery backed up.

1715-1



NOTES

1. APPLICABLE IN THE BURST REFRESH MODE ONLY

2. THE RISE AND FALL TIME OF RCLC0 IS LESS THAN 100 ns (.8 V TO 2.4 V).

Figure 14-13 STM Refresh Mode Timing Diagram

14.2.2 Power Supply

14.2.2.1 Introduction

The STM uses two +5.0 V supplies: P5 and P5U. P5 powers the nonrefresh circuitry. P5U (which is a separate uninterrupted +5.0 V supply) is used to supply the RAM chips and refresh-related circuitry. P5U must be maintained to ensure valid memory. Another source derived from P5U is P5S (switched). The P5S is generated via an on-board PNP transistor switch controlled by PFSD0. P5S powers refresh control circuitry which is pulsed every 2 ms during battery backup operation.

14.2.2.2 P5S Power Down

A P5S power-down sequence starts upon arrival of PFSD0 going low (active). This sets comparator A61, pin 10 high, which is compared to pin 11 (which maintains a 2.4 V level during normal operation). Since A61, pin 10 is higher than pin 11, pin 13 of A61 goes low, turning off the PNP transistor switch and thereby causing P5S to discharge eventually to ground. As P5S discharges below 4.8 V, A61, pin 14 goes low activating MCLC0, CC0, and RCLD0 to prevent an accidental write operation into RAMs. Low RCLC0 indicates to the controller (LBC) that the STM is in the low-power mode.

14.2.2.3 P5S Power Up

P5S power-up is accomplished following the release of PFSD0=1 (inactive). PFSD0 going high turns on the PNP transistor switch which raises P5S to P5U level. Once P5S reaches approximately 4.8 V, A61, pin 14 goes high releasing RCLC0, CC0, and RCLD0. This signifies to the controller that the STM is ready to accept refresh cycles.

14.3 MNEMONICS

The following is a list of the mnemonics on the STM board. The meaning and the 35-764D08 schematic location of each signal are provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
BREF0	Buffered refresh	2E1
BSCLR0	Buffered systems clear	16B5
CA"A":CA"D"	Chip address lines (A-D)	3G1-9
CAE0	Column address enable	2M4
CAS"A":CAS"D"	Column address strobe	3M5-9
CASTA1:CASTB1	Column address strobe timing	2M4
CRAA0:CRAD0	Row address strobe	3K1-9

MNEMONIC	MEANING	SCHEMATIC LOCATION
CWEA:D	Chip write enable	4D1-9
DIE0	Data in enable	2M7
DOE0	Data out enable	2M8
LMB001:061	Local memory bus (row address and data lines)	3A2
LMB071:131	Local memory bus (column address and data lines)	3A5
LMB141:151	Local memory bus (word row selection and data lines)	3A7
LMB161	Local memory bus (single/quad select and data line)	3A7
LMB171:381	Local memory bus (data lines)	6E7
MB0	Memory busy	2D3
MCC0	Memory cycle complete	2A3
MCI0	Memory cycle initialize	2A3
MEA00:30	Memory expansion address	2B7
MRDS0	Memory read data strobe	2M8
MRE0	Memory read enable	2E7
MREF0	Memory refresh	3A7
MS1	Module select	2H5
MWA001:011	Memory word access	2B9
MWE0	Memory write enable	2E7
MX031:011	Memory super expansion address	2A5
P5	+5 V supply	16A8
P5S	+5 V switched supply (internal)	16M7
P5U	+5 V uninterruptible supply	16L6
PFSD0	P5S shutdown	16B6
RAE0	Row address enable	2F4
RAST1	Row address strobe timing	2M2
RCLC0:D0	Refresh clear	16J5
RE0	Read enable	2J6
REF0	Refresh	3C7
WA0, WA1	Word access select lines	2C9
WT1	Write timing	2N3

CHAPTER 15
ADJUSTMENTS

15.1 INTRODUCTION

This section provides the adjustments for the EDMA Protocol Logic, EDMA control oscillator, and the High Performance Floating-Point Processor (HPFPP). The CPU clocks are derived from a crystal oscillator and require no adjustments.

15.2 EDMA PROTOCOL LOGIC OSCILLATOR ADJUSTMENT

These oscillators are set at the factory and usually do not require further adjustments. If adjustments are necessary, however, the following procedure should be followed (refer to Sheet 6 of Functional Schematic 35-770D08):

1. Turn processor power off.
2. Connect 04H09 to ground.
3. Connect 04B11 to ground.
4. Connect 04B04 to ground.
5. Turn processor power on.
6. With scope probe on QUE0 (04R08), adjust capacitor 02A (80-02) for a 60 to 65 nanoseconds pulse width of QUE0.
7. Attach another scope probe on SOT0 (04R11). Adjust capacitor 04A (02-80) for 270 to 280 nanoseconds from falling edge of QUE0 to falling edge of SOT0.

15.3 LOCAL MEMORY TO EDMA CONTROL OSCILLATOR ADJUSTMENT

Perform the following five steps (refer to Sheet 5 of Functional Schematic 35-770D08):

1. Turn power off.
2. Connect 01A01 to ground.
3. Connect 01A04 to ground.

4. Turn power on.

5. Adjust capacitor 00A (80-02) for FDA1 to be a square wave period of 480 nanoseconds.

NOTE

If the waveform appears unstable, readjust the capacitor to a different position.

15.4 CLOCK ADJUSTMENTS FOR THE HPFPP

Refer to the Perkin-Elmer 3220 High Performance Floating-Point Processor Installation and Maintenance Manual, Publication Number 29-705, while performing the following steps:

1. Turn CPU power off and remove the HPFPP.

2. Install an M80 Extender Board (28-015) in slot 8 of the processor chassis.

3. Install the HPFPP in the M80 Extender Board with the HPFPP-A Board on top.

4. Connect a scope probe to TP1 (100-2 on HPFPP-A) ACLK1A and adjust the scope time base for 20 nanoseconds/division. (Refer to Functional Schematic 35-715D08, Sheet 4, Location M7.)

5. Select nominal clocks by setting the dip switches in location 16A on the HPFPP-A to the following positions:

SWITCH #	POSITION	SWITCH #	POSITION
1	OFF	5	OFF
2	ON	6	OFF
3	OFF	7	ON
4	OFF	8	OFF

6. Turn CPU power on and momentarily ground pin 5 of the IC at 16B (HPFPP-A).

NOTE

Grounding 16B05 forces the HPFPP oscillator into a free-running condition which can be halted only by an initialize or power down.

7. Set the HPFPP clocks to nominal by adjusting the trimmer capacitor at location 14B on the HPFPP-A Board. Nominal clocks are:

   ACLK1A (TP-1) = 100 nanoseconds (rise edge to rise edge at 1.5 V levels)

8. Turn CPU power off and remove HPFPP from the extender board.

9. Remove extender board from the processor chassis.

10. Install the HPFPP-B Board in slot 8 and the HPFPP-A board in slot 7 of the processor chassis. Install the two 50-conductor cables between connectors 3 and 4 of the HPFPP-A and -B Boards.

CHAPTER 16
02-663 TEST AID

16.1 INTRODUCTION

The 02-663 Test Aid is a compact, durable, and simple-to-use test fixture. It provides the necessary control to display the B, S, and ROM DATA (RD) buses of the processor, as well as the Control Store Address (CSA), four processor flags, Instruction Register (IR), and I/O attention lines (INT).

This chapter covers the operation, installation, and maintenance of the Test Display.

16.2 GENERAL DESCRIPTION

The 02-663 Test Aid consists of two printed circuit board assemblies, one of which is attached to the processor boards by two front cables. The other board is connected to the backpanel on one of the processor board positions and cabled to the first board by a single flat ribbon cable. Figure 16-1 shows the connections to the processor.

Figures 16-2 and 16-3 show the switch, displays, and cable connections of the test display.

The numbered parts illustrated in Figures 16-2 and 16-3 have the following functions:

1. Cable to CPU-B board connector 4, slot 10
2. Cable to CPU-A board connector 3, slot 09
3. Cable to Test Aid multiplexor
4. Control store address display
5. Display for selected bus
6. Bus selection switch
7. Flag register display
8. Cable from Test Aid multiplexor to display box
9. Connector to mate at location 0, slot 09
10. Connector to mate at location 1, slot 09

1883-1

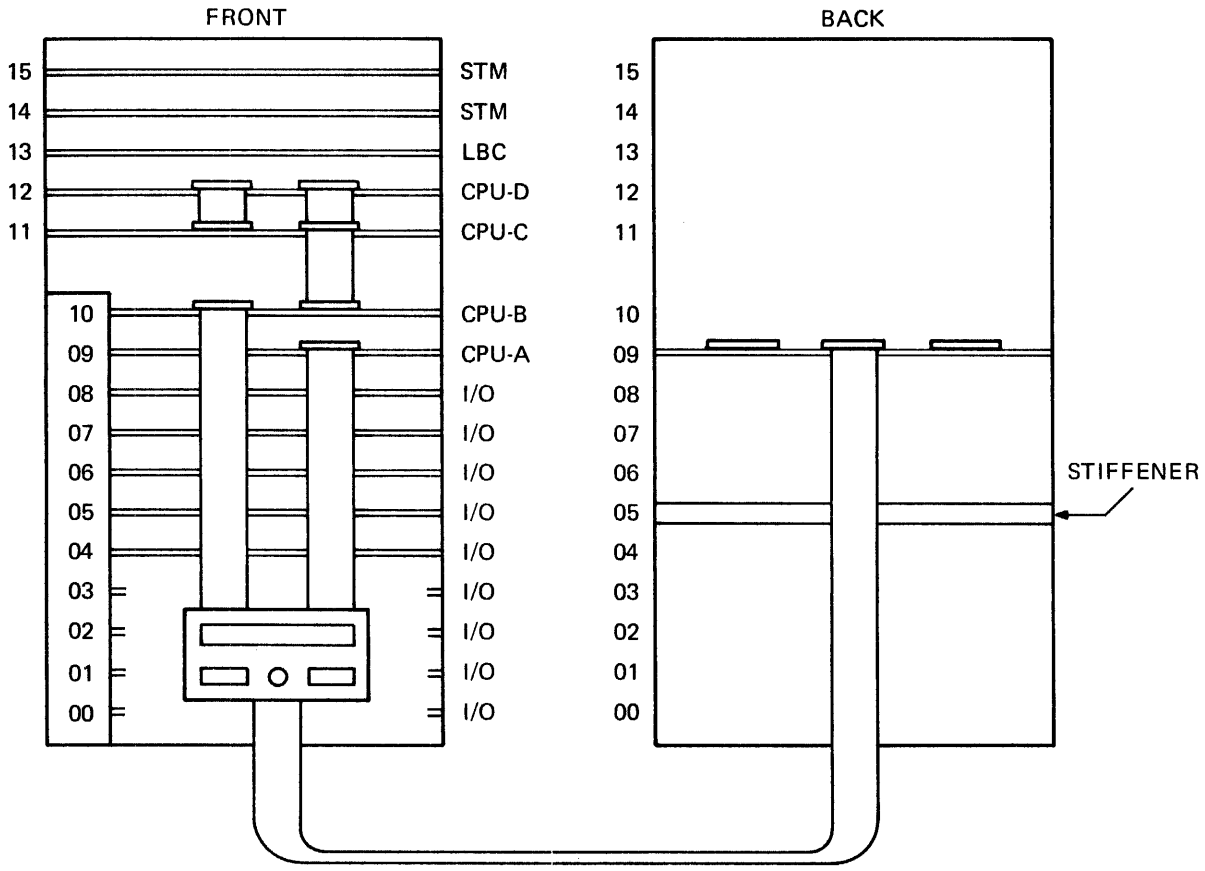


Figure 16-1 Test Aid Connections to Processor

0906

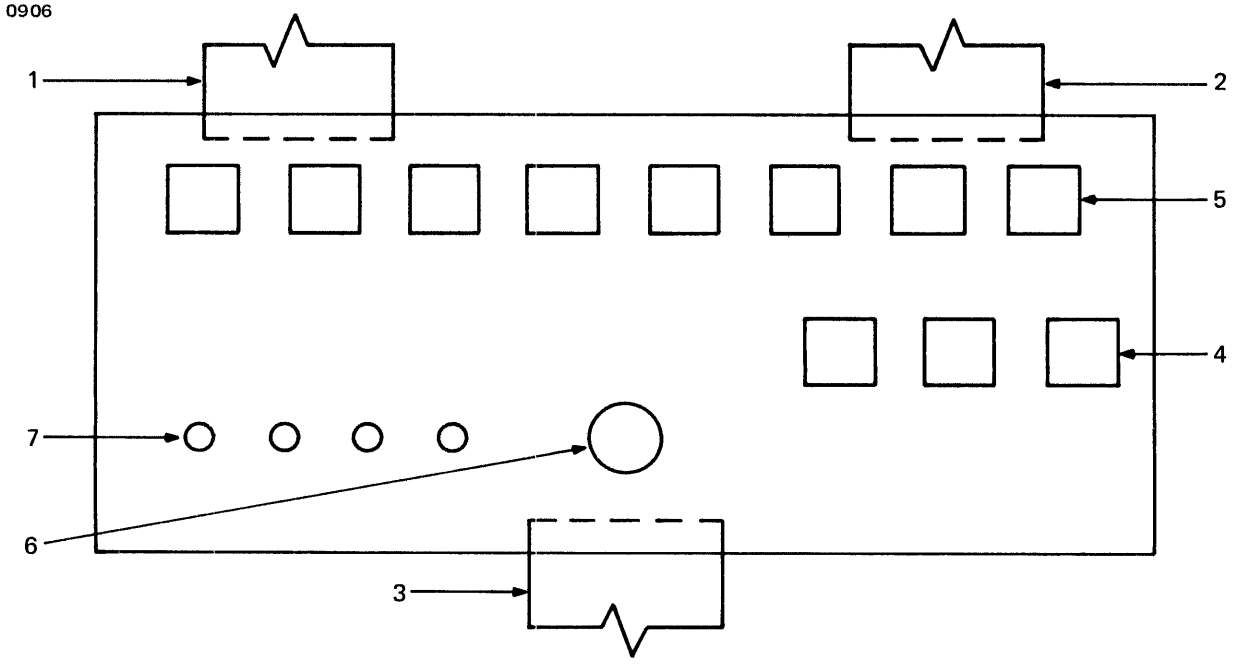


Figure 16-2 Display Box

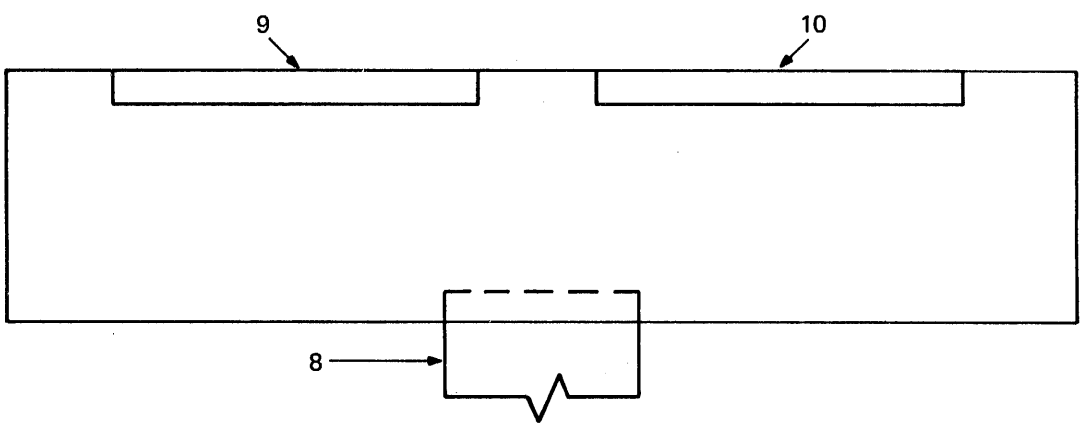


Figure 16-3 Test Aid Multiplexor Board

16.3 INSTALLATION AND OPERATION PROCEDURE

Install and operate the 02-663 Test Aid as follows:

1. Place the console power switch in the STANDBY position.
2. Install cable 1 (refer to Figure 16-2) on connector 4 of the CPU-B board, slot 10. (Refer to Figure 16-1.)
3. Install cable 2 (refer to Figure 16-2) on connector 3 of the CPU-A board, slot 09. (Refer to Figure 16-1.)
4. Put the Test Aid multiplexor on the backpanel CPU-A position, slot 09.
5. Connect the cable from the display box to the Test Aid multiplexor. The cable should lie flat with no twists.
6. Select the bus to be displayed, IR, B, S, or RD by switch 6 (refer to Figure 16-2).
7. Operate the system in the usual manner. The displays track the state of the buses.

16.4 POWER SUPPLY

Power is supplied to the Test Aid multiplexor directly from the backpanel. Power is supplied to the display board from the Test Aid multiplexor through the cable.

16.5 EXTENDER BOARD OPERATION

Cable 2 (refer to Figure 16-2) is provided with enough length for extender board operation.

16.6 TEST AID OPERATION

16.6.1 Test Aid Multiplexor

The Test Aid multiplexor buffers the flag register bits and sends them to the display board; it also corrects the logic levels of some signals and multiplexes the instruction register with I/O attention lines, B bus, and ROM Data Bus (RD Bus) data to the display board. The bus selection switch on the display board generates the two multiplexor control lines, IR0 and RD0, which steer the multiplexors as follows:

IR0	RD0	FUNCTION TO DISPLAY
Low	Low	Not used
Low	High	IR bus with attention lines
High	Low	RD bus
High	High	B bus

NOTE

The RD bus does not display RD bits 6, 7, or 8. Bit 7 is SFTEN1 (Single-Precision Floating-Point Enable); bit 6 is DFTEN1 (Double Precision Floating-Point Enable); and bit 8 is tied to ground.

16.6.2 Display Board

The display board selects either the input from the backpanel board or the S bus data by a signal from the selector switch. It then displays the selected bus on the hexadecimal display. The control store address is also inverted and displayed on hexadecimal displays. The flag register bits are displayed on individual LEDs.

16.7 TEST AID DISPLAY

The 02-663 Test Aid uses the Model 8/32 test display printed circuit assembly. The following is a mnemonic cross reference between the 8/32 test display schematics provided (35-612D08) and the Test Aid multiplexor board.

203-5	SAB1EN0	IR0
103-5	SAB2EN0	RD0
121-5	CC0	FLR280
221-5	VCC0	FLR290
120-5	GCC0	FLR200
220-5	LCC0	FLR310
216-3	CSAD040	CSAR200
116-3	CSAD050	CSAR210
218-3	CSAD060	CSAR220
117-3	CSAD070	CSAR230
219-3	CSAD080	CSAR240
118-3	CSAD090	CSAR250
220-3	CSAD100	CSAR260
120-3	CSAD110	CSAR270
222-3	CSAD120	CSAR280
121-3	CSAD130	CSAR290
223-3	CSAD140	CSAR300
122-3	CSAD150	CSAR310
119-5	SAB0	MXD001
219-5	SAB1	MXD011
118-5	SAB2	MXD021
218-5	SAB3	MXD031
117-5	SAB4	MXD041
217-5	SAB5	MXD051
116-5	SAB6	MXD061
216-5	SAB7	MXD071
115-5	SAB8	MXD081
215-5	SAB9	MXD091
114-5	SAB10	MXD101
214-5	SAB11	MXD111
113-5	SAB12	MXD121
213-5	SAB13	MXD131
112-5	SAB14	MXD141
212-5	SAB15	MXD151
111-5	SAB16	MXD161
211-5	SAB17	MXD171
110-5	SAB18	MXD181
210-5	SAB19	MXD191
109-5	SAB20	MXD201
209-5	SAB21	MXD211
108-5	SAB22	MXD221
208-5	SAB23	MXD231
107-5	SAB24	MXD241
207-5	SAB25	MXD251
106-5	SAB26	MXD261
206-5	SAB27	MXD271
105-5	SAB28	MXD281
205-5	SAB29	MXD291
104-5	SAB30	MXD301
204-5	SAB31	MXD311
204-4	CSD001	S001
105-4	CSD011	S011

TEST AID CONN PIN NO.	8/32	02-563
205-4	CSD021	S021
106-4	CSD031	S031
207-4	CSD041	S041
107-4	CSD051	S051
208-4	CSD061	S061
109-4	CSD071	S071
209-4	CSD081	S081
110-4	CSD091	S091
211-4	CSD101	S101
111-4	CSD111	S111
212-4	CSD121	S121
113-4	CSD131	S131
213-4	CSD141	S141
114-4	CSD151	S151
215-4	CSD161	S161
115-4	CSD171	S171
216-4	CSD181	S181
117-4	CSD191	S191
217-4	CSD201	S201
118-4	CSD211	S211
219-4	CSD221	S221
119-4	CSD231	S231
220-4	CSD241	S241
121-4	CSD251	S251
221-4	CSD261	S261
122-4	CSD271	S271
223-4	CSD281	S281
123-4	CSD291	S291
224-4	CSD301	S301
124-4	CSD311	S311

CHAPTER 17
HIGH SPEED DATA HANDLING OPTION

17.1 INTRODUCTION

The High Speed Data Handling Option upgrades the autodriver channel of the processor and adds two instructions to the user instruction repertoire. The autodriver channel calculation time for CRC-BISYNC is greatly reduced and error checking capability is increased to include the CRC-SDLC format. The two added instructions are: Process Byte (PB) and Process Byte Register (PBR). These provide the capability to perform error checking of characters or generation of check characters one data byte at a time. An error check can be calculated in any one of the three formats: LRC, CRC-BISYNC (also called CRC-16), or CRC-SDLC.

17.2 BLOCK DIAGRAM ANALYSIS

The D bus receivers shown in Figure 17-1 buffer direct the I/O bus data to the appropriate logic. The address logic determines if the High Speed Data Handling Option has been selected by the processor. The steering counter logic determines what type of data is being sent to the board and enables the appropriate register for loading. Three types of data can be sent to the board: format data, residual check character data, or the current data character tc be included in the residual check character. The format select register is set up by the format data from the processor. One of three formats can be selected: LRC, CRC-BISYNC, or CRC-SDLC. The current data character register contains the current data character for inclusion into the residual character. Table 17-1 contains the base numbers used to calculate the residual check character and is used to calculate CRC-BISYNC and CRC-SDLC. The table in use is selected by the format select logic. The check character buffer contains the residual check character and is updated with a new residual check character each time the current data character register is loaded. The D bus drivers gate data to the D bus when the processor attempts to read the check character buffer. The box active logic is part of the control logic that allows the board to accumulate an error check character.

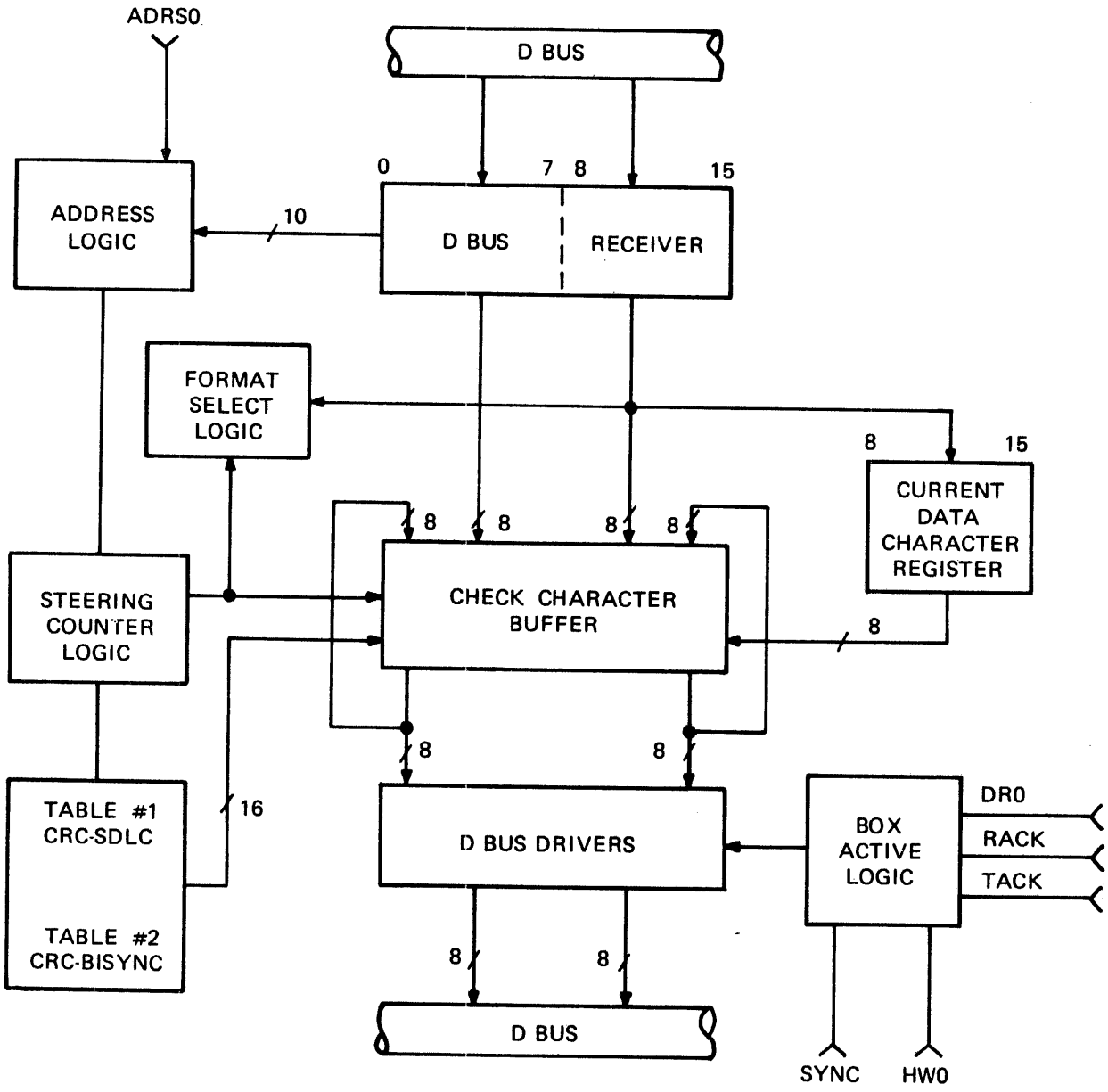


Figure 17-1 High Speed Data Handling Option Block Diagram

TABLE 17-1 DATA BASE TABLES

(a) Data for the CRC-BISYNC

00	0000	C0C1	C181	0140	C301	03C0	0280	C241
08	C601	06C0	0780	C741	0500	C5C1	C481	0440
10	CC01	0CC0	0D80	CD41	0F00	CFC1	CE81	0E40
18	0A00	CAC1	CB81	0B40	C901	09C0	0880	C841
20	D801	18C0	1980	D941	1B00	DBC1	DA81	1A40
28	1E00	DEC1	DF81	1F40	DD01	1DC0	1C80	DC41
30	1400	D4C1	D581	1540	D701	17C0	1680	D641
38	D201	12C0	1380	D341	1100	D1C1	D081	1040
40	F001	30C0	3180	F141	3300	F3C1	F281	3240
48	3600	F6C1	F781	3740	F501	35C0	3480	F441
50	3C00	FCC1	FD81	3D40	FF01	3FC0	3E80	FE41
58	FA01	3AC0	3B80	FB41	3900	F9C1	F881	3840
60	2800	E8C1	E981	2940	EB01	2BC0	2A80	EA41
68	EE01	2EC0	2F80	EF41	2D00	EDC1	EC81	2C40
70	E401	24C0	2580	E541	2700	E7C1	E681	2640
78	2200	E2C1	E381	2340	E101	21C0	2080	E041
80	A001	60C0	6180	A141	6300	A3C1	A281	6240
88	6600	A6C1	A781	6740	A501	65C0	6480	A441
90	6C00	ACC1	AD81	6D40	AF01	6FC0	6E80	AE41
98	AA01	6AC0	6B80	AB41	6900	A9C1	A881	6840
A0	7800	B8C1	B981	7940	BB01	7BC0	7A80	BA41
A8	BE01	7EC0	7F80	BF41	7D00	BDC1	BC81	7C40
B0	B401	74C0	7580	B541	7700	B7C1	B681	7640
B8	7200	B2C1	B381	7340	B101	71C0	7080	B041
C0	5000	90C1	9181	5140	9301	53C0	5280	9241
C8	9601	56C0	5780	9741	5500	95C1	9481	5440
D0	9C01	5CC0	5D80	9D41	5F00	9FC1	9E81	5E40
D8	5A00	9AC1	9B81	5B40	9901	59C0	5880	9841
E0	8801	48C0	4980	8941	4B00	8BC1	8A81	4A40
E8	4E00	8EC1	8F81	4F40	8D01	4DC0	4C80	8C41
F0	4400	84C1	8581	4540	8701	47C0	4680	8641
F8	8201	42C0	4380	8341	4100	81C1	8081	4040

TABLE 17-1 DATA BASE TABLES (Continued)

(b) Data for the CRC-SDLC

00	0000	1189	2312	329B	4624	57AD	6536	74BF
08	8C48	9DC1	AF5A	BED3	CA6C	DBE5	E97E	F8F7
10	1081	0108	3393	221A	56A5	472C	75B7	643E
18	9CC9	8D40	BFDB	AE52	DAED	CB64	F9FF	E876
20	2102	308B	0210	1399	6726	76AF	4434	55BD
28	AD4A	BCC3	8E58	9FD1	EB6E	FAE7	C87C	D9F5
30	3183	200A	1291	0318	77A7	662E	54B5	453C
38	BDCB	AC42	9ED9	8F50	FBEF	EA66	D8FD	C974
40	4204	538D	6116	709F	0420	15A9	2732	36BB
48	CE4C	DFC5	ED5E	FCD7	8868	99E1	AB7A	BAF3
50	5285	430C	7197	601E	14A1	0528	37B3	263A
58	DECD	CF44	FDDF	EC56	98E9	8960	BBFB	AA72
60	6306	728F	4014	519D	2522	34AB	0630	17B9
68	EF4E	FEC7	CC5C	DDD5	A96A	B8E3	8A78	9BF1
70	7387	620E	5095	411C	35A3	242A	16B1	0738
78	FFCF	EE46	DCDD	CD54	B9EB	A862	9AF9	8B70
80	8408	9581	A71A	B693	C22C	D3A5	E13E	F0B7
88	0840	19C9	2B52	3ADB	4E64	5FED	6D76	7CFF
90	9489	8500	B79B	A612	D2AD	C324	F1BF	E036
98	18C1	0948	3BD3	2A5A	5EE5	4F6C	7DF7	6C7E
A0	A50A	B483	8618	9791	E32E	F2A7	C03C	D1B5
A8	2942	38CB	0A50	1BD9	6F66	7EEF	4C74	5DFD
B0	B58B	A402	9699	8710	F3AF	E226	D0BD	C134
B8	39C3	284A	1AD1	0B58	7FE7	6E6E	5CF5	4D7C
C0	C60C	D785	E51E	F497	8028	91A1	A33A	B2B3
C8	4A44	5BCD	6956	78DF	0C60	1DE9	2F72	3EFB
D0	D68D	C704	F59F	E416	90A9	8120	B3BB	A232
D8	5AC5	4B4C	79D7	685E	1CE1	0D68	3FF3	2E7A
E0	E70E	F687	C41C	D595	A12A	B0A3	8238	93B1
E8	6B46	7ACF	4854	59DD	2D62	3CEB	0E70	1FF9
F0	F78F	E606	D49D	C514	B1AB	A022	92B9	8330
F8	7BC7	6A4E	58D5	495C	3DE3	2C6A	1EF1	0F78

17.3 FUNCTIONAL DESCRIPTION

Sheet 2 of the High Speed Data Handling Schematic (02-428D08) contains the logic comprising the most significant portion (bits 0:7) of the Residual Check Character Register (RCCR). Sheet 3 of the schematic contains the least significant portion (bits 8:15) of the RCCR. The most significant bits can be loaded with three different data forms: data from the D bus, data from Table 17-1, or data from the RCCR itself. The least significant bits can also be loaded with three data formats. The major difference is that the former is loaded with its own contents, while the latter is loaded with the Exclusive-ORed data of the RCCR's most significant 8 bits and the least significant 8 bits of the Table Data (TDAT 8:15). The steering counter shown on Sheet 5 determines the format of data loaded into the RCCR.

Sheet 4 of the schematics contains the format register, Current Character Register (CCR), and the CRC tables. The CCR is an 8-bit register containing the data character currently being calculated into the RCCR. The CCR is loaded from the D bus if the steering counter (Sheet 5) causes it to be a destination. The output of the CCR is Exclusive-ORed with the least significant bits of the RCCR. The resultant data is used as the new residual check character in the LRC mode of error check or the resultant data is applied as an address on CRC tables. There are two distinct data groups that provide data base information for the calculation of character error checks in either a CRC-SDLC or CRC-BISYNC format. Selection of a specific character within the tables is accomplished by the address data from the Exclusive-ORed gates. This address information selects one 16-bit character out of a possible 256 in a given table. Table selection is accomplished by the Format Register (FMTR) which is loaded from the D bus if the steering counter (Sheet 5) selects the FMTR to be a destination. Data loaded into the FMTR specifies one of three types of error checking: LRC, CRC-BISYNC, or CRC-SDLC.

Sheet 5 of the schematics contains both timing and control logic for the High Speed Data Handling Board. This logic may be divided into three categories:

- addressing logic
- acknowledge logic
- clock steering logic

Depending upon strap options, the addressing logic determines if the board is selected by the processor. If TP6 is high, the processor has selected the board and an operation is in progress.

The High Speed Data Handling Option Board has a preferred device address of X'006' when strapped for operation on the processor. The acknowledge logic captures the RACK0 signal once the board is selected by the XXXX processor. The RACK0 signal, when captured, results in gating the contents of the RCCR to the D bus. The acknowledge logic is disabled when the board is set up for a 3240 processor and all RACK0s are propagated as TACK0s. Assuming the board is selected, every transition of CMD0 and DA0 (3240 processor only) or BCNT0 (XXXX processor only) causes an internal clock to be generated in the clock steering logic. This clock toggles a 2-bit counter that steers a delayed clock to the appropriate destination register. There are three valid states:

- 01 causes the FMTR to be loaded.
- 10 causes the RCCR to be loaded from the D bus.
- 11 causes the CCR to be loaded and the RCCR to be updated.

The counter remains in state 11 until either an ADRS1 (3240 processor) or an ACK0 (3215 processor) is received. At this time the counter is cleared and the board returned to the initialized state until it is again accessed by the processor.

17.4 CHARACTER ERROR CHECKING CALCULATIONS

The following examples describe the interaction between the processor and the High Speed Data Handling Option Board.

LRC Example:

1. The FMTR is loaded with X'02', placing the High Speed Data Handling Option Board in the LRC mode of error checking.

2. The RCCR is loaded with an initial residual of X'0000'. The initial residual can be any number.

3. The CCR is loaded with X'01' and is Exclusive-ORed with the least significant 8 bits of the RCCR.

4. The resultant data (step 3) is loaded into the least significant 8 bits of the RCCR leaving the most significant bits unchanged. The RCCR contains the value of X'001'.

5. The CCR is loaded next with an X'03' and Exclusive-ORed with the current contents of the RCCR. The resultant data is loaded into the RCCR. The content of the RCCR is X'002'.

CRC-BISYNC Example:

1. The FMTR is loaded with X'00', placing the High Speed Data Handling Option Board in the CRC-BISYNC mode of error checking.

2. The RCCR is loaded with an initial residual value of X'0000', but can be any number.

3. The CCR is loaded with X'01' and Exclusive-ORed with the least significant 8 bits of the RCCR.

4. The resulting data (step 3) is applied to the address inputs of the CRC-BISYNC portion of the ROM table. The CRC-BISYNC table output is X'C0C1'.

5. The most significant 8 bits of the ROM table output are loaded into the most significant 8 bits of the RCCR, and the least significant 8 bits of the ROM table output is Exclusive-ORed with the initial most significant 8 bits of the RCCR.

6. The resulting data (step 5) is loaded into the least significant 8 bits of the RCCR. The RCCR contains the value X'C0C1'.

7. The CCR is next loaded with an X'02' and is Exclusive-ORed with the least significant 8 bits of the RCCR. The output of the CRC-BISYNC table is X'5140'.

8. The least significant 8 bits of the CRC-BISYNC table are Exclusive-ORed with the most significant 8 bits of the RCCR. The RCCR still contains the X'C0C1' residual. The most significant 8 bits of the CRC-BISYNC table are loaded into the most significant 8 bits of the RCCR, and the least significant 8 bits of the RCCR are loaded with the Exclusive-ORed result.

CRC-SDLC Example:

Calculations for the CRC-SDLC are identical to the CRC-BISYNC with the exception that the data base table used is for CRC-SDLC.

Table 17-1 is a listing of the data base tables used to calculate CRC-BISYNC and CRC-SDLC. The Exclusive-ORed result of the contents of the CCR and the least significant 8 bits of the RCCR become the 8-bit address of a word in the appropriate table. The words contained in the table are partial results.

17.5 MNEMONICS LIST

The following is a list of the mnemonics within the High Speed Data Handling Option Board. These mnemonics represent the function of a given signal in an abbreviated form, and are taken from the 02-428D08 schematics.

MNEMONIC	MEANING	SCHEMATIC LOCATION
ACCM0	Accumulates a check character; indicates that the steering counter is in the 11 state	Sheets 2, 3, and 5
ADRS0	Used by the processor I/O system when selecting a device on the bus (3240 processor only)	Sheet 5

MNEMONIC	MEANING	SCHEMATIC LOCATION
BADRC	High speed data handling address line (XXXX processor only); must be grounded at backpanel	Sheet 5
BCNTO	High speed data handling control line (XXXX processor only)	Sheet 5
C001:150	Newly calculated residual character input data	Sheets 2 and 3
CCRNTO	Clears the steering counter and initializes the board	Sheets 4 and 5
D000:150	D bus data sent and received by the processor	Sheets 2, 3, and 4
DCRO	Unused processors	Sheet 5
ELRES1	Early load residual character - used when loading the RCCR from the D bus	Sheets 2 and 5
LDATA1	Loads data character from the D bus into the Current Character Register (CCR)	Sheets 4 and 5
LFMT1	Loads Format Register (FMTR) from the D bus	Sheets 4 and 5
LLRES1	Late load residual character - used when updating the RCCR from the internal calculations (C001:151)	Sheets 2 and 5
LRCD081:151	LRC data - this is the Exclusive-ORed contents of the CCR and the least significant 8 bits of the RCCR.	Sheets 3 and 4
LRCEN1	LRC enable - decoded state of the FMTR indicating the selected LRC format of error check	Sheets 3 and 4
RACKO	Received acknowledge - when operation is in progress, indicates processor is unloading RCCR	Sheet 5

MNEMONIC	MEANING	SCHEMATIC LOCATION
RCD001:151	Residual character data - contents of the Residual Check Character Register	Sheets 2, 3, and 4
TDAT001:151	Table data output - may be from either the CRC-BISYNC or CRC-SDCC portion of the table	Sheets 2, 3, and 4
ULCRC1	Unloads the Residual Check Character Register into the D bus	Sheets 3 and 5

CHAPTER 18
8 MEGABYTE (8 MB) LOCAL BANK CONTROLLER (LBC)

18.1 INTRODUCTION

18.1.1 General

Although the 3210 memory system can contain a maximum of only 4 Mb of main memory, the 35-806F02 8 Mb LBC may alternately be installed in place of the 35-771F04 4 Mb LBC described in Chapter 13. Even though the 35-806F02 LBC has 8 Mb addressing capability, the 3210 is restricted to 4 Mb of main memory due to spare slot availability and STM power requirements.

18.1.2 Power Requirements

Table 18-1 provides the power requirements for the LBC board.

TABLE 18-1 POWER REQUIREMENTS

VOLTAGE SYMBOL	NOMINAL VOLTAGE	MAXIMUM CURRENT DRAIN (AMPS)		
		OPERATING (SELECTED)	OPERATING (UNSELECTED)	BATTERY MODE
P5	+5.0 V	13.7A	13.7A	13.7A*
P5U	+5.0 V	1.8A	1.8A	1.8A

*P5 supply may be depowered in the battery mode.

18.1.3 Strapping and Test Point Information

The following test points are located on the front edge of the 35-806F02 LBC Board:

1. ECC Disable (TP1 and TP2, Sheet 5)

   Strapping TP1 to TP2 disables the Error Check and Correction (ECC) circuit, thereby preventing correction or detection of data errors. The error logger cannot be updated with the ECC disabled.

   For normal ECC and error logger operation, TP1 and TP2 should be left unstrapped.

2. TP3-TP4 Strap

   TP3-TP4 must always be strapped for this system.

3. P5U Monitor (TP6, Sheet 13)

   The P5U supply voltage (+5.0 V + 1%) may be monitored at TP6 using TP1, TP3, or TP7 for the ground reference.

4. MB1 Monitor (TP5, Sheet 13)

   The MB1 flip-flop may be monitored at this point using TP1, TP3, TP7, TP10, or TP12 for the ground reference.

5. TP7-TP8 Strap

   TP7-TP8 must always be left unstrapped for this system.

6. TP9-TP10 Strap

   TP9 and TP10 must always be strapped for this system.

7. UCE Lamp Reset (TP11 and TP12, Sheet 7)

   The UCE lamp may be reset by momentarily shorting TP11 and TP12. This feature must be used only by trained personnel.

8. Cycle Steal Refresh Inhibit 0/1 (TP13 and TP14, Sheet 13)

   Cycle steal refresh may be inhibited by connecting either TP13 or TP14 to TP12 (GND). This feature must be used only by trained personnel.

9. Refresh Counter Load (TP15, Sheet 13)

   The refresh counter may be preset to all 1s by connecting TP15 to TP12 (GND). This feature must be used only by trained personnel.

10. Timer A Set (TP16, Sheet 16)

    The A Timer may be forced ON by connecting TP16 to TP12 (GND). The timer will remain in the active high state as long as TP16 is grounded. This feature must be used only by trained personnel.

11. P5 Shutdown and P5 Shutdown A (TPA and TPB, Sheet 13)

    TPA and TPB must remain strapped. Only trained personnel should remove this strap.

12. TPP, TPO, TPN, TPM, TPL, TPK, TPJ, TPI, TPH, TPG, TPF, TPE, TPD, and TPC. These test points are not used on the 35-806F02 LBC.

18.1.4 LBC LED Indicator Information

The following LED indicators are located on the front edge of the 35-806F02 LBC board:

1. P5U Indicator

   The P5U indicator lights whenever the P5U supply is active. The P5U supply remains active at all times unless the REMOTE POWER switch (X5) or the MAINTENANCE RESET switch is placed to the OFF position. Before removing the LBC board or STMs, verify that the P5U LED is extinguished and that the KEY switch on the System Control Panel (SCP) is in the OFF position.

2. Uncorrectable Error (UCE) and Module Identification Indicators

   The Uncorrectable Error (UCE) indicator lights whenever a Storage Module (STM) outputs a data word containing a detectable multiple bit error. When the UCE indicator is lit, the module ID indicators contain the 512 kb module address where the last Read error occurred.

   The UCE indicator remains lit until the SCP INITIALIZE switch is depressed, until the KEY switch is placed in the OFF position, until an REL instruction is executed, until a Read is executed to nonpresent memory, or until TP11 and TP12 are shorted. When the UCE indicator is off and the module ID indicators are on, they indicate that a memory access was made to the module specified by the lamps, but that the system is not equipped with that module.

18.2 FUNCTIONAL ANALYSIS

18.2.1 Refresh

Refer to Figures 18-1 and 18-2 for refresh timing information. The Storage Modules (STMs) utilize MOS dynamic Random Access Memories (RAMs) which require periodic refresh cycles at each of the 128 row address locations every two milliseconds. This is accomplished by executing a single refresh cycle every 16 microseconds (cycle steal mode) or a 128 refresh cycle burst every two milliseconds (burst mode). During any refresh cycle, every memory chip within the system is selected and refreshed at the same row location.

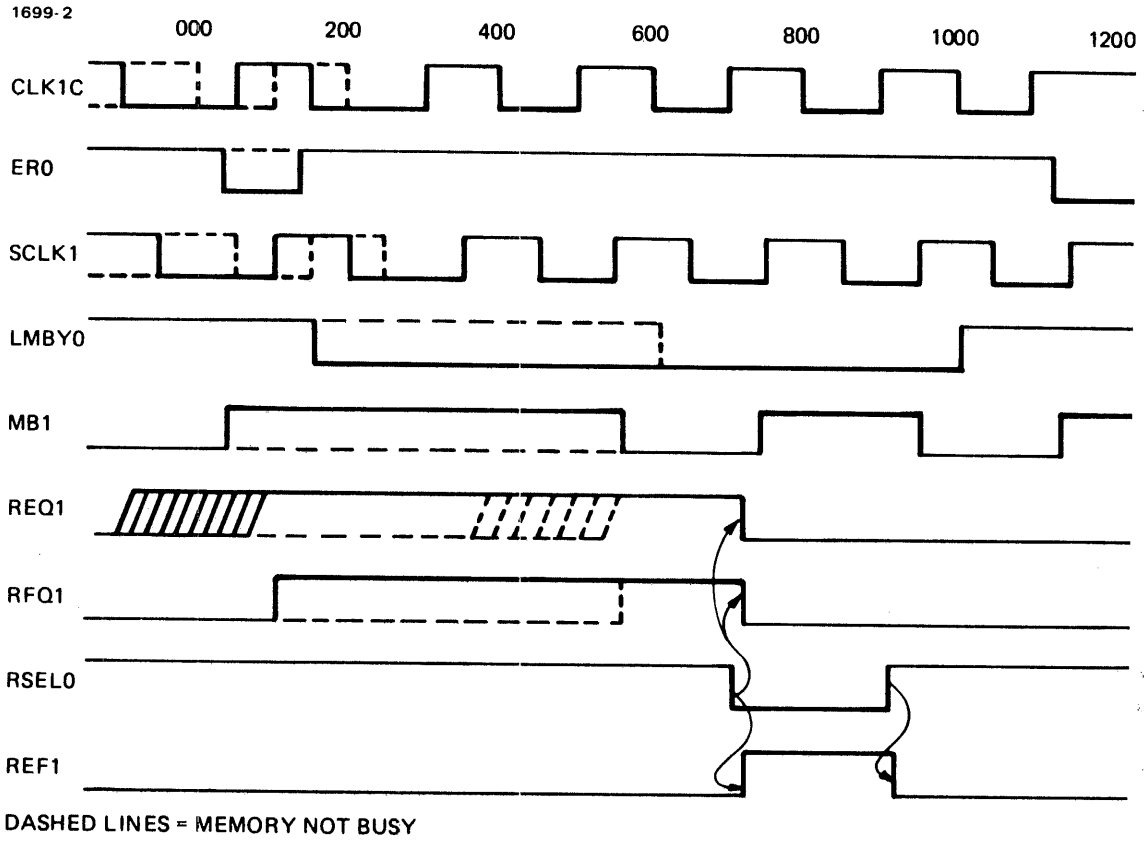


Figure 18-1 Refresh Cycle Steal Timing

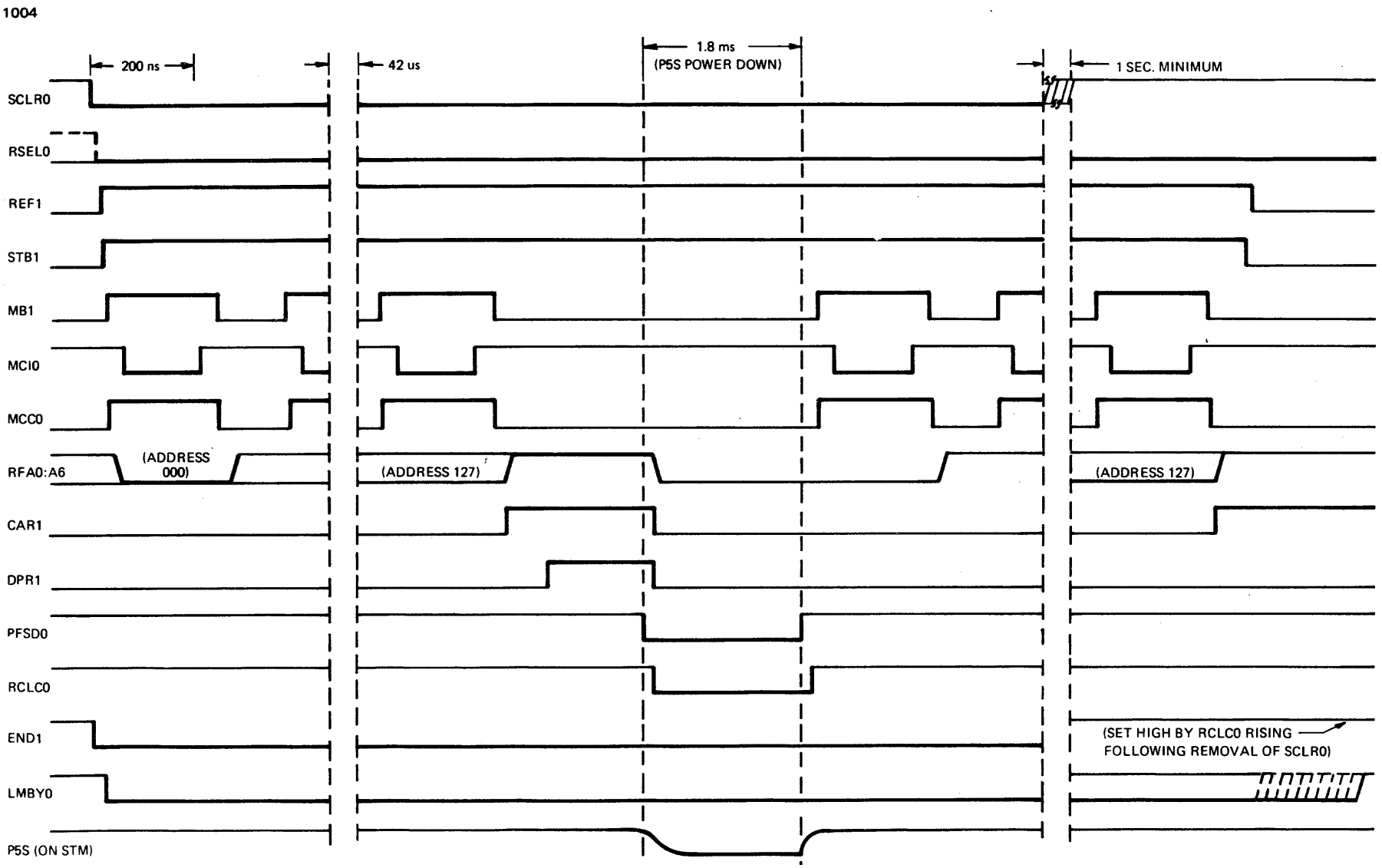


Figure 18-2 Burst Refresh Timing (128 Cycles)

18.2.1.1 Burst Mode

The burst mode is entered whenever the consolette INITIALIZE switch is depressed or the KEY switch is placed to the OFF position, causing the System Clear (SCLR0) line to go active. SCLR0 (13C3) causes REF1 (13C3) to go active, enabling the refresh address driver 11C (3M2) and setting the MB1 flip-flop. MB0 sets the TA001 flip-flop (16B6), starting the TA timer, which causes MCI0 (16S5) to go active and initiate the refresh cycle to the STM(s). With MREF0 (9G5) active, all STMs in the system are enabled to perform the refresh cycle (refer to the chapter on the STM for a detailed description).

When TA201 (13G8) goes high, the refresh counter (13J5 and 13M5) is advanced and the MB1 flip-flop (13K7) is cleared. This causes MCC0 (9G2) to go active, ending the first refresh cycle. When TA181 (13G8) goes low, the MB1 flip-flop (13K7) is directly set, starting the next refresh cycle. This mode of operation continues for 256 cycles allowing the DPR1 flip-flop (13J2) to be clocked set and PFSD (13N2) to be activated. PFSD0 (9R4) going active causes the STM(s) P5S regulator to shut down, placing it into a low power standby mode and activating RCLC0 (9N5). RCLC1 (13E4) causes the refresh counter (13J5 and 13M5) and the DPR1 flip-flop (13J2) to be cleared, allowing the 1.8 ms one-shot (13M2) to time out and deactivate PFSD1. PFSD0 (9R4) going inactive causes the STM(s) P5S regulator to turn on, deactivating RCLC0 (9N5), thereby setting the MB1 flip-flop (13K7) and initiating a 128 cycle burst. A 128 cycle burst is then performed every 1.8 msec.

This mode of operation continues until SCLR0 is brought high by returning the System Control Panel KEY switch to the ON position and timing out the initialize function. This causes the END1 flip-flop (13F5) to be clocked set after completing a 256-cycle burst, allowing the STB1 flip-flop (13H1) to be clocked reset at the end of that burst. STB1 going low causes REF1 (13K3) and REF0 (13L3) to go inactive, allowing LMBY0 (15N8) to be returned high, indicating to the processor that the memory is ready to accept a command. Memory refreshing is continued by performing a single refresh cycle steal every 16 microseconds.

18.2.1.2 Cycle Steal Refresh

A refresh cycle steal is initiated whenever the free-running 16 microsecond oscillator (13B2) clocks the REQ1 flip-flop (13D2) set, thereby allowing the RFQ1 flip-flop (15K7) to queue up this request. Flip-flop 07A (13E2) and the RSEL0 flip-flop (13F2) are used to further synchronize the start and end of the refresh cycle to prevent overlapping of memory operations. Operation in the refresh cycle steal mode is identical to the burst refresh cycle, with the exception that only one cycle is executed and the DPR1 flip-flop (13J2) is never activated.

18.2.2 LBC Operating Modes

The LBC operates in a number of different modes (refer to Table 18-2) as determined by the states of ROM data lines RD011:031 (3E7), WRT0 (3A6), DMAHW0 (3A6), PSEL1 (3A6) and LMA190 (3A5) at the time ER0 (13G7) goes active. These signals are loaded into transparent latches whose outputs drive the mode selector logic consisting of one of eight decoders 20F (14C3) and 20J (14C5) and miscellaneous gate functions (left half of Sheet 14). For any given operation, certain mode decoder outputs go active (refer to Table 18-2), setting up the control logic for the specific data manipulation required.

TABLE 18-2 LBC OPERATING MODES

1873-1

MATRSD0	MATRSR0	DRST0	PSELIA	WRT0	RD 011	RD 021	RD 031	PROCESSOR OPERATIONS	MODE DECODER OUTPUTS ACTIVE (See Sheet 14 35-771D08)
1	1	1	1	0	0	0	0	No Memory Operation	
1	1	1	1	0	0	0	1	Store Byte	SBY1, SPW1, SPW0
1	1	1	1	0	0	1	0	Store Halfword (Privileged)*	SHW1, SPW1, SPW0
1	1	1	1	0	0	1	1	Store Halfword (Data)*	SHW1, SPW1, SPW0
1	1	1	1	0	1	0	0	Test Error Logger (Store Byte)	TEL0, TEL1, SBY1
1	1	1	1	0	1	0	1	No Memory Operation	
1	1	1	1	0	1	1	0	Store Fullword (Privileged)*	SFW1, SFW0
1	1	1	1	0	1	1	1	Store Fullword (Data)*	SFW1, SFW0
1	1	1	1	1	0	0	0	No Memory Operation	
1	1	1	1	1	0	0	1	Read and Set Halfword	RST0, RST1, SPW1, ROAST1
1	1	1	1	1	0	1	0	Read Halfword (Privileged)* (Fullword Operation)	PRFW0, PRFW1, RFW1, ROAST1
1	1	1	1	1	0	1	1	Read Halfword (Data)* (Fullword Operation)	PRFW0, PRFW1, RFW1, ROAST1
1	1	1	1	1	1	0	0	Read Error Logger	EL0, REL1 (active with LMA190 high), ELST1 (active with LMA190 low)
1	1	1	1	1	1	0	1	Read Fullword (Instruction Read)*	PRFW0, PRFW1, RFW1, ROAST1
1	1	1	1	1	1	1	0	Read Fullword (Privileged)*	PRFW0, PRFW1, RFW1, ROAST1
1	1	1	1	1	1	1	1	Read Fullword (Data)*	PRFW0, PRFW1, RFW1, ROAST1
			PSELIA	WRT0	DMAHW0			DMA Operations	
1	1	1	0	0	0			Store Halfword	SHW1, SPW1, SPW0
1	1	1	0	0	1			Store Fullword	SFW1, SFW0
1	1	1	0	1	0			Read Halfword (Fullword Operation)	DRFW0, DRFW1, RFW1, ROAST1
1	1	1	0	1	1			Read Fullword (Fullword Operation)	DRFW0, DRFW1, RFW1, ROAST1
1	1	0						DMA Read and Set	DRST0
1	0	1						MAT Read and Set Reference Bit	MATRSR0
0	1	1						MAT Read and Set Dirty Bit	MATRSD0

*LBC does not differentiate between privileged and data instruction.

There are five basic functional modes used by the LBC to service all operations. They are:

1. Store Fullword (Figure 18-3)
2. Store Partial Word (Figure 18-4) including:
   - store byte
   - store halfword
   - read and set
   - test error logger
3. Read Fullword or DMA read (Figure 18-5)
4. Read Error Logger Status (LMA190 low) (Figure 18-6B)
5. Read Error Logger (LMA190 high)

   (Refer to Figure 18-6A)

NOTE

All read halfword operations are decoded as read fullword operations by the LBC. Data steering for halfword operations is performed on the CPU-C board.

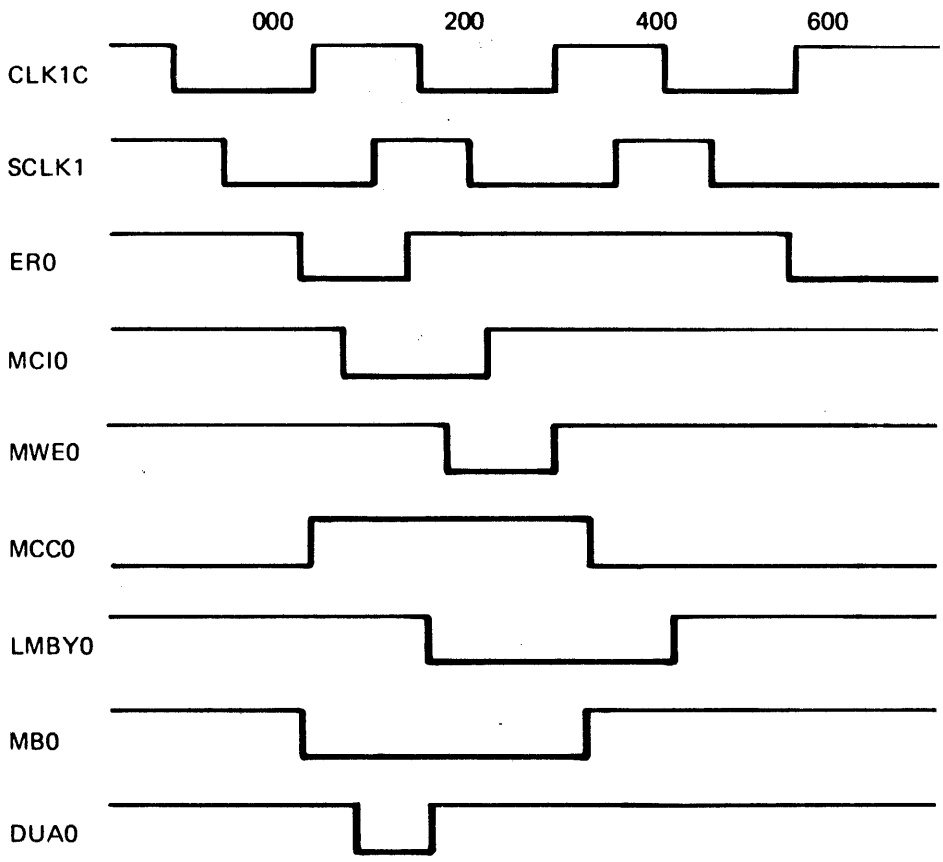


Figure 18-3 Store Fullword

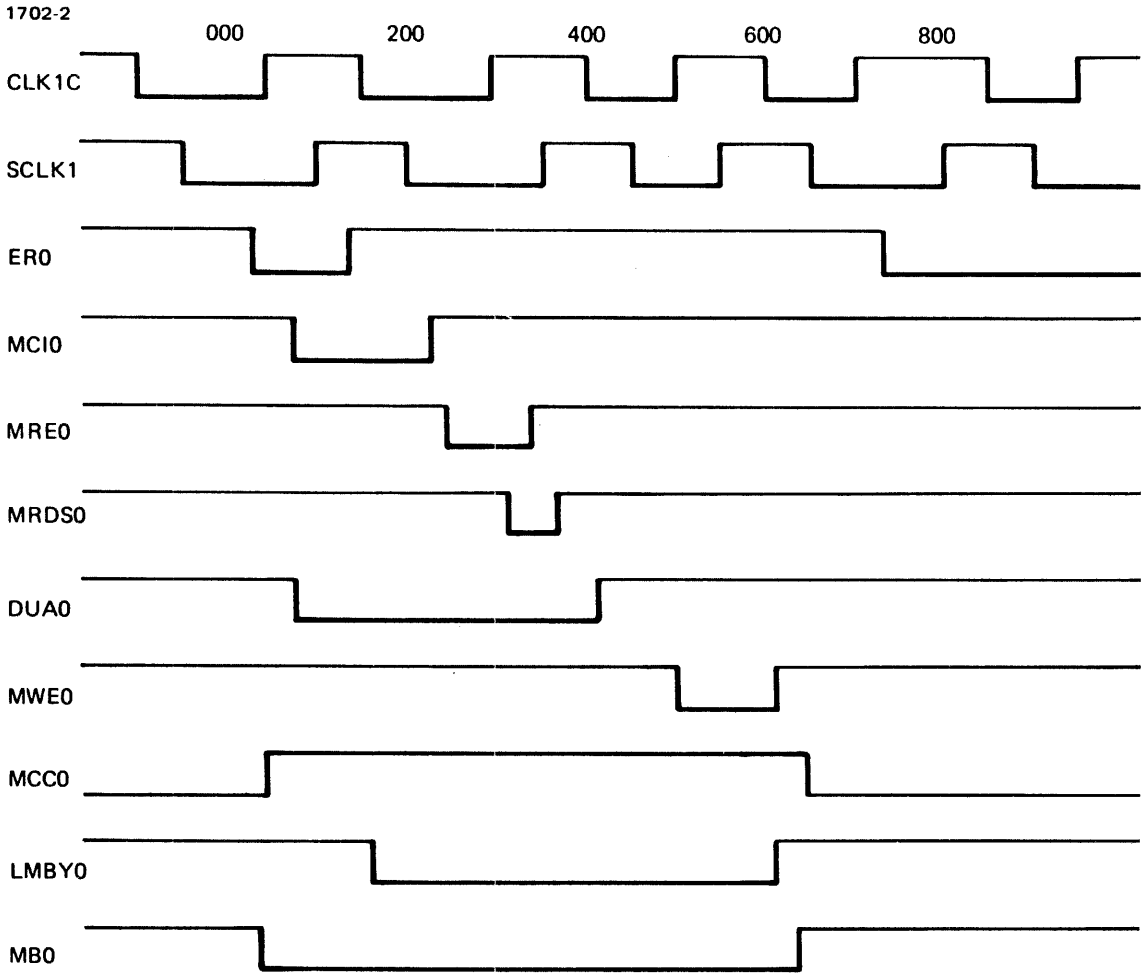


Figure 18-4 Store Partial Word

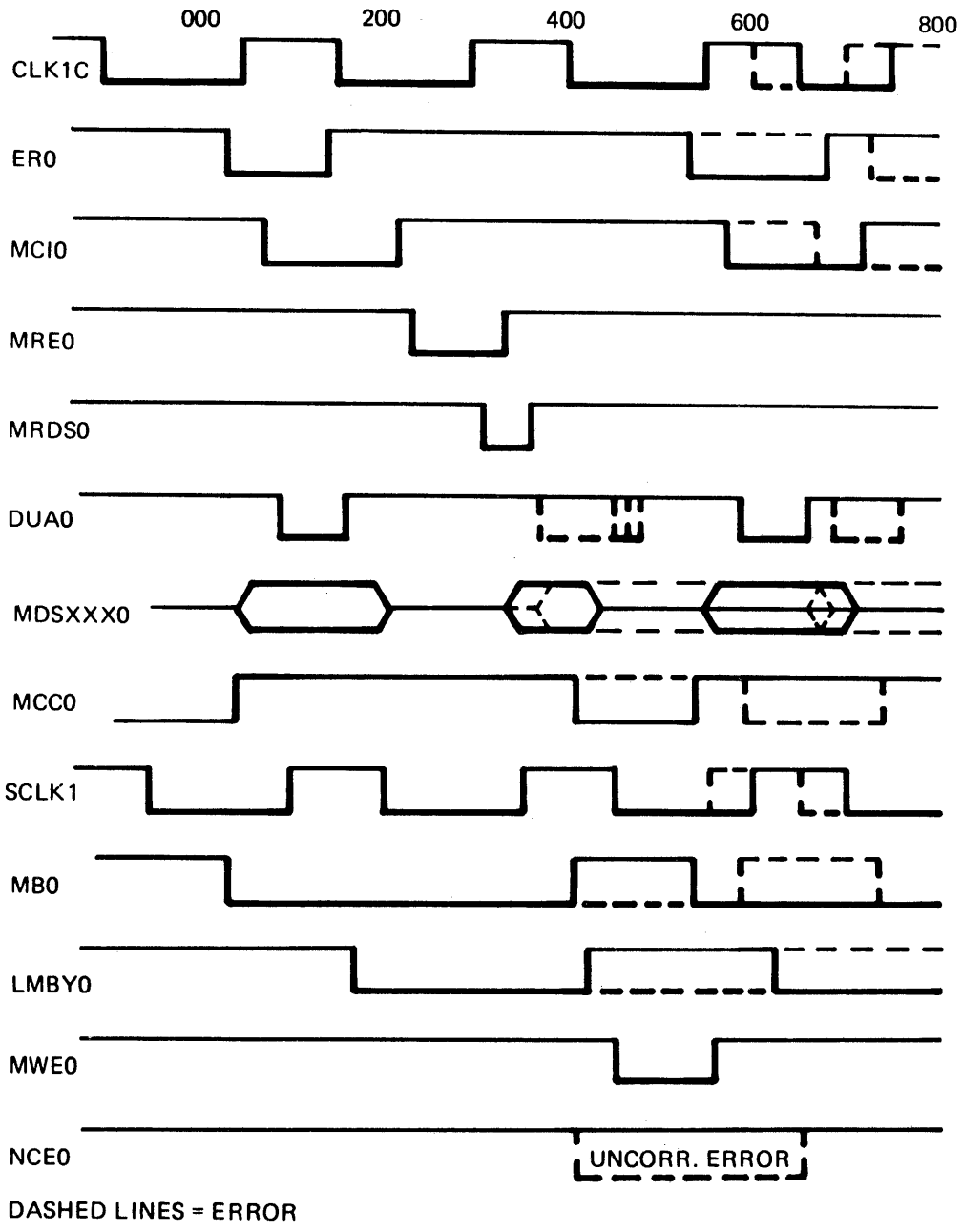
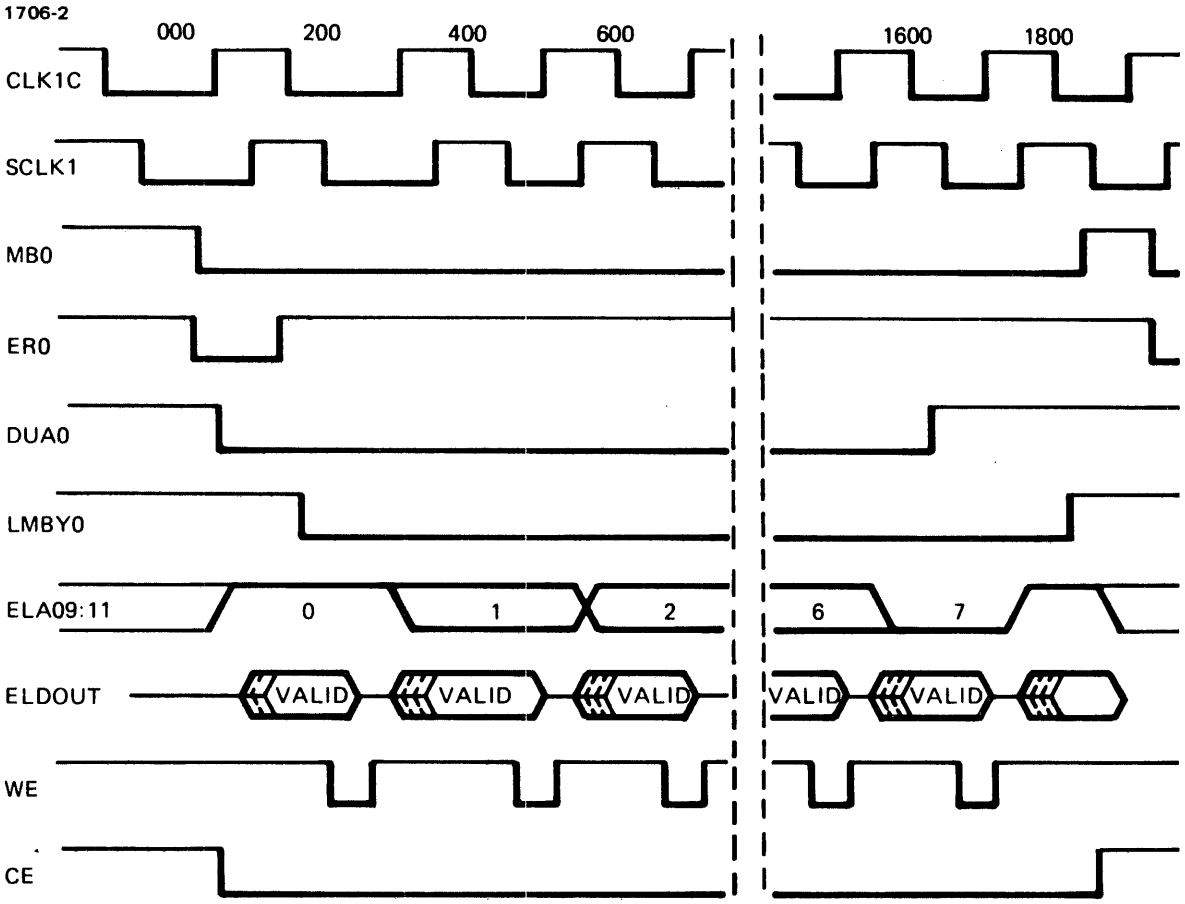
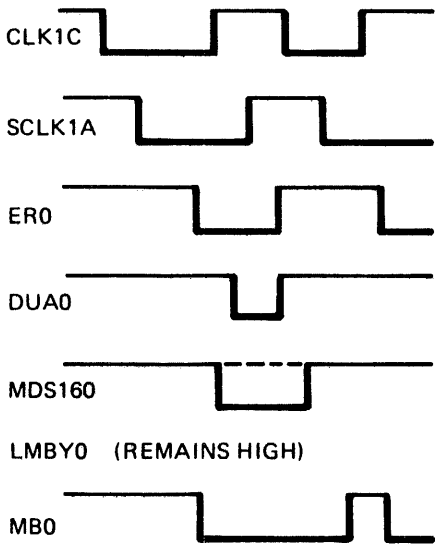


Figure 18-5 Read Fullword



A. Read Error Logger



B. Read Error Logger Status

Figure 18-6 Read Error Logger Status

Timing diagrams for the A and B timers are provided in Figures 18-7 and 18-8. Table 18-3 provides data and address bus alignment information. The subsequent sections describe each of the five basic functional modes.

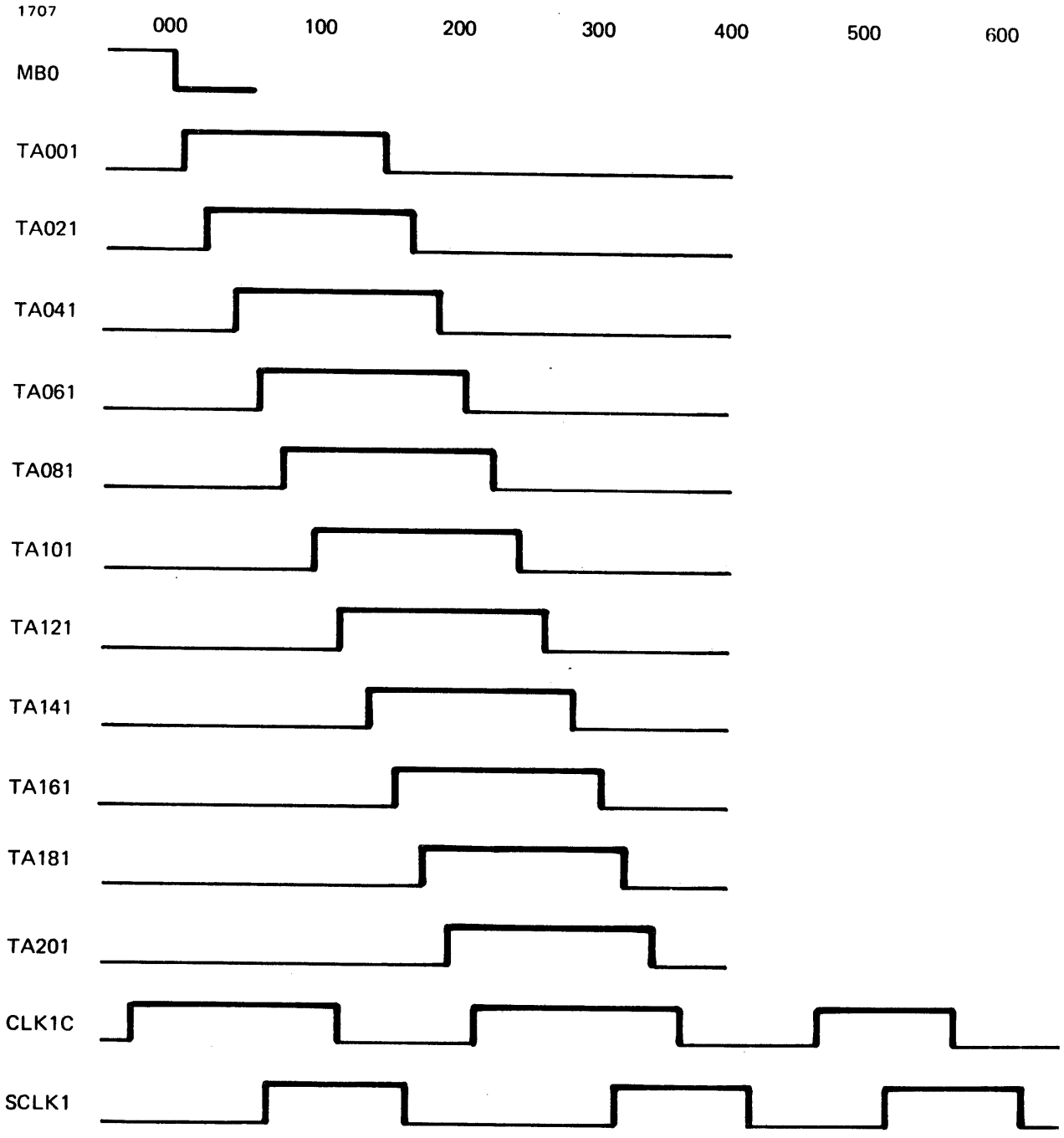
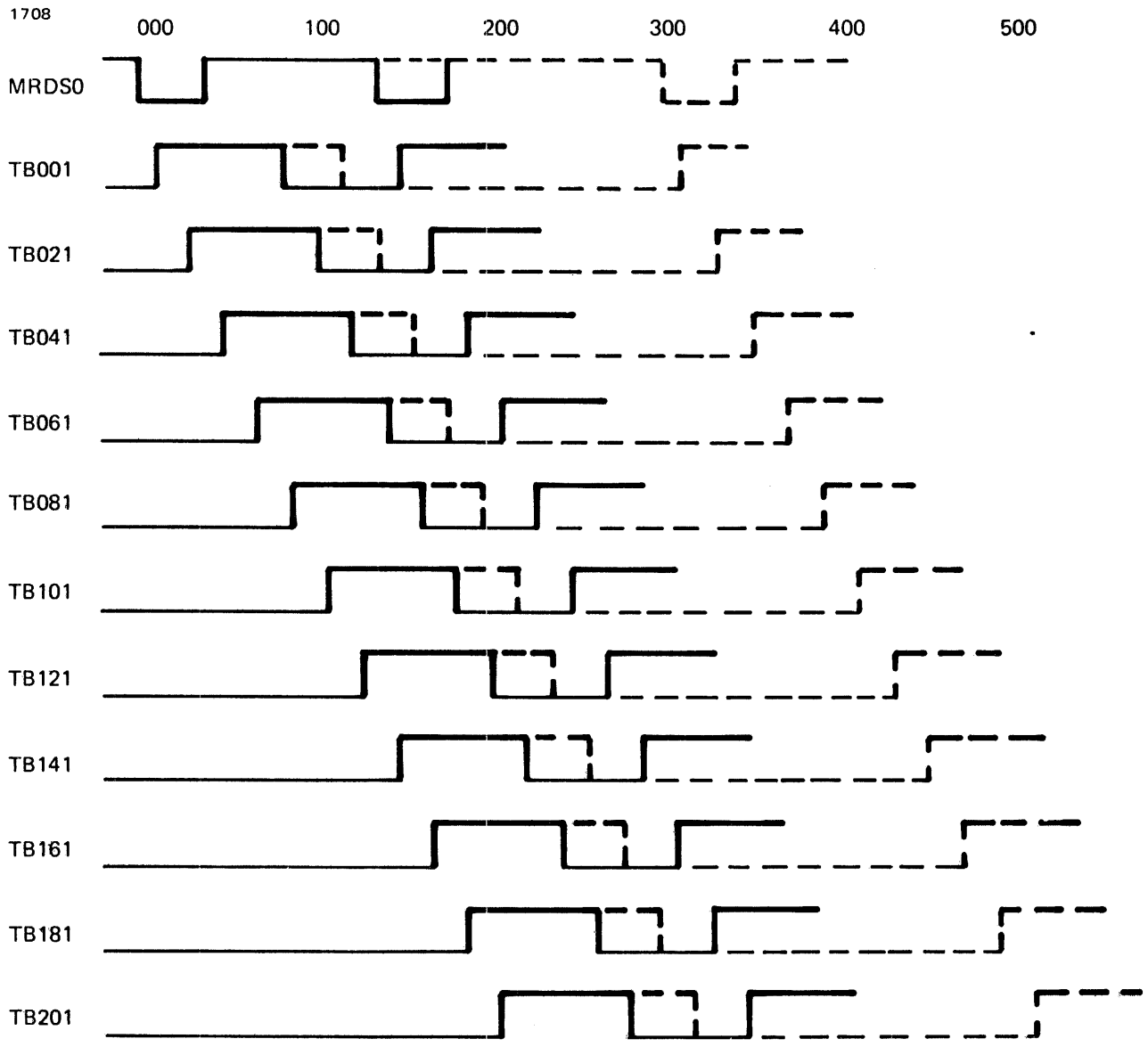


Figure 18-7 A Timer



DASHED LINES = READ FULLWORD OPERATION WITH ERROR

Figure 18-8 B Timer

TABLE 18-3 MEMORY SYSTEM DATA AND ADDRESS BUS ALIGNMENT

1887

LMA	080	090	100	110	120	130	140	150	160	170	180	190	200	210	220	230	240	250	260	270	280	290	300	310
LMB							001	011	021	031	041	051	061	071	081	091	101	111	121	131	141	151		
MEA		000	010	020	030																			
MX					021	011 031																		
MWA																					000	010		
ERROR LOG ADDRESS		ERR. LOG. 1/2 SLCT.	0 (MODULE NO.)	1 (MODULE NO.)	2 (MODULE NO.)	3 (MODULE NO.)	4 (WORD COLUMN)	5 (WORD COLUMN)	6 S0	7 S1	8 S2	ST. BIT												

18.2.2.1 Store Fullword

A store fullword cycle is initiated at the processor by setting up the write data lines MDS000:310 (2A4), address lines LMA080:310 (3A1-3A9), write control line WRT0 (3A6), and mode control lines DMAHW0 (3A6), PSEL1, and RD011:031 (3A7). After these lines are set up, the processor generates an ER0 (13G7), clocking the MB1 flip-flop set, thereby starting the memory cycle. MB1 going active causes write data to be latched in the input data register (2G8), addresses to be latched in the address register (3A), and the control lines in their respective registers (3A6). MB0 having set the TA timer flip-flop (16B6) causes MCI0 (16S5) to go active, latching up the address presented on LMB001:151 (3E5,3K2) into the STM selected by lines MEA030:000 (9G). After satisfying the STM address hold time, the EA0 flip-flop (16R5) is set, thereby tristating the LMB001:151 address drivers (3E5,3K2). TA101 (2R4 and 15B2) going active enables the input data register (2G8) and the data bus drivers (Sheets 8 and 9), placing the word to be written onto lines D000:310 and LMB000:310. Lines D000:310 are input to the parity generators (4C5,4F5), whose outputs P000:060 propagate through the write parity register (7F7) onto lines GP000:060. This causes the parity data to be placed onto lines LMB321:381 by the parity data drivers (9E8). TAA121 (15A4) causes WE0 to go low, activating MWE0 (9G3), allowing the data present on lines LMB001:381 to be written into the selected STM. Following the removal of WE1 (14J3), NCLR1 (14R4) goes active, clearing the MB1 flip-flop (13K7) which enables MCC0 (9G2). With MCC0 activated, the write cycle is completed and CLK0D (15M9) causes LMBY0 to go high, signaling to the processor that the memory is no longer busy.

18.2.2.2 Store Partial Word

A store partial word cycle is initiated in the same way as described in the store fullword description. The cycles differ in that the word to be modified must be read from the STM before performing the write. This is necessary to allow new parity data to be generated from the modified word. The following description continues from the point just prior to enabling the input data register, as described in the store fullword operation.

WDEN0 (2R4) going active enables the input data register (2G8), placing the byte (store byte operation or test error log operation) or halfword (store halfword operation) of write data onto data lines D000:310. WDEN0 (14K9) also activates LDBY01:31, causing D000:310 to be loaded into the Good Data Registers (GDR) (Sheet 6).

NOTE

WDEN0 does not go active during a read and set operation.

TA161 (15G1) going active sets the RE1 flip-flop (15J3) which, in turn, activates the Uncorrected Data Register (UDR) (Sheets 8 and 9) and MRE0 (9G1). The STM responds in 240 nanoseconds by activating MRDS0 (9G6), signaling that lines LMB001:381 have been loaded with the read data. RDS0 causes the RE1 flip-flop (15J3) to be reset, removing MRE0 (9G1), latching the UDR (Sheets 8 and 9) and starting the TB timer (16B2). Data lines D000:310 and UP000:060 propagate through the parity checkers (Sheets 4 and 5), generating the Error Check and Correction (ECC) syndrome code on lines P000:060. If no data bit errors are generated, the syndrome code lines are all low deactivating MER0 (5N2). If a single data bit is in error, MER0 goes low along with one output from the DC error decoder (5J8) and one output from the DA or DB error decoder. One of the correction lines EB000:310 (Sheet 6) or EPB000:060 (7C4) goes high, causing the data bit in error to be input to the GDR (Sheet 6) or Good Parity Register (GPR) (7F4) to be corrected (inverted). If any two data bits are in error, MER0 goes low, correction lines EB000:310 and EPB000:060 remain low (no correction), and the uncorrectable error decoder (7M5) goes low allowing the UCE0 flip-flop (7N4) to be activated. UCE0 at AOI gate 20K (15B2) prevents activating ED1 and ED0 when the modified word is written back into the STM, causing all logical ones to be stored in the STM. This is necessary because the new parity data generated could otherwise make the data appear error free on subsequent reads from this location. TB021 (14G9) going active causes LDGP1 (read and set or test error logger operation only) and select LDBY01:31 lines (14M7) to go active, thereby loading the part of the word not to be modified into the GDRs (Sheet 6). TB080 (14G9) going low deactivates LDBY01:31 and UDD0 (15L4) and activates GDD1 (15N4), placing the modified word onto lines D000:310 (Sheet 6). New parity data is generated from this word and appears on lines P000:060 (Sheets 4 and 5) which are loaded into the write parity register (7F7) and output on lines GP000:060.

NOTE

A test error logger operation does not store away new parity data, but it uses the old parity by enabling the GPR (7F4) onto lines GP000:060.

A read and set operation differs from the above description in that the entire word from the STM is loaded into the GDR and, in turn, output to the processor from the output data register (see read fullword operation for description). Additionally, the most significant bit of the halfword D000 or D160 (15G6), as addressed by LMA140, is set on write data line D000A or D160A (15K6) if MATRS0, DMARS0, or RST0 are activated. D020A is set on write data line D020A if MATRSD0 is activated.

TBB141 (15A2) activates ED1 and ED0, placing the modified word data and parity data onto lines LMB001:381 (Sheets 8 and 9). TB161 (15A4) causes WE0 and MWE0 (9G3) to go active, placing the

STM in the write mode. WE1 (14J3) going inactive causes NCLR1 (13G9) to reset the MB1 flip-flop (13K7), enabling MCC0 (9G2). LMBY0 (15N8), having gone high at the previous edge of CLK0D, signals to the processor that the cycle is complete and the memory is no longer busy.

A DMA read and set and MAT read and set operation is similar to a regular read and set operation, except that only bit 0 is set.

A MAT read and set dirty bit is also similar to a regular read and set operation except that bit 2 is set.

18.2.2.3 Read Fullword

A read fullword operation begins with the processor setting up the address bus and control lines to their appropriate states followed by the initiation of the cycle with ER0 (13G7) being activated. ER0 sets the MB1 flip-flop (13K7), causing the address register (3B) and control registers (3B, 3E) to be latched and the TA timer flip-flop (16B6) to be set. Lines MX011:031, LMB001:151, and MEA000:030 (Sheet 9) are presented with the address which is latched into the selected STM by MCI0 (16S5). After satisfying the STM address hold time, EA0 (16S4) going active tristates the address drivers (3E5,3J3,9K9).

TA161 (15G1) going active sets the RE1 flip-flop (15J3) which, in turn, activates the UDR (Sheets 8 and 9) and MRE0 (9G1). The STM responds in 240 nanoseconds by activating MRDS0 (9G6) signaling that lines LMB001:381 have been loaded with the read data. RDS0 causes the RE1 flip-flop (15J3) to be reset, removing MRE0 (9G1), latching the UDR (Sheets 8 and 9) and starting the TB timer (16B2). Data lines D000:310 and UP000:060 propagate through the parity checkers (Sheets 4 and 5), generating the Error Check and Correction (ECC) syndrome code on lines P000:060. If no data bit errors are generated, the syndrome code lines are all low deactivating MER0 (5N2). If a single data bit is in error, MER0 goes low along with one output from the DC error decoder (5J8) and one output from the DA or DB error decoders. One of the correction lines EB000:310 (Sheet 6) or EPB000:060 (7C4) goes high, causing the data bit input to the GDR (Sheet 6) or GPR (7F4) to be corrected (inverted). If any two data bits are in error, MER0 goes low, correction lines EB000:310 and EPB000:060 remain low (no correction), and the uncorrectable error decoder (7M5) goes low, allowing the UCE0 flip-flop (7N4) to be activated.

TB080 causes lines LDBY01:31 and LDGP1 (14M6) to load and enable the GDRs (Sheet 6) and the GPR (7F3), placing the data (corrected) onto lines D000:310 and GP000:060. 0DD1 (16N3) going active places this data onto the MDS000:310 lines (2A5) for the processor. If an error has been detected, TBB101 (15A1) activates ED1 and ED0 enabling the write data drivers (Sheets 8 and 9) onto LMB001:381; TBB121 (15A3) activates WE0, enabling MWE0 (9G4); and WE0 (14J3) going inactive causes NCLR1 (13G9) to reset the MB1 flip-flop (13K7). If no errors were detected, NE1

(14J2) going active causes NCLR1 (13G9) to reset the MB1 flip-flop (13K7). CLK0D (15M9) going active with DUA0 inactive raises the LMBY0 line, signaling to the processor that the memory is no longer busy.

18.2.3 Read Error Logger (Including ECC Description)

The error logger consists of a 16K x 1 (four 4k x 1 RAMs) buffer (10L8), an address multiplexor (10F1), a 16-bit shift register (10K1 and 10G2), a shift address generator (10B3), a syndrome code register (10C8), two Error Status flip-flops (10K4), and control circuitry (Sheet 10).

18.2.3.1 ECC Circuit Description

The Error Check and Correction (ECC) circuitry (Sheets 4 through 7) consists of parity/syndrome generators P000:060 (Sheets 4 and 5); error detector MER0 (5M3); first-level error decoders DA0:7, DB0:7, and DC0:7 (5J7); correction bit decoders EB000:160 (Sheet 6) and EPB000:060; uncorrectable error detector (UCE0) with LED display indicator (7M5 and 7R7); and Exclusive-OR bit correction gates (Sheets 6 and 7). The ECC code implemented provides detection and correction of all single-bit errors and detection of all double-bit error combinations.

The Error Correction Code (ECC) logic is used to generate the proper parity bits (P00:P06) when writing into the STM (LMB32:LMB37) or to check the 39-bit data word read from the STM.

When writing into memory, the data to be written is available on D00:D31. The seven parity bits (UP00:UP06) are forced low. The resulting parity bit (P00:P06) outputs, along with the 32-bit data word, are written to the STM. (Refer to Table 18-4.)

Reading from the STM fetches a 39-bit data word, which is provided on the inputs of the ECC logic (D00:D31 and P00:06). The syndrome output should be all zero if there is no error. (Refer to Table 18-5.) The syndrome output bits (P00:P06) are decoded to correct any single-bit error. Refer to Table 18-5 for decoding the syndrome bits after a read operation.

TABLE 18-4 ERROR CORRECTION CODE (ECC) LOGIC TABLE

1003

PARITY TO BE WRITTEN ON WRITE

DATA TO BE WRITTEN ON WRITE

FORCED LOW ON WRITE

P00:06

D000:310 (LOW ACTIVE BUS)

UP00:06

0	1	2	3	4	5	6	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	0	1	2	3	4	5	6	PARITY TYPE
X							X	X	X		X	X	X		X					X			X					X			X						X	X		X							ODD
	X						X			X	X	X		X		X			X		X			X			X			X		X					X			X						EVEN
		X						X		X	X		X	X			X		X			X				X			X			X						X	X			X				ODD
			X						X			X	X	X				X			X	X	X				X			X	X	X							X						EVEN
				X			X	X	X	X					X	X	X	X					X	X	X	X									X				X			X				ODD
					X										X	X	X	X	X	X	X	X					X	X	X	X	X	X	X	X	X						X				EVEN
						X																	X	X	X	X	X	X	X	X																X	EVEN

X = BITS USED TO GENERATE SYNDROME

ON READ SYNDROME OUTPUTS SHOULD BE ZERO IF NO ERROR

DATA READ FROM THE STM

EXAMPLE: DATA TO BE WRITTEN = X'00000000' PARITY GENERATED = 1001000

DATA READ AFTER WRITE = X'80000000' PARITY READ = 1001000 SYNDROME RESULT = 1100100 DATA BIT 0 ERROR (SEE TABLE 13-4)

TABLE 18-5 ECC SYNDROME CODE

S000	S010	S020	S030	S040	S050	S060	ERROR	LOCATION
0	0	0	0	0	0	0	NE	0
0	0	0	0	0	0	1	PB6	1
0	0	0	0	0	1	0	PB5	2
0	0	0	0	0	1	1	ME	3
0	0	0	0	1	0	0	PB4	4
0	0	0	0	1	0	1	ME	5
0	0	0	0	1	1	0	ME	6
0	0	0	0	1	1	1	DB28	7
0	0	0	1	0	0	0	PB3	8
0	0	0	1	0	0	1	ME	9
0	0	0	1	0	1	0	ME	10
0	0	0	1	0	1	1	DB27	11
0	0	0	1	1	0	0	ME	12
0	0	0	1	1	0	1	DB19	13
0	0	0	1	1	1	0	DB11	14
0	0	0	1	1	1	1	ME	15
0	0	1	0	0	0	0	PB2	16
0	0	1	0	0	0	1	ME	17
0	0	1	0	0	1	0	ME	18
0	0	1	0	0	1	1	DB26	19
0	0	1	0	1	0	0	ME	20
0	0	1	0	1	0	1	DB18	21
0	0	1	0	1	1	0	DB10	22
0	0	1	0	1	1	1	ME	23
0	0	1	1	0	0	0	ME	24
0	0	1	1	0	0	1	DB23	25
0	0	1	1	0	1	0	DB15	26
0	0	1	1	0	1	1	ME	27
0	0	1	1	1	0	0	DB31	28
0	0	1	1	1	0	1	ME	29
0	0	1	1	1	1	0	ME	30
0	0	1	1	1	1	1	ME	31
0	1	0	0	0	0	0	PB1	32
0	1	0	0	0	0	1	ME	33
0	1	0	0	0	1	0	ME	34
0	1	0	0	0	1	1	DB25	35
0	1	0	0	1	0	0	ME	36
0	1	0	0	1	0	1	DB17	37
0	1	0	0	1	1	0	DB9	38
0	1	0	0	1	1	1	ME	39
0	1	0	1	0	0	0	ME	40
0	1	0	1	0	0	1	DB22	41
0	1	0	1	0	1	0	DB14	42
0	1	0	1	0	1	1	ME	43
0	1	0	1	1	0	0	ME	44
0	1	0	1	1	0	1	ME	45
0	1	0	1	1	1	0	ME	46
0	1	0	1	1	1	1	ME	47

TABLE 18-5 ECC SYNDROME CODE (Continued)

S000	S010	S020	S030	S040	S050	S060	ERROR	LOCATION
0	1	1	0	0	0	0	ME	48
0	1	1	0	0	0	1	DB20	49
0	1	1	0	0	1	0	DB12	50
0	1	1	0	0	1	1	ME	51
0	1	1	0	1	0	0	DB3	52
0	1	1	0	1	0	1	ME	53
0	1	1	0	1	1	0	ME	54
0	1	1	0	1	1	1	ME	55
0	1	1	1	0	0	0	DB7	56
0	1	1	1	0	0	1	ME	57
0	1	1	1	0	1	0	ME	58
0	1	1	1	0	1	1	ME	59
0	1	1	1	1	0	0	ME	60
0	1	1	1	1	0	1	ME	61
0	1	1	1	1	1	0	ME	62
0	1	1	1	1	1	1	ME	63
1	0	0	0	0	0	0	PB0	64
1	0	0	0	0	0	1	ME	65
1	0	0	0	0	1	0	ME	66
1	0	0	0	0	1	1	DB24	67
1	0	0	0	1	0	0	ME	68
1	0	0	0	1	0	1	DB16	69
1	0	0	0	1	1	0	DB8	70
1	0	0	0	1	1	1	ME	71
1	0	0	1	0	0	0	ME	72
1	0	0	1	0	0	1	DB21	73
1	0	0	1	0	1	0	DB13	74
1	0	0	1	0	1	1	ME	75
1	0	0	1	1	0	0	DB2	76
1	0	0	1	1	0	1	ME	77
1	0	0	1	1	1	0	ME	78
1	0	0	1	1	1	1	ME	79
1	0	1	0	0	0	0	ME	80
1	0	1	0	0	0	1	ME	81
1	0	1	0	0	1	0	DB30	82
1	0	1	0	0	1	1	ME	83
1	0	1	0	1	0	0	DB1	84
1	0	1	0	1	0	1	ME	85
1	0	1	0	1	1	0	ME	86
1	0	1	0	1	1	1	ME	87
1	0	1	1	0	0	0	DB6	88
1	0	1	1	0	0	1	ME	89
1	0	1	1	0	1	0	ME	90
1	0	1	1	0	1	1	ME	91
1	0	1	1	1	0	0	ME	92
1	0	1	1	1	0	1	ME	93
1	0	1	1	1	1	0	ME	94
1	0	1	1	1	1	1	ME	95

TABLE 18-5 ECC SYNDROME CODE (Continued)

S000	S010	S020	S030	S040	S050	S060	ERROR	LOCATION
1	1	0	0	0	0	0	ME	96
1	1	0	0	0	0	1	ME	97
1	1	0	0	0	1	0	DB29	98
1	1	0	0	0	1	1	ME	99
1	1	0	0	1	0	0	DB0	100
1	1	0	0	1	0	1	ME	101
1	1	0	0	1	1	0	ME	102
1	1	0	0	1	1	1	ME	103
1	1	0	1	0	0	0	DB5	104
1	1	0	1	0	0	1	ME	105
1	1	0	1	0	1	0	ME	106
1	1	0	1	0	1	1	ME	107
1	1	0	1	1	0	0	ME	108
1	1	0	1	1	0	1	ME	109
1	1	0	1	1	1	0	ME	110
1	1	0	1	1	1	1	ME	111
1	1	1	0	0	0	0	DB4	112
1	1	1	0	0	0	1	ME	113
1	1	1	0	0	1	0	ME	114
1	1	1	0	0	1	1	ME	115
1	1	1	0	1	0	0	ME	116
1	1	1	0	1	0	1	ME	117
1	1	1	0	1	1	0	ME	118
1	1	1	0	1	1	1	ME	119
1	1	1	1	0	0	0	ME	120
1	1	1	1	0	0	1	ME	121
1	1	1	1	0	1	0	ME	122
1	1	1	1	0	1	1	ME	123
1	1	1	1	1	0	0	ME	124
1	1	1	1	1	0	1	ME	125
1	1	1	1	1	1	0	ME	126
1	1	1	1	1	1	1	ME	127

NOTE

PB = Parity Bit
DB = Data Bit
ME = Multiple Bit Error

During a faulty read operation, data from the STM is input to the parity check generators causing one or more parity/syndrome lines P000:060 to go high and activating MER0 (5N2). These lines are also input to the first level decoders (5J5-5J8), whose outputs are further decoded by the correction bit generators (Sheet 6 and 7C3). If a single-bit error is detected, one correction line EB000:160 or EPB000:060 goes high (active), correcting the bit in error. If the error detected was not a single bit error, lines EB000:160 and EPB000:060 remain low (no correction) causing UCE0 (7N3) to go active and latching the address (1 of 4) of the faulty STM in the uncorrected error display (7R7).

18.2.3.2 Error Logger Description

The error logger records all detectable single and multiple bit memory errors (refer to Table 18-5). The error logger is divided in two, with the first half covering the lower 4 Mbs of memory and the other half covering the upper 4 Mbs of memory. The system only uses the first half of the error logger since there can only be 4 Mbs maximum. An error can be detected down to the 16k level.

Errors are recorded as follcws: parity/syndrome lines P000:060 are latched in the syndrome register (10C8) whose outputs S001:051 are steered onto error logger address lines ELA04:11, along with the word address lines WA000 and 010, via the address multiplexors (10D1 and 10D3). Line S061 is used, along with BA09, as the error log RAM chip enable (CE) decode. BA09 selects between the lower 4 Mb 4k x 1 RAMs, 17k and 14k (10J6 and 10M6), and the upper 4 Mb 4k x 1 RAMs, 16k and 15k (10J8 and 10M8). S061 selects between the two RAMs selected by BA09, placing all even errors (refer to Table 18-6) into 4k x 1 RAM 17k or 16k, and all odd errors into 4k x 1 RAMs 14k or 15k. STM module select lines ELMA11:31 and ERLA01 (10J6, 10J8, and 10L8) are input directly to the 4k x 1 RAMs as most significant addresses. ME1 (10H4) and ME0 (10N6), having gone active, cause a low to be written into the address location of the selected RAM, and set either flip-flop 02M (10K4) upper half of the error logger or flip-flop 05K (10K5), lower half of the error logger. These two flip-flops represent the status of their respective error logger halves.

There are two operations provided for obtaining error logger information, read error logger status, and read error logger. Both operations are initiated by sending the read error logger code on lines RD011:31 and setting address bit LMA190 for a read error logger status or resetting address bit LMA190 for a read error logger operation.

A read error logger status operation responds with line MDS160 being set if the error lcgger contains error information, or reset if no errors have been stored. LMA090 is used to select between the status for each error logger half; if LMA090 is reset, MDS160 returns status for the lower half of the error logger; and if LMA090 is set, MDS160 returns status for the upper

half of the error logger. The selected status flip-flop (10K4 or (10K5) is always reset when a read error logger status is performed.

A read error logger operation reads 16 consecutive locations of the error logger, returning a half-word on lines MDS160-310. LMA090 selects between the upper and lower half of the error logger. Address bits LMA100:180 are steered to the error logger RAMs (10J6, 10J8, 10M6, and 10M8) via the address multiplexor (3E1, 3E3), along with lines AD01:21 from the shift counter (10B3). The contents of eight address locations are read from each 4k x 1 RAM (operated in parallel) of the selected error logger half and loaded into their respective shift registers. Each address location is written back to a one (no error state) before reading out from the next address location. The timing used to perform this operation is derived from system clocks CLK1D and SCLK1A (10A4). After loading the shift registers, their contents are enabled onto lines D160:310, which output onto lines MDS160:310 through the output data register (Sheet 2). AD31 (14J2) going active causes NCLR1 (13G9) to reset the MB1 flip-flop (13K7), readying it to accept the next ER0. RCAR0 (10M3), having gone active, allows the ELDUAL1 flip-flop to be reset, removing DUA0 (15N7) and causing LMBY0 (15N8) to be deactivated on the next transition of CLK0D.

The halfword returned during a read error logger operation is interpreted as follows: each bit in the halfword represents 1 of 16 syndrome codes created by concatenating 4 bits with the 3-bit syndrome field (A160:180) sent to the LBC during the REL instruction. For example, if A16:18 were zeros when the REL instruction was executed, the halfword returned would represent syndrome codes 0000000 - 0001111, where bit 31 represents 0000000 and bit 16 represents 0001111. For every bit in the halfword that is set, an error has occurred with the corresponding syndrome. By using Table 18-5, the type of error can then be determined. The location of a chip in error, for errors that have been determined to be single-bit errors, can then be determined using the module number bits and the word column bits in the address field of the REL instruction (refer to Table 18-6).

When performing a read error logger or read error logger status operation, address bit LMA080 must be reset. If LMA080 is set, the operation is not performed and the LBC resets all bits on MDS160:310. Table 18-6 shows the addressing scheme for read error logger and read error logger status operations.

As stated earlier, the system only uses the lower half of the error logger since the maximum memory capacity is 4 Mb. Therefore, performing a read error logger status or read error logger operation with LMA090 set will yield meaningless results in all cases.

Every time P5 is turned off, the error logger is not powered; this means that every time P5 is turned on, the error logger contains invalid data and its status flip-flops may or may not be

set. A read error logger status operation and a read error logger operation must be perfcrmed for all error logger addresses in order to clear out the error logger that valid errors can then be recorded.

TABLE 18-6 ERROR LOGGER ADDRESSING SCHEME

1888-1

	ADDRESS BUS BITS (LMA)											
	080	090	100	110	120	130	140	150	160	170	180	190
READ ERROR LOGGER	MUST BE RESET	MUST BE RESET	MODULE NO. (0 - 15)				WORD COLUMN (0 - 3)		SYNDROME BITS S0	S1	S2	MUST BE RESET
READ ERROR LOGGER STATUS	MUST BE RESET	MUST BE RESET	NOT USED (DON'T CARES)									MUST BE SET

NOTE: LMA200:310 are not used (don't cares)

18.3 MNEMONICS

The following is a list of the mnemonics used on the LBC board. The meaning and 35-806D08 schematic source of each signal are provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
A080:A310	Internal address bus lines	Sheet 3
AD01:AD31	Shift counter bits	10C3
BA08O	Board Address 8	3F1
BA090/1	Board Address 9	3F1
BMCIO	Buffered memory cycle initiate	9M7
BMVFO	Buffered memory voltage failure line	9M9
BSCLRO	Buffered system clear	9M4
CAR1	Refresh ccunter carry	13N5
CB011:CB031	Control bits	3F8
CLKOD	Buffered prccessor clock	10A4
CLK1C	Processor clock	9L7
CLK1D	Buffered prccessor clock	7N8

MNEMONIC	MEANING	SCHEMATIC LOCATION
CLR0	Cycle steal clear	13D2
CLR0B	Clear DU circuit	15E7
CLTB1	TB timer feedback	16A1
CSTRIN00:10	Cycle steal refresh inhibit	13A3
D000:D310	Internal data bus lines	Sheets 2,6,8, 9,10,11
D000A	Test and set bit	15K5
D160A	Test and set bit	15K6
DA0:DA7	First-level error decode bits	5K6,5K7
DB0:DB7	First-level error decode bits	5K5,5K6
DC0:DC7	First-level error decode bits	5K8,5K9
DERR0	Disable error correction line	5G6
DHW0	Buffered DMA halfword line	3C6
DMAHW0	DMA halfword line	3A6
DMARS0	DMA read and set	3D9
DMARST0	DMA read and set latched	3F9
DPR1	Depower line	13K2
DRFW0/1	DMA read fullword	14E7
DREL1	Data read error logger	14H5
DSFW0	DMA store fullword	14D4
DSHW0	DMA store halfword	14D3
DUA0/1	Data unavailable	15N7
EA0/1	Enable address flip-flop	16S4
EB000:EB310	Data bit correction lines	Sheet 6
ED0/1	Enable data lines	15G1
ELMA00:30	Error logger and module address	3G2,3F3
EL0	Error logger select line	14G4
ELA04:ELA11	Error logger address lines	Sheet 10
ELDUA0/1	Error logger data unavailable	10G4
ELST1	Error logger status select line	14H5
END1	Standby end flip-flop	13F5
EPB000:EPB310	Parity bit correction lines	Sheet 7
ER0	Memory cycle start	13G7
ERLA01	Error logger address 0	3F1
EWE1	End write enable flip-flop	15F3
FNPM0/1	Nonpresent memory flip-flop	14S5
GDD1	Good data disable flip-flop	15N4
GMVF0	Nonpresent memory or memory voltage fail	9N7
GP000:GP060	Good parity lines	7H2,7H4
LD01	Error logger RAM output	10K8
LD02	Error logger RAM output	10N7
LDBY01:LDBY31	Load byte	Sheet 14
LDGP1	Load good parity line	14M5
LDOD1	Load output data register	16K9
LMA080:310	Local memory address lines	Sheet 3
LMB001:381	Local memory bus lines	Sheets 3,8,9
LMBY0/1	Local memory busy flip-flop	15N8

MNEMONIC	MEANING	SCHEMATIC LOCATION
MATDO	MAT read and set dirty bit latched	3F8
MATRO	MAT read and set reference bit latched	3F8
MATRSDO	MAT read and set dirty bit	3D8
MATRSRO	MAT read and set reference bit	3D8
MBO/1	Memory busy flip-flop	13K7
MBOA	Buffered memory busy lines	13N7
MB1A	Buffered memory busy lines	13N7
MB1B	Buffered memory busy lines	13N8
MB1C	Buffered memory busy lines	13N8
MCCO	Memory cycle complete line	9G2
MCIO	Memory cycle initiate line	16R5
MDS000:MDS310	Processor data bus lines	Sheet 2
MEO/1	Memory error flip-flop	15L2
MEA000:MEA030	Memory expansion address lines	9G1,4
MERO	Memory error detect line	5N2
MER1	Memory error detect line	5N6
MRDSO	Memory read data strobe	9G6
MREO	Memory read enable control line	9G1
MREFO	Memory refresh line	9G5
MWA001	Memory word address line	9G3
MWA011	Memory word address line	9G5
MWEO	Memory write enable control line	9G3
MX01:31	Memory extension address lines	3H2
NCEO	Noncorrectable error line	7R4
NCLR1	Normal clear line	14R4
NEO/1	No error flip-flop	15N2
NPMO	Nonpresent memory line	14R4
NVAL1	Valid RAM data output	12N3
NVMO	Memory voltage failure signal	9L9
ODD1	Output data disable	16N3
P000:P060	Parity/syndrome bits	Sheets 4,5
PFSDO/1	P5 shutdown lines	9R4
PRFWO/1	Processor read fullword line	14H5
PSBYO	Processor store byte line	14D2
PSEL1	Processor select line	3A6
PSEL1A	Buffered processor select line	3C6
PSFWO	Processor store fullword line	14D4
PSHWO	Processor store halfword line	14D3
QWEO	Quadword enable line	16S7
QWMO/1	Quadword mode lines	16S8
RCARO	Ripple carry line	10E4
RCLCO/1	STM refresh clear lines	9N5
RCLRO	Internal refresh clear line	13H4
RCTO/1	Refresh clear time select lines	13L4

MNEMONIC	MEANING	SCHEMATIC LOCATION
RD011	ROM data line	3D8
RD021	ROM data line	3D8
RD031	ROM data line	3D8
RDS0/1	Buffered memory read data strobe lines	9M6
RE0/1	Read enable flip-flop	15K3
REF0/1	Refresh mode control lines	13L3
REL1	Read error logger line	14H5
RELA1	Read error logger RAM chip select enable	10E9
REQ1	Cycle steal request flip-flop	13D2
RFA0:RFA7	Refresh address bus	13N5,13K5
RFCTLD0	Refresh counter load	13N6
RFQ1	Refresh queue flip-flop	15L7
RFW1	Read fullword control line	14G6
ROAST1	Read and/or set control line	14H6
RSEL0	Refresh cycle steal select line	13G2
RST0/1	Read and set control lines	14H2
RSTDCD1	Read and set decode	14D1
RURE1	Data bus control line	14M7
S000:S060	Syndrome bit lines	10C7,10C8, 10C9
SBY1	Store byte control line	14H2
SCLK0A	Buffered processor shift clock	10C4
SCLK1	Processor shift clock	9L8
SCLK1A	Buffered processor shift clock	9N8
SCLR0	Systems clear relay contact	13C3
SCLR0B	Buffered systems clear line	13G3
SCLR0C	Buffered systems clear line	13E3
SCLR1B	Buffered systems clear line	13D3
SFW0/1	Store fullword lines	14H4
SHIFT1	Shift register advance line	10G3
SHW1	Store halfword line	14H4
SPW0/1	Store partial word line	14H2,14G1
STB0/1	Standby mode flip-flop	13H2
TA001:TA201	TA timer outputs	Sheet 16
TB001:TB161	TB timer outputs	Sheet 16
TEL0/1	Test error logger control lines	14H2
UCE0/1	Uncorrectable error flip-flop	7R4
UDD0/1	Uncorrectable data disable flip-flop	15L4
UFP1	P5U pullup	13F1
UP000:UP060	Uncorrected parity bit lines	9H8
VAL0/1	Valid bit data input	12H1
WA000/1	Word address counter bits	3M6
WA010/1	Word address counter bits	3M6
WC0	Word counter carry	3M9

MNEMONIC	MEANING	SCHEMATIC LOCATION
WCC0/1	Word counter carry	3M7
WDEN0	Write data enable line	14M9
WE0/1	Write enable lines	15E3
WRT0	Write contrcl line	3A6
WRT0A	Buffered write control line	3C6
WRT1	Buffered write control line	14A3
XRP1	P5 pullup	15N3
XRP2	P5 pullup	14K3
XRP3	P5 pullup	3M8

APPENDIX A
HARDWARE DOCUMENTATION GENERAL DESCRIPTION

1. INTRODUCTION

The hardware documentation system establishes the guidelines for:

- Number notation
- Part, drawing, and publication identification
- Component reference designation
- Connector pin numbering
- Drawing system

Hexadecimal numbering and equipment identification systems are also explained.

Component reference designations are determined by the logic board layouts. Assigned reference designations are used throughout the text and drawings when referring to components.

All logic boards have one or more header connectors to connect the board to the chassis backpanel. The boards may have one or more front edge cable connectors, allowing the boards to be interconnected. The pin numbering scheme explains the pin callouts for all connectors used.

The drawing system defines the standard format of all drawings. It specifies how net and registers are named and how ICs, flip-flops, and clocked devices are represented. Schematic drawing conventions are described.

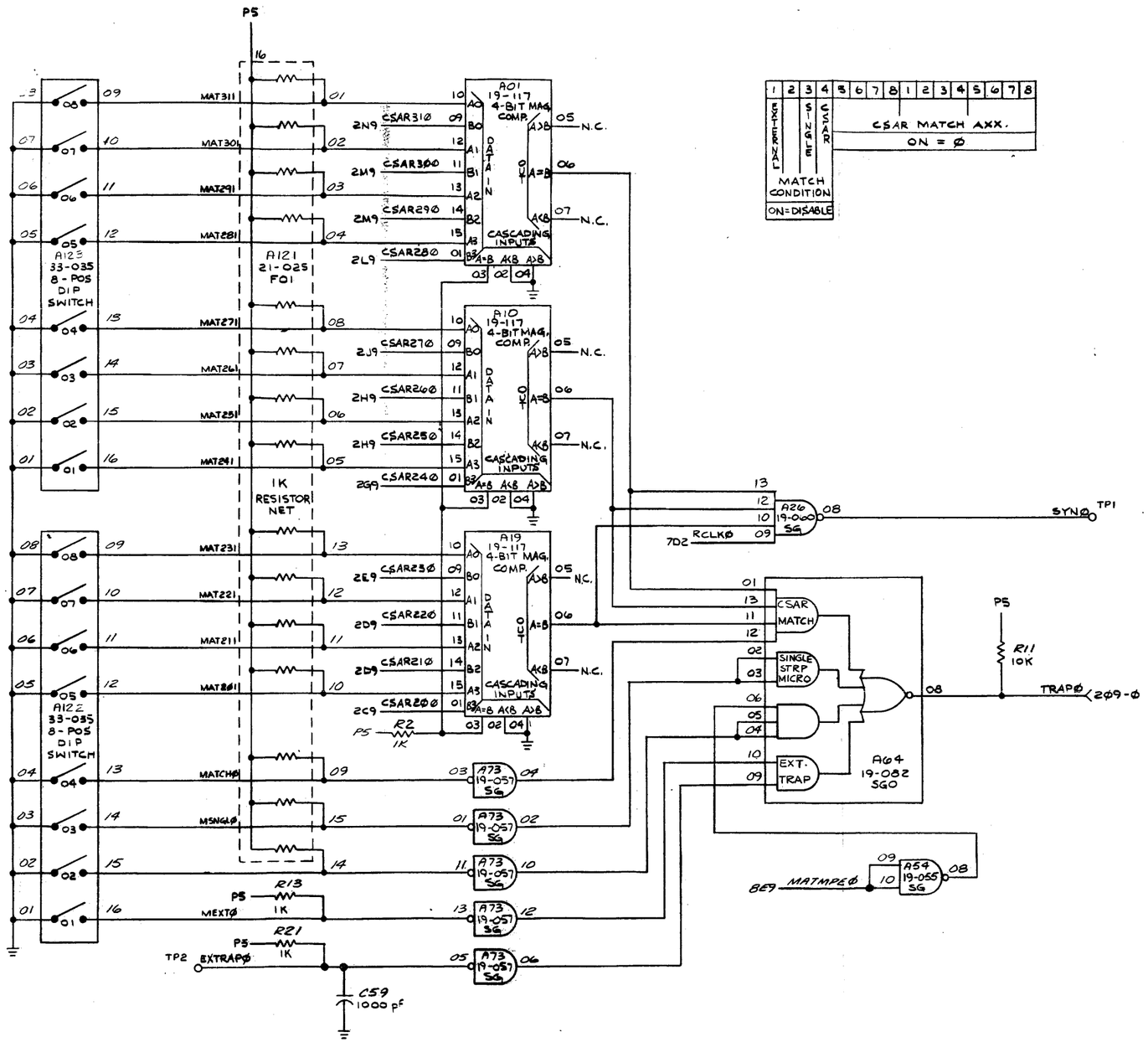
2. SCOPE

This appendix enables the digital technician to understand the documentation system. It describes number notation, the part numbering system, and the drawing system, as well as detailed illustrations.

Also included is a cross reference list of Perkin-Elmer Computer Systems Division part numbers and standard industry part numbers for the ICs and transistors found in the equipment.

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
EXT. TRAP		SINGLE STRP	CSAR	CSAR MATCH AXX.											
MATCH CONDITION				ON = 0											
ON=DISABLE															

SCALE –	NAME	TITLE	DATE
TOLERANCE		DRAFT	
		CHK	
		ENGR	

TITLE CPU-A TEST AID

TASK NO. 03179 SHEET OF
DWG NO. 35-816 D08 10 — 10

3. NUMBER NOTATION

Hexadecimal notation is the most common form of number notation used in Perkin-Elmer Computer Systems Division documentation. A single hexadecimal digit represents a group of four binary bits. Table A-1 lists the hexadecimal characters used.

Hexadecimal numbers are preceded by the letter X and the number is enclosed in single quotation marks. Examples of hexadecimal numbers are: X'1234', X'2EC6', X'A340', X'EEFA', and X'10B9'.

TABLE A-1 HEXADECIMAL CHARACTERS

1884

BINARY	DECIMAL	HEXADECIMAL	BINARY	DECIMAL	HEXADECIMAL	BINARY	DECIMAL	HEXADECIMAL
0000	0	0	0110	6	6	1100	12	C
0001	1	1	0111	7	7	1101	13	D
0010	2	2	1000	8	8	1110	14	E
0011	3	3	1001	9	9	1111	15	F
0100	4	4	1010	10	A			
0101	5	5	1011	11	B			

4. PART NUMBERING SYSTEM

Perkin-Elmer Computer Systems Division parts, drawings, and publications use a common numbering system. The part number and drawing numbers for drawings which describe the part are related. Figure A-1 shows the part number format. The following paragraphs describe the different fields.

0002

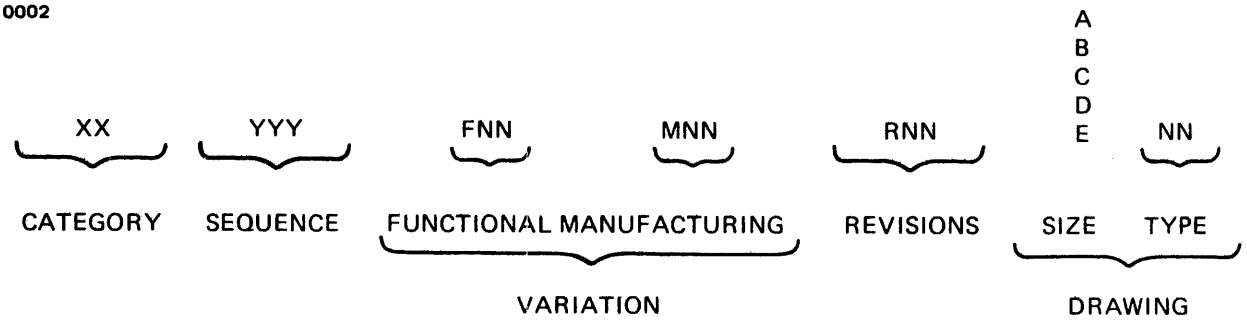


Figure A-1 Part Number Format

4.1 Category Field

The two-digit category number indicates the broad class or category to which a part belongs. Examples of category number assignments are:

01 - basic hardware systems
02 - basic hardware expansions
03 - basic software systems
04 - software packages
05 - microprograms
06 - test programs
07 - subroutines of general utility
10 - spare parts packages
12 - card file assemblies
13 - panels
17 - wire and cables
19 - integrated circuits
20 - transistors
27 - peripheral equipment
29 - manuals
34 - power supplies
35 - assembled printed circuit boards
36 - electro-mechanical devices

4.2 Sequence Field

The sequence number identifies a particular item within the category. Sequence numbers are assigned serially and have no other significance.

4.3 Functional Variation Field

The optical functional variation field consists of the letter F followed by two digits. The F field distinguishes between parts which are not necessarily electrically or mechanically equivalent, but which the same set of drawings describes. For example, a power supply may be internally strapped to operate on either 110 VAC or 220 VAC. With the exception of this strap, all power supplies of this type are identical. A note on the assembly and test specification drawings describes the strapping option.

4.4 Manufacturing Variation Field

The optional manufacturing variation field consists of the letter M followed by two digits.

The M field distinguishes between parts which are electrically and mechanically equivalent (interchangeable), but which vary in manufacture method. For example, if leads are welded instead of soldered on an assembly, the M field changes.

An exception to the M field meaning exists for software related categories. When used in software, the M field number indicates the form in which a particular program is presented. If a program is a set of machine instructions, these instructions may be presented on punched cards, paper tape, or magnetic tape and can be in symbolic, relative, or absolute binary form. Thus, the same program is presented several ways.

The format for the M field and its meaning for software is:

Mxy

where x identifies the media selection (i.e., paper tape, magnetic tape, cassette, etc.) and y identifies object or source and the format.

x		y	
conceptual	0	1	object program standard format 32-bit processor
paper tape	1		
cassette	2	4	memory image
magnetic tape (800 bpi)	3	6	object program standard format 16-bit processor
cards	4	7	object nonstandard format
disk (2.5 Mb)	5	8	object established task
disk (10 Mb)	6	9	source program
magnetic tape (1600 bpi)	7		

These numbers refer to the physical program placed on an approved media for software. A paper tape object program, in standard format for a 16-bit processor, has an M16 identifier. A magnetic tape object program, in standard format for a 32-bit processor, has an M31 identifier.

The following M numbers also have special meaning:

00 conceptual object
91 32-bit object listing
92 programming specifications
95 program description
96 16-bit object listing
98 operating procedures
99 documentation and manuals

4.5 Revision Field

The optional revision field consists of the letter R followed by two digits.

The R field indicates electrical or mechanical changes to a part. It does not change the part's original character. The R field changes often reflect improvements. A part with a revision level higher than the one specified can be used; however, a part with a revision level lower than specified cannot be used.

NOTE

A part number must contain a category number and a sequence number. All other fields are optional.

4.6 Drawing Field

The optional drawing field consists of a letter from A to E followed by two digits. The letter indicates the size of the original drawing. Each letter's size is as follows:

A - 216 mm x 279 mm (8 1/2" x 11")
B - 279 mm x 432 mm (11" x 17")
C - 432 mm x 558 mm (17" x 22")
D - 558 mm x 864 mm (22" x 34")
E - 864 mm x 1118 mm (34" x 44")

The two digits indicate the drawing type:

01 - parts list
02 - machine details
03 - assembly details
05 - art details
06 - wire run list
08 - schematic
09 - test specification
10 - purchase specification
12 - information
13 - program listing
14 - abstracts
15 - program description
16 - operating instructions
17 - program design specifications
18 - flowcharts
19 - product specification
20 - installation specification
21 - maintenance specification
22 - programming specification
24 - application information
25 - functional specifications

Examples:

Some examples of the part numbering system follow. The numbers were arbitrarily selected, and in most cases, they are fictitious.

35-060	The sixtieth printed circuit board assigned a part number under this system.
35-060M01	A printed circuit board electrically and mechanically interchangeable with the 35-060, but differing in manufacture method.
35-060F01	A printed circuit board not electrically, but mechanically, interchangeable with the 35-060 and described by the same set of drawings.
35-060R01	A revised 35-060 printed circuit board which supersedes the 35-060.
35-060B01	The 279 mm x 432 mm (11" x 17") parts list for a 35-060.
35-060B08	The 279 mm x 432 mm (11" x 17") schematic for a 35-060.
06-072A13	A 216 mm x 279 mm (8 1/2" x 11") listing of the 06-072 test program.
06-072A12	A 216 mm x 279 mm (8 1/2" x 11") information drawing on the 06-072 test program. Probably a part of the program.
29-060	The sixtieth manual assigned a number under this system. This number is not referenced to the part number of equipment described in the manual.

5. DRAWING SYSTEM

This section describes the drawings provided with the equipment. Drawings provided with peripheral devices and other purchased items may vary from the system described in this section. A digital system may be divided into a collection of functionally independent circuits such as memory, processor, and I/O device controllers. These circuits could be saleable units in their own right; electrically, they are self-contained and perform their function with minimum dependence on other functional circuits in the system. Hence, a functional circuit is treated as a building block. Each schematic contains information including type and location of discrete Integrated Circuits (ICs), pin connections, all interconnections within the schematic, connector pin numbers, and connections to other boards. The schematics reflect all the logical operations performed by the circuits. Symbols used on schematics generally conform to MIL-STD-806B.

5.1 Logic Boards

Three logic boards are used in the equipment: half, regular, and oversize. All logic boards contain one or more header connectors to connect the logic board to the chassis backpanel. The boards may contain front edge cable connectors, as required, allowing boards to be interconnected. Component locations on the logic boards are determined by the board layout.

Four standard chassis house the logic boards. The chassis are either 178 mm (7") or 356 mm (14") high and are classified by the number and type of boards they hold.

The chassis and the logic boards they can accommodate are given in Table A-2.

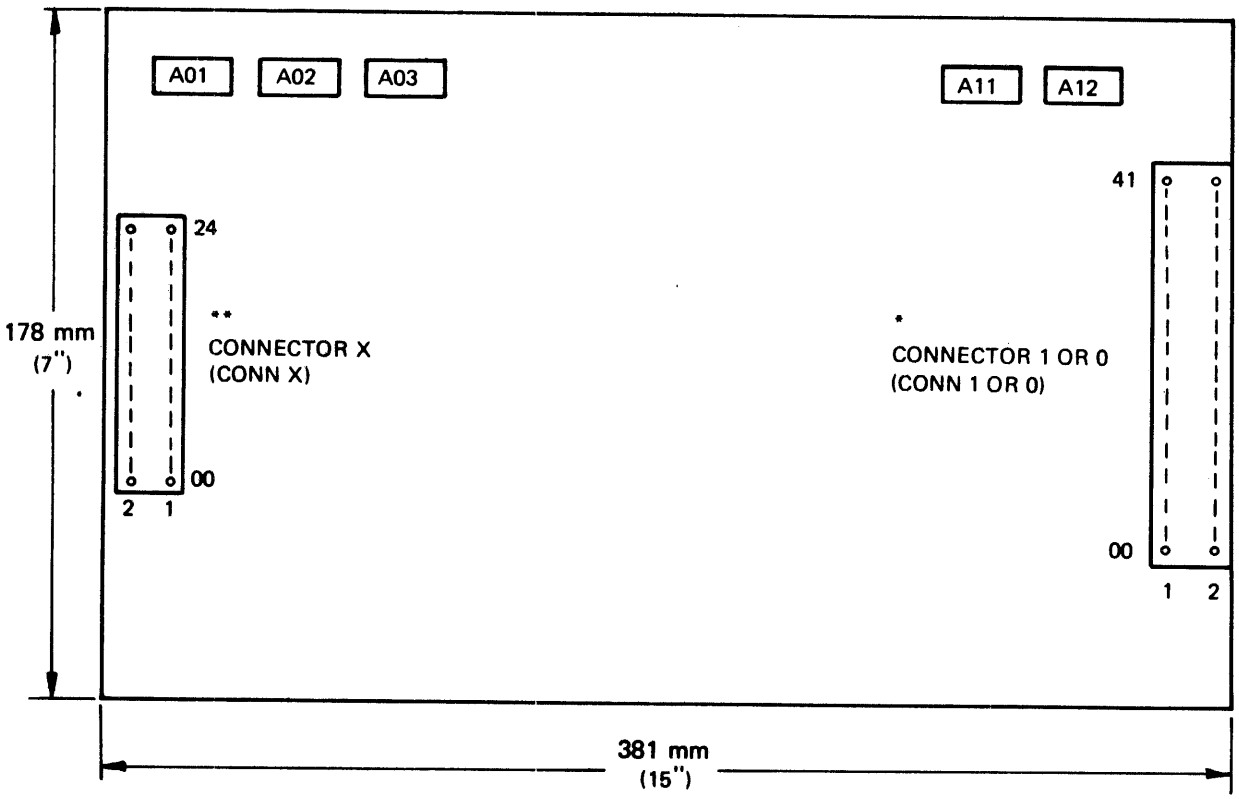
TABLE A-2 CHASSIS/BOARD CONFIGURATIONS

CHASSIS	BOARD MAXIMUM NUMBER AND TYPE
356 mm (14 inch) 16 slot	5 Oversize, 11 Regular

5.1.1 Half-Board Logic Layout

Figure A-2 illustrates a half-board 178 mm (7") logic board layout. Half-boards measure 178 mm x 381 mm (7" x 15") and can be placed in either the right or left half chassis position as required.

With the single header connector 1 or 0 (CONN 1 or CONN 0), components are numbered from left to right, starting in the upper left corner. If a front edge cable connector is required, it is located and numbered as shown in Figure A-2.



*The 178 mm (7") half-board is installed, with an adapter, in either the 1 or 0 side of a chassis slot. The backpanel connector and pins are referenced by the board location, 1 or 0.

**The front edge connector number (X) depends upon the board location in the slot as shown below:

BOARD BACKPANEL CONNECTION	FRONT EDGE CONNECTOR
0	2
1	3

Figure A-2 Half-Board Layout

Two 178 mm (7") half-boards can be inserted into a designated chassis slot via the 16-398 Half-Board Adapter Kit. (See Figure A-3.) Depending on requirements, the half-board adapter kit can strap two active 178 mm (7") boards or one active board and one blank 178 mm (7") board. Wiring does not take place between the boards and the adapter. Due to the adapter's design, the connectors on the board plug directly into the chassis slot backpanel connector.

665

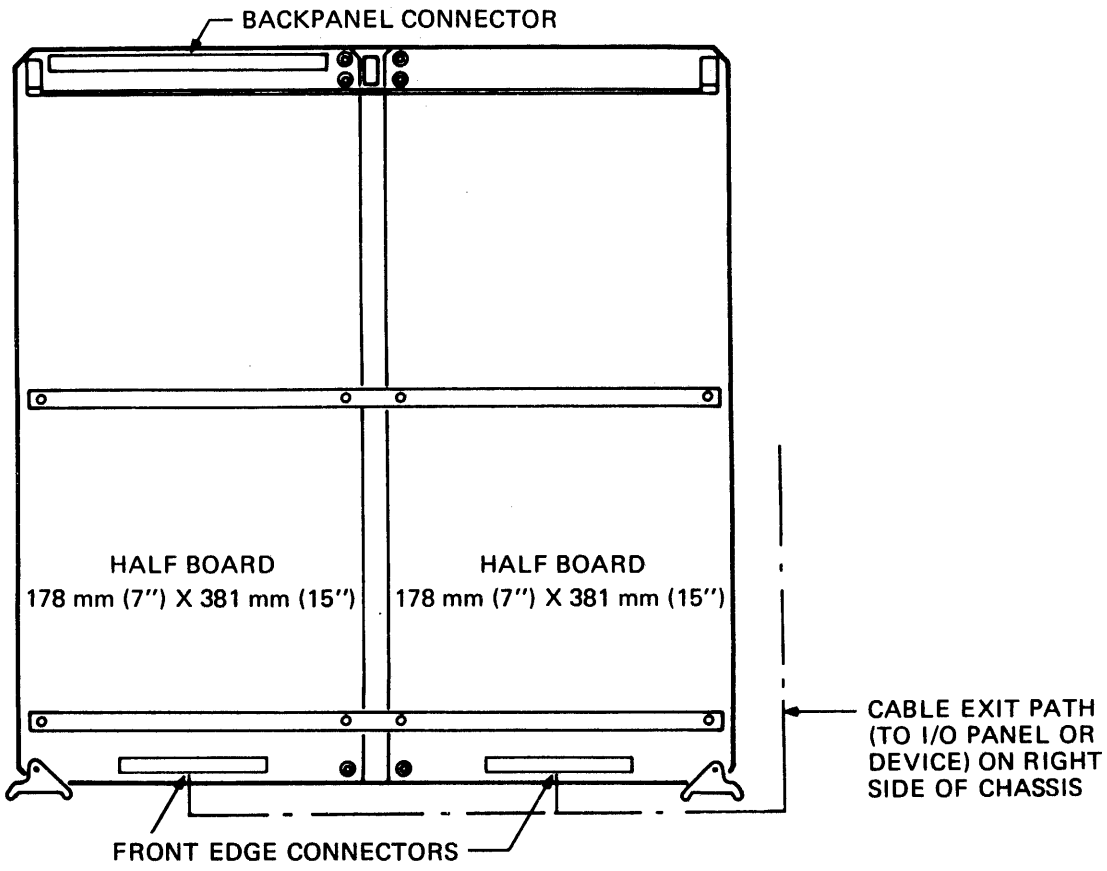


Figure A-3 16-398 Half-Board Adapter

5.1.2 Regular Logic Board Layout

Figure A-4 illustrates a regular logic board layout. Regular logic boards measure 381 mm x 381 mm (15" x 15") with header connectors (CONN 0 and CONN 1) located on the right. The first IC in the upper corner is 01 and the first capacitor is C1. Optional front edge cable connectors (CONN 2 and CONN 3) are located as shown in Figure A-4.

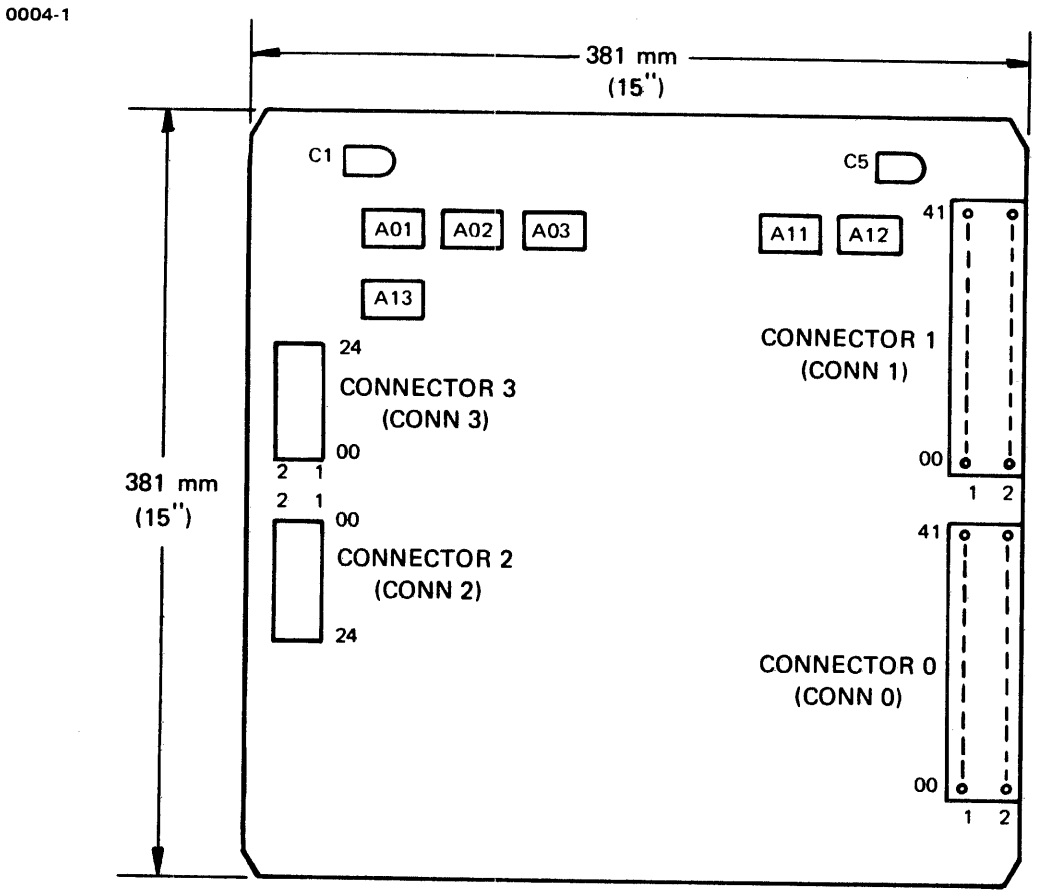
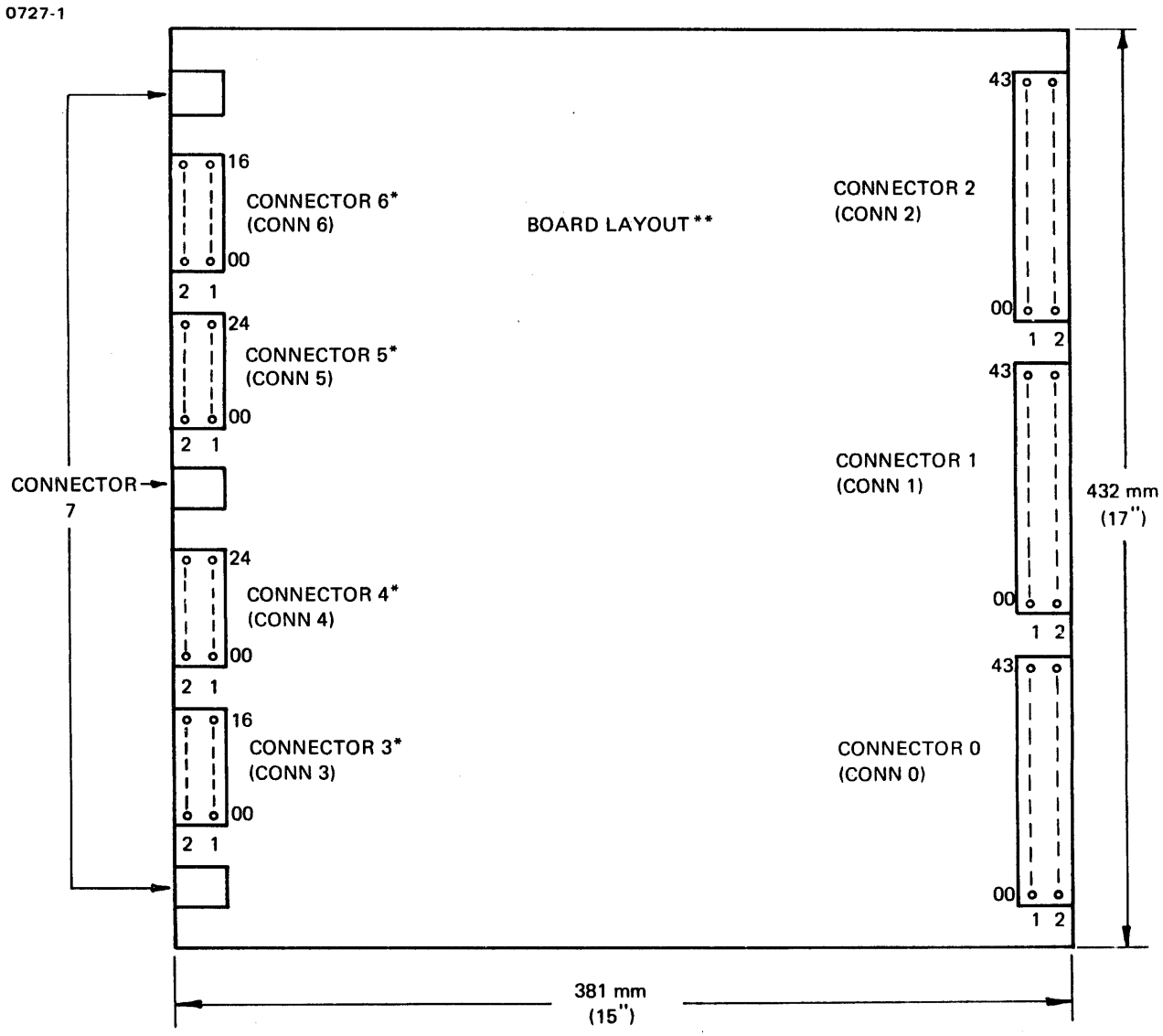


Figure A-4 Regular Logic Board Layout

5.1.3 Oversize Logic Board Layout

Figure A-5 illustrates an oversize logic board layout. Oversize logic boards measure 381 mm x 432 mm (15" x 17"). The boards have three header connectors (CONN 0, 1, and 2). Five front edge connectors (CONN 3, 4, 5, 6, and 7) are located as shown in Figure A-5. For individual board layouts, refer to the related installation manual.



*FRONT EDGE CONNECTORS AS REQUIRED.
**REFER TO APPLICABLE INSTALLATION MANUAL FOR INDIVIDUAL BOARD LAYOUT.

Figure A-5 Oversize Logic Board Layout

5.2 Connector Pin Numbers

Connector pin numbers are identified by a 4-digit number in the format rpp-c,

where:

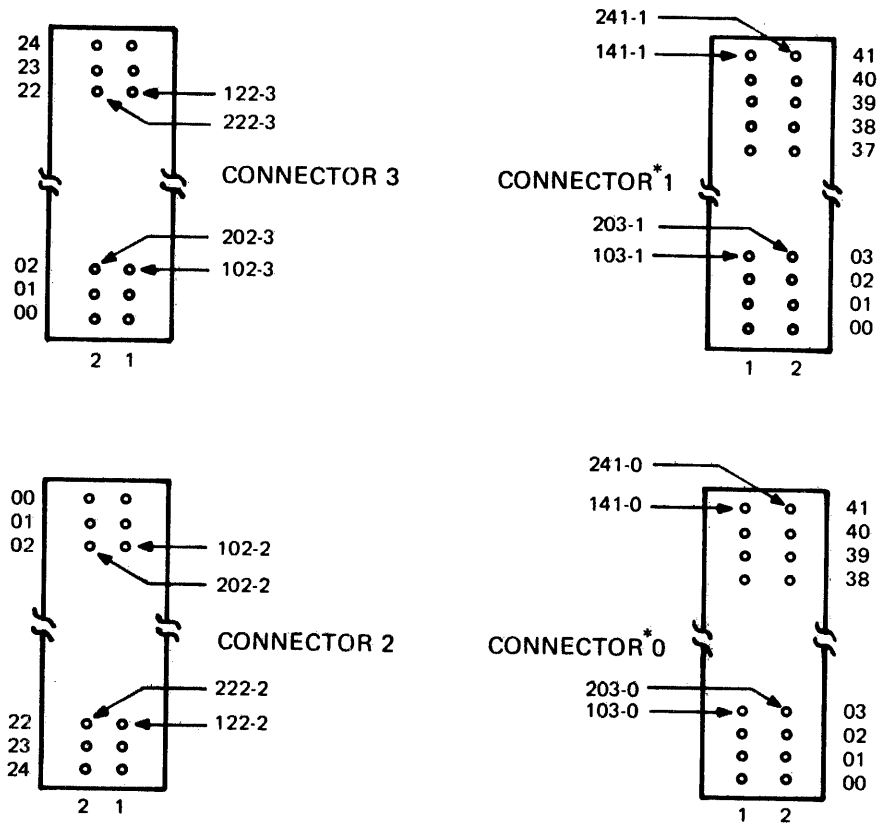
r is the row number
pp is the 2-digit pin number
c is the connector number

For example, connector pin number 103-1 refers to the fourth pin (03) in row 1 of connector 1. (See Figure A-6.)

5.2.1 Regular and Half-Boards

Figure A-6 shows the header and front edge cable connector's pin numbering scheme for regular and half boards. Header connectors have two rows of pins, and 42 positions. Front edge cable connectors have two rows of pins, but the pins may vary in the number of positions.

0006-1



*THE HALF BOARD IS INSTALLED WITH AN ADAPTER, IN EITHER THE 1 OR 0 SIDE OF A CHASSIS SLOT. THE BACKPANEL CONNECTOR AND PINS ARE REFERENCED BY THE BOARD LOCATION, 1 OR 0.

Figure A-6 Regular and Half-Board Connector Pin Numbering

5.2.2 Oversize Boards

Figure A-7 shows the header and front edge cable connector's pin numbering scheme for oversize boards. Header connectors (CONN 0, 1, and 2) have two rows of pins and 44 positions. Front edge cable connectors (CONN 3, 4, 5, and 6) have two rows of pins, but the pins may vary in number. Connector 7 is located in three positions, as indicated.

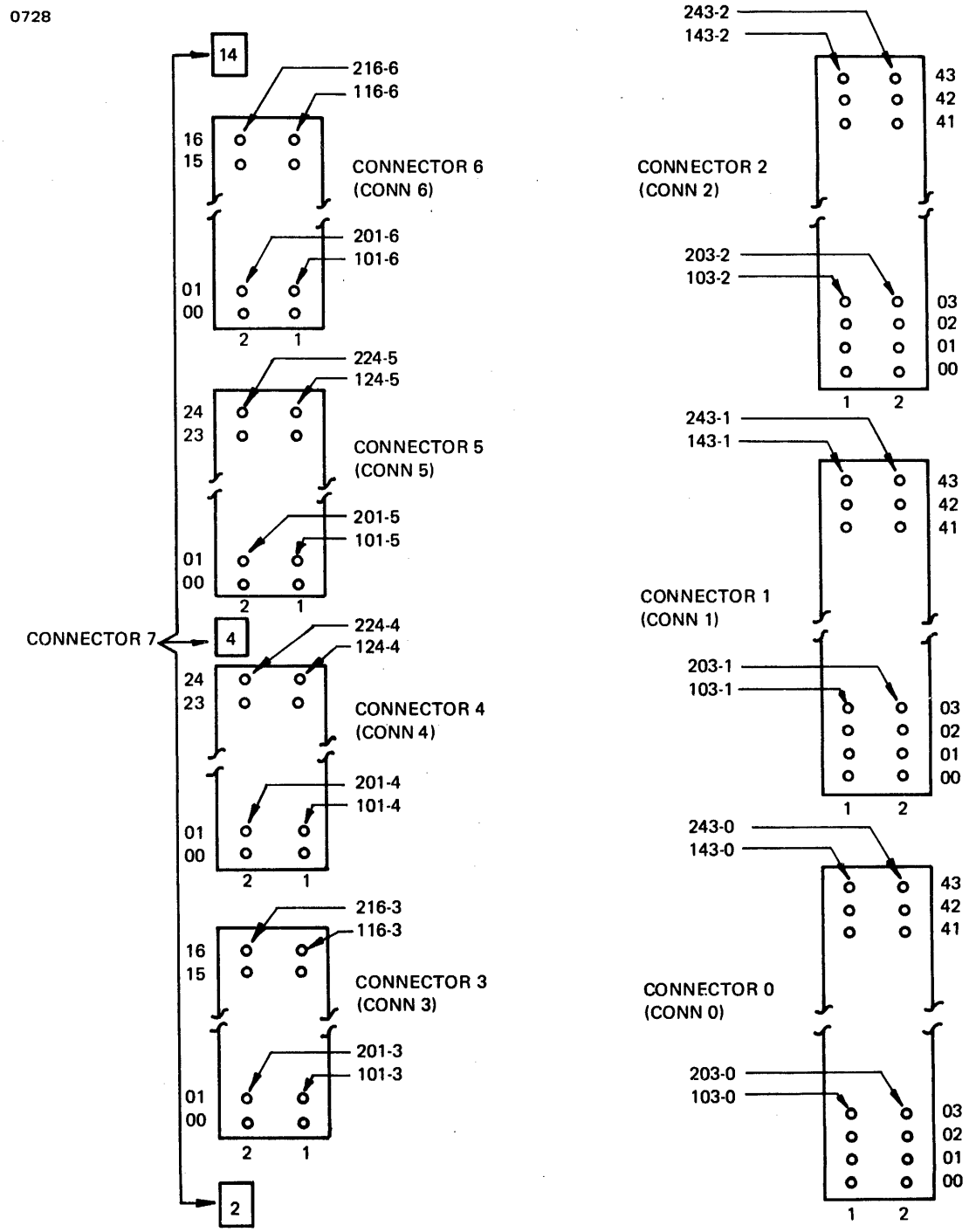


Figure A-7 Oversize Board Connector Pin Numbering

5.3 Register Naming System

The following rules are used to name registers:

1. Mnemonic names are restricted to six descriptors and a state indicator.

2. Each bit in the register is numbered, usually starting at 00 on the left, or most significant positions, and continuing to N-1 on the right. N is the number of bits in the register.

3. The 00 bit is the Most Significant Bit (MSB) and N-1 is the Least Significant Bit (LSB).

5.4 IC Representation

The ICs mounted directly on the logic board are represented on the schematic drawing by logic symbols. Each symbol contains the reference designation, device part number (category and sequence), and symbol mnemonic designation. (See Figure A-8.)

0003

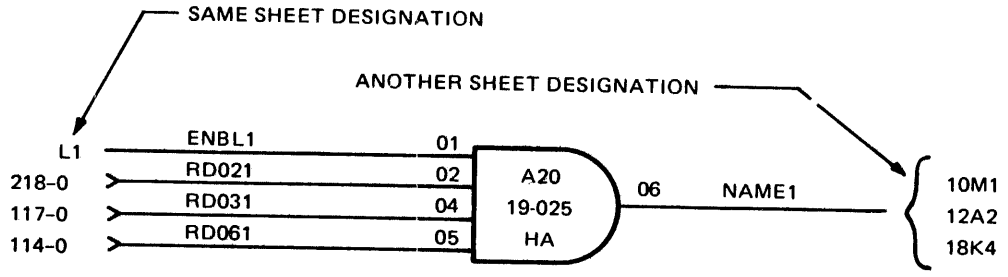


Figure A-8 High Speed AND Gate

The designations, numbers, and references shown in Figure A-8 are:

A20 Shows the component location on the logic board. (Refer to Section 5.1.)

19-025 The number 19 is the category number of ICs and the 025 is the sequence number of the component.

HA — Designates that this component is a high speed AND gate. Other common designators are:

- P - power gate
- SDF - Schottky, D flip-flop
- SG - Schottky gate
- SGO - Schottky high speed gate, open collector
- SBO - Schottky high speed buffer, open collector
- B - Buffer
- SB - Schottky high speed buffer
- LOR - Low power Schcttky OR
- LN - Low power Schottky NOR
- SOR - Schottky OR
- SN - Schottky NOR
- SA - Schottky AND
- SF - Schottky J/F flip-flop

L1 — This input lead is from area L1 on the same schematic sheet.

10M1, 12A2, 18K4 — Designate outputs to other logic schematic sheets.

218-0, 117-0, 114-0 — Designate inputs from connector 0.

Pin numbers 01, 02, 04, 05, and 06 correspond directly to the actual IC pin numbers.

5.5 Flip-Flops

When possible, the immediate cutput from a flip-flop (1 or 0 side) has a mnemonic name preceded by an F. Usually, a flip-flop named PSEL (Processor Selected) has an output mnemonic on the 0 side of FPSEL0. (Refer to Figure A-9.) Thus, when observing a mnemonic at the terminal end of a net, the digital technician has an indication that the signal is the output from a flip-flop rather than a decoded function.

0005

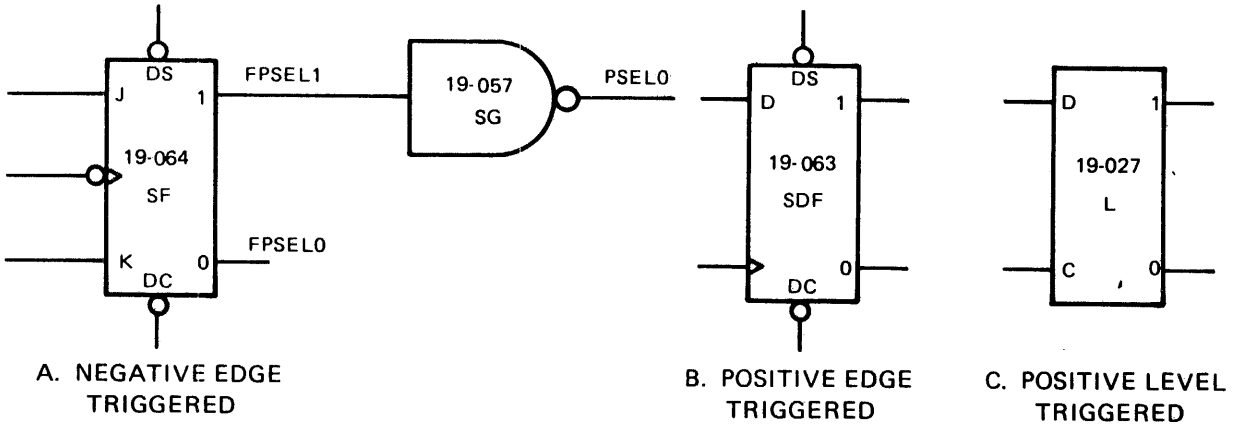


Figure A-9 Clocked Devices

5.6 Clocked Devices

Clocked devices, flip-flops, and counters in particular, are drawn to indicate information concerning their inputs. An input, having a circle adjacent to the pin designation, implies that a low active signal is needed to perform the specified operations. The symbol > at the clock input shows that the device changes state on an edge. If no circle is present, the chip is positive edge triggered. (Refer to Figure A-9.)

5.7 Nets

A net is an electrical connection between two or more points in a circuit. Ordinarily, a net has an originating end, usually a collector where the signal is generated, and one or more terminating ends. It is often convenient to assign descriptive mnemonic names to nets to identify them on schematics. Whether or not a net is named is arbitrary; however, a net is always assigned a name if:

1. The net is contained on one drawing sheet; but it is not a complete solid line on that sheet.
2. Part of the net appears on more than one sheet.
3. Part of the net connects with a different schematic.
4. Part of the net leaves a logic board.

If a net is named, the following rules apply:

1. Except in special cases, mnemonic names are a maximum of six characters plus a state indicator.

2. No other characters are permitted.

3. Where possible, mnemonics are descriptive; however, descriptive names are not always possible and the danger of misinterpreting a mnemonic exists.

4. A mnemonic name can be assigned to only one net.

5. A state indicator suffixes every mnemonic. This indicator consists of the digit 1, for the logically true state, or the digit 0, for the logically false state. For example, the set side of a flip-flop normally has 1 state indicator; the reset side normally has the 0 state indicator. The state indicator for a function changes each time that function is inverted. Thus, the state indicator permits assigning the same mnemonic to functions that are identical except for an inversion. Logic 0=.5 VDC or less, logic 1=2.4 VDC or more.

6. When a logical function is inverted, an inversion indicator is added after the state indicator allowing for functionally equivalent, but electrically different nets to have the same mnemonic name. Assume a signal NAME1 may be inverted to produce NAME0. If NAME0 is then inverted, NAME1A is produced. NAME1 and NAME1A are functionally equivalent, but physically different nets.

If a net fans out to many sheets of a schematic or to sheets on different schematics, it is assigned a mnemonic name and zoned from sheet to sheet. This zoning allows for proper identification of the originating and terminating ends of the net. The originating end of a net is the driver where a signal is generated. Terminating ends are all other points to which the net connects. When a lead leaves a sheet at the originating end, it is zoned by first indicating the sheet on which the net reappears. Assume that the gate shown in Figure A-8 is on schematic Sheet 20. The output NAME1 appears on Sheet 10, 12, and 18 of the schematic. The schematic number is implied. When a net enters a sheet from another sheet, it is labeled with the same mnemonic name and is only zoned back to the originating end of the net. In Figure A-8, the ENBL1 may have many other terminations in addition to the one shown. When a net leaves the sheet where it originates, it is generally zoned to every other sheet where the net terminates; the terminating end is zoned only to the originating sheet. On schematics, signals are coordinated between sheets only when the sheets are related to the same board. When a signal leaves a board, the backpanel map must be used.

When a lead leaves a logic board, it usually leaves through a logic board backpanel connector pin. Even if the complete net is on one drawing sheet, these connector pins must be shown on the schematic. Since the logic board location number, either in the logic symbol or the footnote, implies the connector number itself, only the connector pin number must be indicated under the pin symbol. In Figure A-8, RD061 enters the logic board on pin 114 of header connector 0.

5.8 Schematics

Figure A-10 is a schematic sheet with call-outs of the described conventions. The schematic drawings for a basic digital system are located in the rear of the appropriate digital system maintenance manual. Schematic drawings for other expansions are included with the expansion or with the publications which describe the expansion.

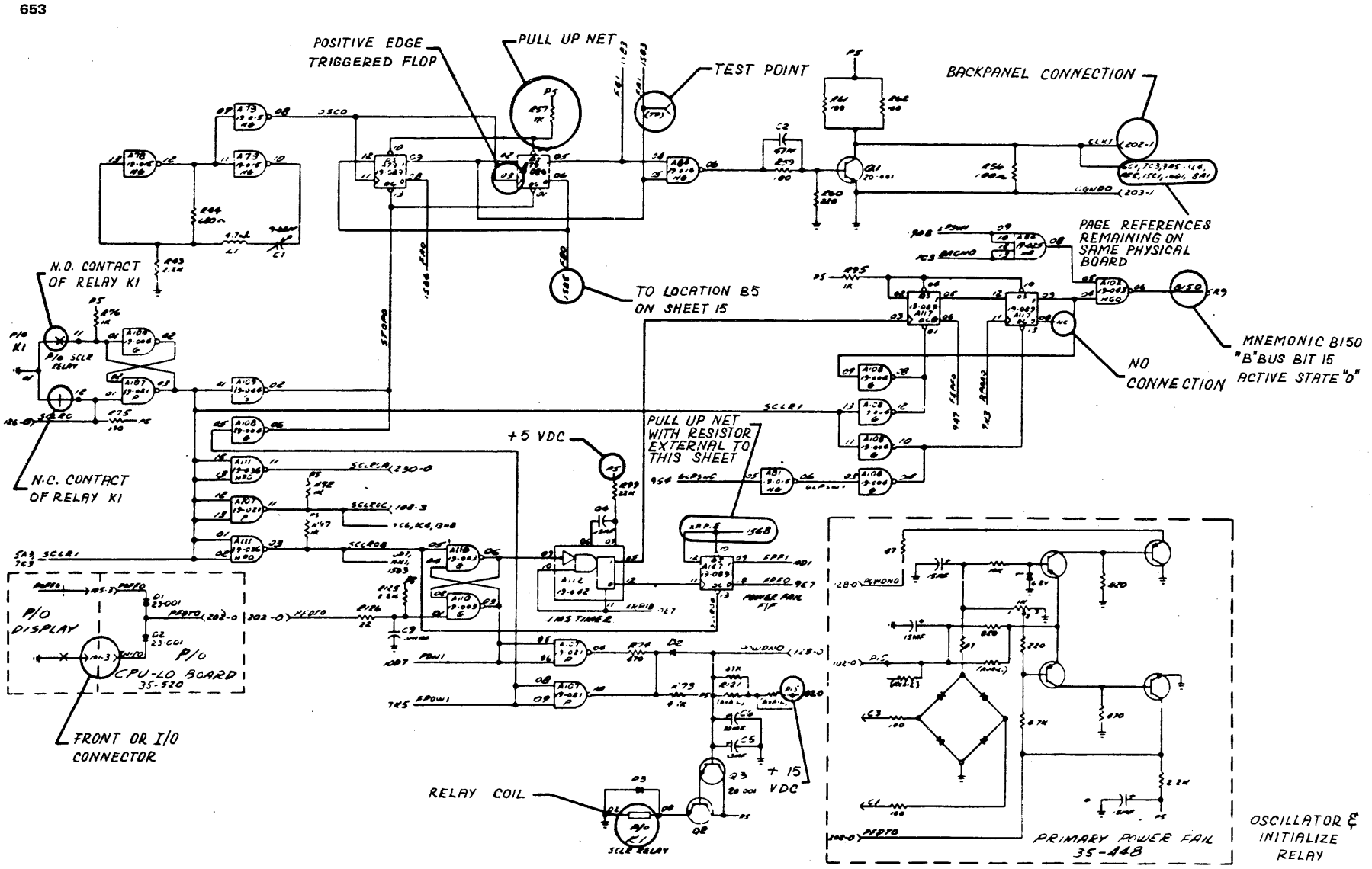


Figure A-10 Functional Schematic Format Drawing

6. PART NUMBER CROSS REFERENCE LIST

PART NO.	TYPE	VENDOR/JEDEC NUMBER
19-001	Dual 4 Input NAND DTL	861*
19-002	Triple 3 Input NAND DTL	863
19-003	Quad 2 Input NAND DTL	849
19-004	Hex 1 Input NAND DTL	837
19-005	Dual Power Gate DTL	844*
19-006	Dual Buffer DTL	832*
19-007	Flip-Flop DTL	848*
19-008	Gate Expander Dual 4 Input DTL	833*
19-009	8 Bit Stack DTL	930*
19-010	Differential Comparator LIN	710C
19-012	Dual 4 Input NAND Buffer TTL	74H40
19-013	Quad 2 Input NAND DTL	946
19-014	Dual J-K FLip-Flop DTL	855*
19-015	Hex Inverter 1 Input	74H04
19-016	Quad 2 Input NAND TTL	74H00
19-017	Triple 3 Input NAND TTL	74H10
19-018	Dual 4 Input NAND TTL	74H20
19-019	Single 8 Input NAND TTL	9007*
19-020	Operational Amplifier LIN	1709*
19-021	Quad 2 Input Power DTL	1644*
19-022	Dual J-K Flip-Flop TTL	3061*
19-023	Selected Dual Buffer 19-006 with 20-30 nanosecond delay DTL	932*
19-024	Triple 3 Input AND TTL	74H11
19-025	Dual 4 Input AND TTL	74H21
19-026	2-2-2-3 Input AND/OR TTL	74H52
19-027	4 Bit Adder TTL	7475
19-028	4 Bit Serial Adder TTL	7483
19-029	Quad Exclusive - OR TTL	7486
19-030	4 Bit Shift Register TTL	7495
19-031	One Shot TTL	74121
19-032	1 of 10 Decoder Open Collector	74145
19-033	Dual Sense Amplifier LIN	7524
19-034	Retriggerable One Shot TTL	74122
19-035	4 Bit Up/Down Counter TTL	74193
19-036	Quad 2 Input Open Collector TTL	7438
19-037	High Performance Operational Amp	748393
19-038	Dual 4 line to 1 line Mux TTL	74153
19-039	4 Bit ALU TTL	74181
19-040	4 Stage Look Ahead Carry TTL	74182
19-041	4 x 4 Register Stack TTL	74170
19-042	Dual Retriggerable One Shot TTL	74123
19-043	Quad 2 Input NAND Open Collector	74H01
19-044	Hexadecimal Inverter Open Collector TTL	74H05

*Obsolete

PART NC.	TYPE	VENDOR/JEDEC NUMBER
19-045	Dual J-K Flip-Flop TTL	74H106*
19-046	Quad RS-232C Line Driver	ML1488
19-047	Quad RS-232C Line Receiver	MC1489A
19-048	8 Bit Shifter 24 Pin DIP	74198
19-049	1024 Bit PROM TTL	DM8587
19-050	8 Input NAND TTL	74H30
19-051	1024 Bit PROM TTL	74187
19-052	Dual 4 Input Buffer	832*
19-053	4 2-line-to-1-line Data Sel. Mux	74157/9322
19-054	Quad 2 Input NAND STTL	7400
19-055	Quad 2 Input NAND STTL	74S00
19-056	Quad 2 Input NAND Open Collector STTL	74S03
19-057	Hex 1 Input Inverter STTL	74S04
19-058	Triple 3 Input NAND STTL	74S10
19-059	Triple 3 Input AND STTL	74S11
19-060	Dual 4 Input NAND STTL	74S20
19-061	Dual 4 Input Buffer STTL	74S40
19-062	2-2-3-4 Input AND/OR Inverter STTL	74S64
19-063	Dual D Edge Triggered Flip-Flop STTL	74S74
19-064	Dual J-K Flip-Flop STTL	74S112
19-065	Quad 2:1 Mux Non-Inverting STTL	74S157
19-066	Quad 2:1 Mux Inverting STTL	74S158
19-067	4 Bit ALU STTL	74S181
19-068	4 Stage Carry Look Ahead Carry STTL	74S182
19-069	8 line to 1 line Mux STTL	74151
19-070	4 Bit Synchronous Counter TTL	74161
19-071	Quad D Edge Triggered Flip-Flop	74175
19-072	4 Bit Left/Right Shift Register TTL	74194
19-073	Dual 4:1 Mux Tri-State TTL	8214(NAT)
19-074	8 Bit Priority Encoder TTL	9318(F)
19-075	16 x 4 Register Stack TTL	3101(INT)
19-076	1024 Bit Memory MOS	TM54062
19-077	256 Bit Memory TTL	6531(MON)
19-078	Dual 4 Input NAND Open Collector	74S22
19-079	Comparator Dual	NE5211
19-080	1024 Bit PROM TTL	82S29(SIG)
19-081	Univ. Asynchronous Receiver/ Transmitters	TR1042A
19-082	2-2-3-4 Input AND/OR Invert Open Collector STTL	74S65

* Obsolete

PART NO.	TYPE	VENDOR/JEDEC NUMBER
19-083	9 Bit Parity Generator/Checker STTL	82S62(SIG)
19-085	Timer	MC1555
19-086	741 C DIP Operational Amplifier	741
19-087	747 DIP Operaticnal Amplifier	747
19-088	733 C DIP Operational Amplifier	733
19-089	Dual D Edge Triggered Flip-Flop	74H74
19-090	High Speed (710) Differential Comparator DIP	710
19-091	Retriggerable Single One Shot	9600
19-092	Negative Voltage Regulator	1463
19-093	Positive Voltage Regulator	1469
19-094	Positive Voltage Regulator	723
19-095	Linear Positive Voltage Regulator	805
19-096	First In-First Out Serial Memory 64 Word 4 Bit	3341
19-097	Amplifier	LH0002* (RES)
19-098	Quad 2:1 Multiplexor Non-Inverting	74157
19-099	Dual Sense Amplifier Inverting	75234
19-100	Dual Driver 8 Pin DIP	75452
19-101	Quad-2 Input Positive NAND Buffer	7437
19-102	6-1 Input Buffer/Buffer Open Collector	7407
19-103	1 of 10 Decoder	7442
19-104	Current Switch Memory Driver	75325
19-105	Dual Differential Driver	75114/ 9614
19-106	Dual Differential Receiver	75115/ 9615
19-107	Dual Sense Amplifier	7520
19-108	Quad 2 Input NAND	7400
19-109	Hex Inverter Buffer Driver Open Collector	7406
19-110	Hex Inverter	7404
19-111	Dual 4 Input NAND Buffer	7440
19-112	Optically Coupled Isolator	4N25
19-113	360 Dual Line Driver	75123
19-114	360 Triple Line Receiver	75124
19-115	Quad 2 Input AND TTL	74H08
19-116	Dual 4:1 Multiplexor STTL	74S153
19-117	4 Bit Magnitude Comparator STTL	74S85
19-118	Quad Bus Transceiver TTL	26S12A
19-119	Expandable AND/OR Invert TTL	74H55
19-120	Dual Timer	NE556
19-121	Matched Pair 19-085 (P.S. Timing)	MC1555

* Obsclete

PART NO.	TYPE	VENDOR/JEDEC NUMBER
19-122	1024 Bit PROM TTL	SEE 19-051
19-123	Dual Voltage Controlled Oscillator	74S124
19-124	4-2 Input NAND Buffer STTL	74S37
19-125	4-2 Input NAND Buffer STTL	74S38
19-126	Dual 2 Wide 2 Input AND/OR Inverter STTL	74S51
19-127	4-2 Input Exclusive OR STTL	74S86
19-128	13 Input NAND, 3-State STTL	74S134
19-129	3 to 8 Line Decoder STTL	74S138
19-130	2-4 Input NAND 50 Ohm Line Driver STTL	74S140
19-131	4D FF STTL	74S175
19-132	4 2/1 Mux STTL	74S258
19-133	4 Bit Binary Full Adder TTL	74283
19-134	Hexadecimal Buffer/Inverter TTL	8T98
19-135	4 Bit Binary Counter STTL	(98S16)
19-136	1 of 10 Decoder HS & HV	74145
19-137	Dual Peripheral Positive OR Driver 8 Pin DIP	75453(SIG)
19-138	Character General	2513
19-139	Driver/Decoder	7447AN
19-140	8 Bit Latch	9334PCQM
19-141	Multi-Port Register	9338PCQM
19-142	1024 Bit PROM TTL	SEE 19-080
19-143	4K x 1 NMOS RAM	9050
19-144	4-Hysteresis Rec	8T380
19-145	Voltage Regulator +15 500 Milli-amperes	78M15AUC
19-145F01	Voltage Regulator +12 500 Milli-amperes	78M12AUC
19-145F02	Voltage Regulator -15 500 Milli-amperes	LM340T-15
19-146F00	Voltage Regulator -15 500 Milli-amperes	79M15/ LM320T-15
19-146F01	Voltage Regulator -12 500 Milli-amperes	79M12/ LM320T-15
19-146F02	Voltage Regulator -2 500 Milli-amperes	79M05
19-146F03	Voltage Regulator -5 500 Milli-amperes	7905/ LM320T-5
19-147F01	8 Channel Analog Mux	H11-181A-5
19-147F02	8 Channel Analog Mux	Analog Devices A07503JN

PART NO.	TYPE	VENDOR/JEDEC NUMBER
19-148	Voltage Follower	LM310D
19-149	High Speed Op Amp	HA2-2525-5
19-150	2 Channel Analog Switch	DG1828A/ IH5048 CTW
19-151	Low Level Inst Amp	AD521JD
19-152	Linear Amp	BB3660J
19-153	4-2 Input NAND LPTTL	74LS00
19-154	Hex Inverter LPTTL	74LS04
19-155	3-3 Input NAND LPTTL	74LS10
19-156	2-4 Input NAND LPTTL	74LS20
19-157	8 Input NAND LPTTL	74LS30
19-158	4-2 Input NOR LPTTL	74LS02
19-159	4-2 Input OR LPTTL	74LS32
19-160	4-2 Input AND LPTTL	74LS08
19-161	3-3 Input AND LPTTL	74LS11
19-162	2-4 Input AND LPTTL	74LS21
19-163	4-2 Input NAND Schmitt Trigger LPTTL	74LS132
19-164	4-2 Input NAND Buffer LPTTL	74LS37A
19-165	2-D FF LPTTL	74LS74
19-166	2-JK FF LPTTL	74LS112
19-167	4-D FF LPTTL	74LS175
19-168	3 to 8 Decoder Demux LPTTL	74LS138
19-169	Hex Inverter Open Collector LPTTL	74LS05
19-170	4-2 Input NAND Open Collector LPTTL	74LS03
19-171	Dual Multivibrator	74LS123
19-172	4-2 Input Exclusive OR LPTTL	74LS86
19-173	8 to 1 AND/OR Invert Mux LPTTL	74LS151
19-174	4-2 Input AND/OR Mux LPTTL	74LS257
19-175	4-2 Input AND/OR Mux LPTTL	74LS157
19-176	4-2 Input Mux LPTTL	74LS258
19-177	4-1 Input AND/OR Mux LPTTL	74LS153
19-178	3-3-2-2 Wide AND/OR Inverter LPTTL	74LS51A
19-179	4-3-3-2 AND/OR Inverter LPTTL	74LS54
19-180	4 Bit Counter LPTTL	74LS161
19-181	4 Bit Up/Down Counter LPTTL	74LS193
19-182	4 Bit Left/Right Shift Register TTL	74LS194
19-183	2-Line Driver	75110
19-184	4 Bit Micro Controller	AMD2901
19-185	4K-Bit ROM	N82S115
19-186	4K-Bit PROM	82S215N
19-187	Quad 2:1 Mux with Storage LPTTL	74LS298
19-188	RCM Chip Programmed In House 16 Bit LSU	
19-189	ROM Chip Programmed In House 32 Bit LSU	

PART NO.	TYPE	VENDOR/JEDEC NUMBER
19-190	Quad Comparator	LM339
19-191	Quad 2-Input NOR Gate	CD4001AE
19-192	Dual D Flip Flop	CD4013AE
19-193	1024 Bit PROM TTL	SEE 19-051
19-194	2K PROM TTL	N82S131
19-195	2K PROM TTL	SEE 19-051
19-196	Quad 2 Input 3 State Mux. Non Inverting	74S257
19-197	1024 B Dynamic RAM (NMOS)	MK4096N-16
19-198	Field Programmable Logic Array	82S00
19-200	16 x 4 First In-First Out (FIFO)	9430
19-201	6800 Micro-Processor	MC6800
19-202	Peripheral Interface Adapter (PIA)	MC6820
19-203	Sync Serial Data Adapter (SSDA)	MC6852
19-204	1K RAM	MCM6810A
19-205	2 Phase Clock	MC6870A
19-206	4 Input 3 State Line Transceiver	8T26/ 8T26A
19-207	Error Checking, Polynomial Gen.	MC8506P
19-208	Dual VCO	MC4024P
19-209	Phase Frequency Detection	MC4044
19-210	Micro-Processor	2608-1/ MCM6830P
19-214	Asynchronous Communication Interface Adapter	MC6850
19-215	Differential Line Driver	AM26LS31
19-216	Differential Line Receiver	AM26LS33
19-217	Tri-state Line Driver/Receiver	74S214A
19-218	1024 x 1 Bi-Polar RAM	82S181A
19-219		82S181A
19-220	1024 x 8 PROM	MK4116P-2
19-221	16,384 x 1 MOS RAM	MC3423U
19-222	Over-Voltage Protector	74S280
19-223	9 Bit Even/Odd Parity Generator/ Checker	74LS377
19-224	Octal Flip-Flop	74LS244
19-225	Line Driver/Receiver	3242
19-226	Refresh Counter	74LS174
19-227	Hex Flip-Flop	MK4027-2
19-228	4096 x 1 MOS RAM	8T97
19-229	Tri-state Hex Buffer	74S350
19-230	Shift	MC2918
19-231	D Register	74S373
19-232	8 Bit Latch	74S374
19-233	Octal Flip-Flop	74S02
19-234	Quad 2 Input NOR Gate	74S32
19-235	Quad 2 Input OR Gate	74S08
19-236	Quad 2 Input AND Gate	AD581JH
19-238	10 Volt Precision Reference	
19-239	Baud Rate Generator	

PART NO.	TYPE	VENDOR/JEDEC NUMBER
19-240	Octal Bus Driver	74S241
19-241	Dual 5 Input NOR Gate	74S260
19-242	Optically Coupled Isolator	MCT273
19-243		
19-244	ROM	702,703 (Centronics)
19-245		
19-246	Reg Pulse Width Modulator	SG3524
19-247	3 Term Reg 1 Amp	SG78XXCK UA78XXKC
19-248	3 Term Reg 1 Amp	UA78L12, UA78C12ACDB, LM78L12AHC
19-249	Digital Delay Module	212XX(Pulse), DL-18XX(Valor)
19-250	Dual Mono Multivibrator	74221, SN74221
19-251	Hex Invert/Hysteresis	SN7414
19-252	1KX1 RAM (MOS)	2125AL, 93L425XC
19-253	2KX8 Bipolar PROM	3636-1, 76161-5
19-254	256 x 9 RAM	93479XC, N82S212
19-255		
19-256	Xtal Clock Osc.	XO-33C20 (Dale), 7401-308, 20MHZ (Spectrum)
19-258	P NAND Gate/Invert	SN74S133
19-259	2-4 Decoder/Demux	SN74S139
19-260	2-4 Decoder/Demux	SN74LS139
19-261	8-3 Encoder	SN74LS148
19-262	Octal Buffer/3 State Output	SN74LS240
19-263	Octal D Type Flip-Flop	SN74LS374
19-264	256 x 4 RAM	93422
19-265	256 x 4 RAM	93L422
19-266	4 x 4 Register File	SN74LS170
19-267	Optically Coupled Isolator	TIL102
19-268	4096 Bit High Speed RAM	52147 (Amer,Micro)
20-001	Transistor NPN High Speed Switch	2N3646
20-002	Transistor PNP 500 MA	MPS6534
20-003	Transistor	DT5-423/ 2N3902
20-004	Transistor NPN	2N5189/ 64493
20-005	Transistor	2N3056

PART NO.	TYPE	VENDOR/JEDEC NUMBER
20-006	Transistor NPN 15 Amps 100W T03 Case	2N3055
20-007	Transistor NPN 3 Amps	TIP31A
20-008	Transistor PNP 3 Amps	TIP32A
20-009	Transistor Triac 2 Amps 100V	A03001
20-010	Transistor NPN 500 MA Code Driver	2N5845/ 2N5845/ 74659A
20-011	Transistor Photo	2N5777
20-012	Transistor PNP High Current Switch	2N2907/ TS3413
20-013	Transistor NPN	2N3302
20-014	Transistor NPN	2N4238
20-015	Transistor PNP	2N4235
20-016	Transistor PNP	2N3740
20-017	Transistor NPN	2N3766
20-018	Transistor, Power Silicon NPN	2N3054
20-019	Transistor	2N6038
20-020	Transistor Switching 1 Amp T05 can	2N3725
20-021	Transistor NPN Silicon	MPS3646
20-022	Transistor NPN	2N1711
20-023	Transistor PNP	2N905A/ J2N2905A
20-024	Transistor Switch	2N3776
20-025	PNP High Speed Switch	2N3467
20-026	Transistor Module, Quad	FSQ1079/ FPQ3724
20-027	Transistor	2N2369
20-029	Transistor	
20-030	Transistor	HPX002
20-031	Transistor	2N3568
20-032	Transistor NPN	SEE 2N6486 SPEC
20-033	Transistor	KE4393
20-034	Transistor	2N3904
20-035	Transistor	2N3906
20-036	Transistor	MP54356
20-037	Transistor	D45H2
20-038	Transistor	2N2520
20-039	Transistor	2N222A
20-043	MOS FET	
21-025F01	1K ohm-15 to Common DIP	898 1-1K ohm (Beckman)
21-025F02	470 ohm-15 to Common DIP	898-1-470 ohm (Beckman)
21-025F03	330 ohm-15 to Common DIP	898-1-330 ohm (Beckman)

PART NO.	TYPE	VENDOR/JEDEC NUMBER
23-001	Diode High Speed-High Current	1N4150
23-002	Diode 5.1 V Zener	1N4733A
23-003	Diode 10V Zener	1N4750A
23-004	Diode 6.1 V Zener	1N4735A
23-007	Diode Mot Bridge	MDA962-2
23-008	Diode Int. Rectifier	40HF-5R
23-009	Diode	1N4735
23-010	Diode Int. Rectifier	S1Y1P
23-011	Diode Rectifier	2N681
23-012	Diode Thermistor	1D2032
23-013	Diode 9.3V	1N2163
23-014	Diode	1N3880
23-015	Diode	1N3889
23-016	Diode Bridge Rectifier	YS448
23-017	Diode	1N2070
23-018	Diode 18 V Zener	1N4746
23-019	Diode	1N3615
23-020	Diode 8.2V Zener	1N756A
23-021	Diode 9.1 V Zener	1N757A
23-022	Diode 3.3V Zener	1N746A
23-023	Diode Bridge Rectifier	KDH250
23-024	Diode, Power Fast Rec. 30 Amps	1N3909
23-025	Diode, Power Fast Rec. 3 Amps	MR841/ A115A
23-026	Triac 600V 30 Amps	2N6162
23-027	Diac 32V	1N5761
23-028	Power SCR Thyristor	2N4441
23-029	Diode	1N4607
23-030	Diode	1N4156A
23-031	Diode 6.8 V Zener	1N4736A
23-032	Diode 9.1 V Zener	1N4739
23-033	16 Diode Array	45190 (Litton)
23-034R01	Switch Diode 600 MA	TSC1N4607
23-035	Diode 40A	MBA4030
23-036	Diode	MPD-400
23-037	Zener Diode 2.4V	1N4370
23-041F00	Low Voltage Zener Diode	LVA51A40114/ LVA51A22819
23-041F02	Low Voltage Zener Diode	LVA62A40098/ LVA62A22941/ LVA62A40212
23-042	Power Schottky	SD41
23-043F00	Zener Diode Avalanche 5.1V	
23-043F01	Zener Diode Avalanche 5.6V	
23-043F02	Zener Diode Avalanche 6.2V	
23-060	Bridge Rectifier, 600V,50A	
30-013	4.7uH Inductor	
30-013F02	1.5uH Inductor	
30-013F03	2.2uH Inductor	

PART NO.	TYPE	VENDOR/JEDEC NUMBER
30-018	100 nanoseconds Delay Line 10 taps	30-018 (Princeton Advanced Eng.)
30-019	50 nanoseconds Delay Line 10 taps	30-018 (Princeton Advanced Eng.)
33-032	Hexadecimal Switch	BERG or AMP

PROG= *NONE* ASSEMBLED BY CAL/32 03-338R00-00

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                0000 0001                1  LSU      EQU   1                                                    LSU00000
                0000 0000                2  TEST     EQU   0                                                    LSU00010
                                         3  *                                                                  LSU00020
000000:I                                 4           IFZ   LSU                                                  LSU00030
                                         5           PROC  PERKIN-ELMER 32-BIT LOAD-STORE UNIT (LSU) LOADER     LSU00040
                                         6           ELSE                                                       LSU00050
                                         7           PROG  PERKIN-ELMER SERIES 3200 LSU LOADER, 03-235M91R00-00 LSU00060
                                         8           ENDC                                                       LSU00070
                                         9  *                                                                  LSU00080
                                        10           ERSOZ                                                      LSU00090
                                        11           NORX3                                                      LSU00100
                                        12           SQUEZ                                                      LSU00110
                                        13           CROSS                                                      LSU00120
                                        14           FREZE                                                      LSU00130
                                        15           TARGT 32                                                   LSU00140
                                        15+          TARGT 32
                                        16  *                                                                  LSU00150
                                        17  * THIS PROGRAM IS DESIGNED TO RUN ON THE PERKIN-ELMER SERIES       LSU00160
                                        18  * 3200 ONLY.  IT USES INSTRUCTIONS NOT AVAILABLE ON THE           LSU00170
                                        19  * PERKIN-ELMER 7/32 OR 8/32.                                       LSU00180
                                        20  *                                                                  LSU00190
                                        21  * USING CONDITIONAL ASSEMBLY INSTRUCTIONS THIS SOURCE             LSU00200
                                        22  * WILL PRODUCE EITHER OF THE FOLLOWING PROGRAMS:                   LSU00210
                                        23  *                                                                  LSU00220
                                        24  *   SETTING                          PROGRAM                       LSU00230
                                        25  *                                                                  LSU00240
                                        26  *     LSU                                                          LSU00250
                                        27  *                                                                  LSU00260
                                        28  *      1  ..................STANDARD LSU LOADER - FOR CHIPS.       LSU00270
                                        29  *      0  ..................BOOTSTRAP LOADER (TAPE) - FOR TESTING. LSU00280
                                        30  *                                                                  LSU00290
                                        31  * IF THE LSU OPTION IS SPECIFIED THIS PROGRAM PRODUCES THE FORMAT  LSU00300
                                        32  * REQUIRED FOR LSU STORAGE AND OPERATION (SEE PROGRAMMING          LSU00310
                                        33  * SPECIFICATION 02-267R02A22 SECTION 5)                           LSU00320
                                        34  *                                                                  LSU00330
                                        35  * NOTE:  IF 'TEST' IS SET TO A NON-ZERO VALUE, THE PROGRAM(S)      LSU00340
                                        36  *        GENERATED WILL RUN ON A 7/32 OR 8/32.                     LSU00350
                                        37  *                                                                  LSU00360
                                        38  * THIS PROGRAM IS A LOADER THAT READS A CORE IMAGE OF OS/32        LSU00370
                                        39  * FROM A 5, 67, OR 256 MEGABYTE DISC, FROM A FLOPPY DISC,          LSU00380
                                        40  * OR FROM A MAGNETIC TAPE.                                        LSU00390
                                        41  *                                                                  LSU00400
                                        42  *    DEVICE CODES          DEVICE                                  LSU00410
                                        43  *                                                                  LSU00420
                                        44  *        X'32'               5MB DISC - FIXED                      LSU00430
                                        45  *        X'33'               5MB DISC - REMOVABLE                  LSU00440
                                        46  *        X'35'              67MB DISC                              LSU00450
                                        47  *        X'36'             256MB DISC                              LSU00460
                                        48  *        X'37'            FLOPPY DISC                              LSU00470
                                        49  *        X'40'             800 BPI MAG TAPE                        LSU00480
                                        50  *        X'41'            1600 BPI OR DUAL DENSITY MAG TAPE        LSU00490
                                        51  *                                                                  LSU00500
                                        52  * THE LOADER FUNCTIONS IN THE FOLLOWING MANNER:                    LSU00510
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53  *                                                                      LSU00520
54  *       1. OUTPUT A "MENU" OF STANDARD DEVICES FROM WHICH THE O.S.     LSU00530
55  *          MAY BE LOADED.                                              LSU00540
56  *                                                                      LSU00550
57  *       2. IN RESPONSE TO USER'S INPUT, READ LOADER INFORMATION BLOCK  LSU00560
58  *          OF REQUESTED O.S. TO DETERMINE THE O.S. SIZE.               LSU00570
59  *                                                                      LSU00580
60  *       3. TEST THE MEMORY IN WHICH THE O.S. IS TO RESIDE.             LSU00590
61  *                                                                      LSU00600
62  *       4. RELOCATE THE LOADER ABOVE THE MEMORY TO BE OCCUPIED         LSU00610
63  *          BY THE O.S.                                                 LSU00620
64  *                                                                      LSU00630
65  *       5. TEST THE MEMORY JUST VACATED BY THE LOADER.                 LSU00640
66  *                                                                      LSU00650
67  *       6.  LOAD AND EXECUTE THE O.S.                                  LSU00660
68  *                                                                      LSU00670
69  * THE MEMORY TEST FUNCTIONS IN THE FOLLOWING MANNER:                   LSU00680
70  *                                                                      LSU00690
71  *       1. THE ADDRESS OF EACH LOCATION TO BE TESTED IS WRITTEN TO     LSU00700
72  *          THAT LOCATION.  AFTER ALL ADDRESSES ARE WRITTEN, THEY ARE   LSU00710
73  *          READ BACK AND COMPARED TO THE ADDRESS POINTER.              LSU00720
74  *                                                                      LSU00730
75  *       2. TEST 1 IS RUN USING THE COMPLEMENT OF EACH ADDRESS AS       LSU00740
76  *          THE TEST DATA.                                              LSU00750
77  *                                                                      LSU00760
78  *       3. A SERIES OF BIT PATTERNS ARE THEN TESTED IN THE             LSU00770
79  *          FOLLOWING MANNER:                                           LSU00780
80  *                                                                      LSU00790
81  *          A. A PATTERN IS WRITTEN TO EACH LOCATION TO BE TESTED.      LSU00800
82  *          B. AFTER ALL LOCATIONS HAVE BEEN WRITTEN TO WITH ONE        LSU00810
83  *             PATTERN, THE DATA IS READ BACK AND COMPARED TO THE       LSU00820
84  *             PATTERN BEING TESTED.                                    LSU00830
85  *          C. A AND B ARE REPEATED UNTIL ALL PATTERNS HAVE BEEN USED.  LSU00840
86  *                                                                      LSU00850
87  *       IF A NON-COMPARE OCCURS DURING ANY OF THE TESTS, THE           LSU00860
88  *       ERROR MESSAGE "MEMTST ERR NNNNNN" IS OUTPUT, AND TESTING       LSU00870
89  *       IS TERMINATED.  "NNNNNN" REPRESENTS THE ADDRESS AT WHICH       LSU00880
90  *       THE NON-COMPARE OCCURRED.                                      LSU00890
91  *                                                                      LSU00900
92  *       THE PATTERNS AND METHOD USED IN THIS TEST ASSURE THAT:         LSU00910
93  *                                                                      LSU00920
94  *       1. ALL LOCATIONS TESTED ARE INDEPENDENTLY ADDRESSABLE;         LSU00930
95  *                                                                      LSU00940
96  *       2. NO BITS WITHIN ANY FULLWORD ARE STUCK IN THE ON OR          LSU00950
97  *          OFF STATE;                                                  LSU00960
98  *                                                                      LSU00970
99  *       3. NO BITS WITHIN ANY FULLWORD ARE SHORTED TOGETHER;           LSU00980
100 *                                                                      LSU00990
101 *       4. ACCESSING ANY FULLWORD WILL NOT CHANGE ANY OTHER FULLWORD   LSU01000
102 *          WITHIN THE TESTED RANGE.                                    LSU01010
```

GENERAL EQUATES

```
                                 104  * ENTRY/EXTRN DECLARATIONS = NONE                                          LSU01030
                                 105  *                                                                         LSU01040
                                 106  *        COPY  DIR                                                        LSU01050
                                 107  *        COPY  LIB                                                        LSU01060
                                 108           NLSTM                    Turn off macro expansions.     *rod*    LSU01070
                                 109           $DIR                     .                              *rod*    LSU01080
                                 110           $LIB                     .                              *rod*    LSU01090
                                 111           LIST                                                             LSU01100
0000 1000                        112  LSUADDR  EQU   X'1000'            INITIAL BASE ADDRESS OF LOADER.          LSU01110
0000 0078                        113  BINDV    EQU   X'78'              BINARY DEVICE ADDRESS.                   LSU01120
0000 0060                        114  OS.START EQU   X'60'              O.S. START ADDRESS.                      LSU01130
0000 000D                        115  CR       EQU   X'0D'              CARRIAGE RETURN.                         LSU01140
0000 000A                        116  LF       EQU   X'0A'              LINE FEED.                               LSU01150
0000 0008                        117  BSY      EQU   8                                                          LSU01160
                                 118  *                                                                        LSU01170
                                 119  * REGISTER EQUATES                                                       LSU01180
                                 120  *                                                                        LSU01190
0000 0000                        121  R0       EQU   0                                                          LSU01200
0000 0001                        122  R1       EQU   1                                                          LSU01210
0000 0002                        123  R2       EQU   2                                                          LSU01220
0000 0003                        124  R3       EQU   3                                                          LSU01230
0000 0004                        125  R4       EQU   4                                                          LSU01240
0000 0005                        126  R5       EQU   5                                                          LSU01250
0000 0006                        127  R6       EQU   6                                                          LSU01260
0000 0007                        128  R7       EQU   7                                                          LSU01270
0000 0008                        129  R8       EQU   8                                                          LSU01280
0000 0009                        130  R9       EQU   9                                                          LSU01290
0000 000A                        131  R10      EQU   10                                                         LSU01300
0000 000B                        132  R11      EQU   11                                                         LSU01310
0000 000C                        133  R12      EQU   12                                                         LSU01320
0000 000D                        134  R13      EQU   13                                                         LSU01330
0000 000E                        135  R14      EQU   14                                                         LSU01340
0000 000F                        136  R15      EQU   15                                                         LSU01350
000000:I                         137           IFNZ  LSU                                                        LSU01360
```

LSU LOADER - PREAMBLE

```
000000:I  0000                  139           DCX   0                       START PSW                                    LSU01380
000002:I  1000                  140           DC    Z(LSUADDR)              START ADDRESS                                LSU01390
000004:I  1000                  141           DC    Z(LSUADDR)              LOAD ADDRESS                                 LSU01400
000006:I  17EC                  142           DC    Z(LSUADDR+LENGTH)       END ADDRESS                                  LSU01410
                                143           ELSE                                                                       LSU01420
                                144           TITLE BOOTSTRAP LOADER - ABSOLUTE PREAMBLE (X'80' TO X'CF')                LSU01430
                                145 ** NOTE:   THE INSTRUCTIONS OR DATA RESIDING AT LOCATIONS X'84'                        LSU01440
                                146 *          AND X'86' SHOULD ALWAYS HAVE FULLWORD VALUES.                               LSU01450
                                147 *          THESE LOCATIONS SERVE AS THE POWER FAIL CURRENT PSW SAVE                    LSU01460
                                148 *          POINTER, AND THE POWER FAIL REGISTER SAVE POINTER.                          LSU01470
                                149 *                                                                                      LSU01480
                                150 PREAMBLE BS    START                   START.                                       LSU01490
                                151 BKSPC    DC    X'9100'                 BACKSPACE COMMAND.                           LSU01500
                                152          DC    X'3000'                 POWER FAIL CURRENT PSW SAVE POINTER.         LSU01510
                                153          DC    X'3008'                 POWER FAIL REGISTER SAVE POINTER.            LSU01520
                                154 *                                                                                      LSU01530
                                155 START    EQU   *                                                                    LSU01540
                                156          LIS   R4,0                                                                 LSU01550
                                157          EPSR  R1,R4                                                                LSU01560
                                158          LI    R2,S1END                GET BUFFER ADDRESS.                          LSU01570
                                159          LB    R1,BINDV                GET ADDRESS OF BINARY DEVICE.                LSU01580
                                160          THI   R1,X'0004'              IS IT A PTRP OR TTYR?                        LSU01590
                                161          BZS   ST.READ                 YES, THEN DON'T BACKSPACE.                   LSU01600
                                162 MTNCHK   EQU   *                                                                    LSU01610
                                163          SSR   R1,R3                   IS MAG TAPE STOPPED YET?                     LSU01620
                                164          THI   R3,X'0010'              :                                            LSU01630
                                165          BZS   MTNCHK                  NO, THEN WAIT UNITL IT DOES.                 LSU01640
                                166          OC    R1,BKSPC                YES, THEN ISSUE THE BACKSPACE.               LSU01650
                                167 MTNCHK1  EQU   *                                                                    LSU01660
                                168          SSR   R1,R3                   AND WAIT UNTIL BACKSPACE COMPLETE.           LSU01670
                                169          THI   R3,X'0010'              :                                            LSU01680
                                170          BZS   MTNCHK1                 :                                            LSU01690
                                171          SHI   R4,80                   OFFSET FOR BACKSPACE.                        LSU01700
                                172 ST.READ  EQU   *                       START THE READ.                              LSU01710
                                173          LHI   R4,LSUADDR-S1END(R4) GET BUFFER END ADDRESS.                         LSU01720
                                174          OC    R1,BINDV+1              ISSUE THE READ COMMAND.                      LSU01730
                                175 READATA  EQU   *                                                                    LSU01740
                                176          SSR   R1,R3                   GET STATUS.                                  LSU01750
                                177          BTBS  BSY,READATA             LOOP UNITL NOT BUSY.                         LSU01760
                                178          RD    B1,0(R2,R4)             READ A BYTE.                                 LSU01770
                                179          AIS   R4,1                    ELSE, BUMP BUFFER POINTER,                   LSU01780
                                180          BNPS  READATA                 AND READ UNTIL COUNTED OUT.                  LSU01790
                                181          B     LSUADDR                 THEN, GO EXECUTE LOADER.                     LSU01800
                                182 *                                                                                      LSU01810
                                183          IFP   PREAMBLE-*+80                                                        LSU01820
                                184          DO    PREAMBLE-*+80                                                        LSU01830
                                185          DB    0                       FILL BYTE.                                   LSU01840
                                186          ENDC                                                                       LSU01850
                                187 S1END    EQU   LSUADDR+LENGTH                                                       LSU01860
                                188          ENDC                                                                       LSU01870
```

LSU LOADER / SEGMENT 2 (RELOCATABLE)

```
                0000 0008:I                 190  LODRSTRT EQU   *                                                    LSU01890
000008:I        C840 0010                   191           LHI   R4,X'10'          GET DEVICE # AND                   LSU01900
00000C:I        DE40 87A3 =0007B3:I         192           OC    R4,COM2           SET-UP PASLA.                      LSU01910
00000E:I        9B47                        193           RDR   R4,R7             ISSUE DUMMY READ.                  LSU01920
000012:I        E610 8500 =000516:I         194           LA    R1,MSG            GET ADDRESS OF MESSAGE HANDLER.    LSU01930
000016:I        2480                        195           LIS   R8,0              INITIALIZE STRING REGISTER.        LSU01940
000018:I        01F1                        196           BALR  R15,R1            OUTPUT THE IDENTIFIER.             LSU01950
00001A:I        06DC                        197           DC    Z(ID-LODRSTRT)    :                                  LSU01960
00001C:I        01F1                        198           BALR  R15,R1            OUTPUT THE MENU.                   LSU01970
00001E:I        06F4                        199           DC    Z(MENU-LODRSTRT)  :                                  LSU01980
                                            200  *                                GET THE REPLY.                     LSU01990
                0000 0020:I                 201  GETNAME  EQU   *                                                    LSU02000
000020:I        41E0 852C =000550:I         202           BAL   R14,GETC          LOOP UNTIL DELIMITER               LSU02010
*000024:I       2212      =000020:I         203           BNM   GETNAME           :                                  LSU02020
000026:I        E690 86DA =000704:I         204           LA    R9,DEVTABLE       NO, GET BASE ADDR OF DEVICE TABLE. LSU02030
00002A:I        E6A0 8716 =000744:I         205           LA    R10,DEVTBLND      GET END ADDRESS OF DEVICE TABLE.   LSU02040
                0000 002E:I                 206  CK.NAME  EQU   *                                                    LSU02050
00002E:I        5589 0000                   207           CL    R8,0(R9)          MATCH?                             LSU02060
*000032:I       2336      =00003E:I         208           BE    FOUND.NM          YES, THEN GO GET FILENAME.         LSU02070
000034:I        2698                        209           AIS   R9,8              NO, BUMP POINTER.                  LSU02080
000036:I        059A                        210           CLR   R9,R10            AT END YET?                        LSU02090
000038:I        2035      =00002E:I         211           BNES  CK.NAME           NO, TRY NEXT NAME.                 LSU02100
00003A:I        4300 FFCA =000008:I         212           B     LODRSTRT          YES, INVALID NAME - START AGAIN.   LSU02110
                                            213  *                                                                  LSU02120
                0000 003E:I                 214  FOUND.NM EQU   *                                                    LSU02130
00003E:I        08D9                        215           LR    R13,R9            HOLD ADDRESS OF SELECTION.         LSU02140
000040:I        E6AC 86C0 =000704:I         216           LA    R10,DEVTABLE      CALCULATE OFFSET.                  LSU02150
000044:I        0B9A                        217           SR    R9,R10            :                                  LSU02160
000046:I        2334      =00004E:I         218           BZS   VECTOR            IF ZERO, NO FURTHER CALCULATION.   LSU02170
000048:I        2480                        219           LIS   R8,0              ELSE, CALCULATE INDEX              LSU02180
00004A:I        2478                        220           LIS   R7,8              INTO VECTOR TABLE.                 LSU02190
00004C:I        1D87                        221           DR    R8,R7             (R9) = INDEX.                      LSU02200
                0000 004E:I                 222  VECTOR   EQU   *                                                    LSU02210
00004E:I        4090 89EA =000A3C:I         223           STH   R9,TBNTRY         SAVE AS INDEX INTO DEVICE TABLE.   LSU02220
000052:I        E6A0 86E6 =00073C:I         224           LA    R10,OTHER         WAS "OTHR" SELECTED?               LSU02230
000056:I        05DA                        225           CLR   R13,R10           :                                  LSU02240
000058:I        4230 606A =0000C6:I         226           BNE   SET.IO            NO, SET-UP TO READ O.S.            LSU02250
                                            227  *                                YES, ASK FOR SPECIFICS.            LSU02260
00005C:I        2490                        228           LIS   R9,0              INITIALIZE INDEX INTO DEVICE TABLE. LSU02270
00005E:I        24D0                        229           LIS   R13,0             INITIALIZE INDEX INTO ADDRESS TABLE. LSU02280
                0000 0060:I                 230  NXT.ITEM EQU   *                                                    LSU02290
000060:I        486D 8676 =0006DA:I         231           LH    R6,ADDRTABL(R13)  GET MESSAGE ADDRESS.               LSU02300
000064:I        4060 8002 =00006A:I         232           STH   R6,NAM.ITEM       :                                  LSU02310
000068:I        01F1                        233           BALR  R15,R1            ISSUE REQUEST.                     LSU02320
00006A:I        0062                        234  NAM.ITEM DC    Z(NAM.ITEM-LODRSTRT) :                             LSU02330
00006C:I        2400                        235           LIS   R0,0              INITIALIZE FOR HEX CHARACTERS.     LSU02340
                0000 006E:I                 236  GET.ITEM EQU   *                                                    LSU02350
00006E:I        2480                        237           LIS   R8,0              INITIALIZE STRING REGISTER.        LSU02360
000070:I        41E0 84DC =000550:I         238           BAL   R14,GETC          GET A CHARACTER.                   LSU02370
*000074:I       2116      =000080:I         239           BM    CHK.ITEM          EXIT IF CARRIAGE RETURN DETECTED.  LSU02380
000076:I        41E0 852C =0005A6:I         240           BAL   R14,X.CONV        ELSE, CONVERT TO HEX NIBBLE.       LSU02390
00007A:I        1104                        241           SLLS  R0,4              CONCATENATE WITH PREVIOUS RESULTS. LSU02400
00007C:I        0608                        242           OR    R0,R8             :                                  LSU02410
```

LSU LOADER / SEGMENT 2 (RELOCATABLE)

```
*00007E:I     2208      =00006E:I

              0000 0080:I
 000080:I     C5D0 0008
*000084:I     2132      =000088:I
 000086:I     1104
              0000 0088:I
 000088:I     4009 8646 =0006D2:I
 00008C:I     26D2
 00008E:I     C5D0 0004
 000092:I     4230 8026 =0000BC:I
 000096:I     2460
              0000 0098:I
*000098:I     C560 0038
 00009C:I     4380 FF68 =000008:I
 0000A0:I     4506 85F8 =00069C:I
*0000A4:I     2333      =0000AA:I
 0000A6:I     2668
*0000A8:I     2208      =000098:I

              0000 00AA:I
 0000AA:I     C500 0037
*0000AE:I     2187      =0000BC:I
 0000B0:I     26D2
 0000B2:I     2692
 0000B4:I     C500 0037
*0000B8:I     2132      =0000BC:I
 0000BA:I     26D2
*0000BC:I

              0000 00BC:I
 0000BC:I     2692
 0000BE:I     C590 0008
 0000C2:I     4280 FF9A =000060:I
*0000C6:I
```

```
243           B     GET.ITEM          GET NEXT CHARACTER.
244  *
245  CHK.ITEM EQU   *
246           CLHI  R13,8             WAS ITEM "DRV#"?
247           BNE   STR.ITEM          NO, THEN STORE AS IS.
248           SLLS  R0,4              YES, THEN SHIFT BY 4.
249  STR.ITEM EQU   *
250           STH   R0,OTHR(R9)       STORE ITEM IN DEVICE TABLE.
251           AIS   R13,2             BUMP ADDRESS TABLE POINTER.
252           CLHI  R13,4             WAS LAST ITEM "CODE"?
253           BNE   BMP.ITEM          NO, GO STORE ITEM NOW.
254           LIS   R6,0              YES, CHECK VALIDITY OF DEV CODE.
255  NXT.CODE EQU   *
256           CLI   R6,OTHR-DTABLE    AT END OF TABLE?
257           BNL   LODRSTRT          YES, ERROR - RESTART.
258           CLH   R0,DTABLE+2(R6)   VALID DEVICE CODE?
259           BE    END.CODE          YES, THEN EXIT.
260           AIS   R6,8              NO, BUMP POINTER.
261           B     NXT.CODE          CHECK NEXT CODE.
262  *
263  END.CODE EQU   *
264           CLHI  R0,X'37'          WAS CODE FOR "NORMAL" DISC?
265           BL    BMP.ITEM          YES, NOW GET CONTROLLER.
266           AIS   R13,2             NO, DON'T ASK FOR "CTLR".
267           AIS   R9,2              :
268           CLHI  R0,X'37'          WAS CODE FOR FLOPPY?
269           BNE   BMP.ITEM          NO, THEN ASK FOR "SLCH".
270           AIS   R13,2             YES, ASK FOR "DRV#".
271           B     BMP.ITEM          :
272  *
273  BMP.ITEM EQU   *
274           AIS   R9,2              BUMP INDEX.
275           CLHI  R9,8              ARE WE DONE YET?
276           BL    NXT.ITEM          NO, GET THE NEXT ITEM.
277           B     SET.IO            YES, SET-UP TO READ O.S.
```

```
LSU02420
LSU02430
LSU02440
LSU02450
LSU02460
LSU02470
LSU02480
LSU02490
LSU02500
LSU02510
LSU02520
LSU02530
LSU02540
LSU02550
LSU02560
LSU02570
LSU02580
LSU02590
LSU02600
LSU02610
LSU02620
LSU02630
LSU02640
LSU02650
LSU02660
LSU02670
LSU02680
LSU02690
LSU02700
LSU02710
LSU02720
LSU02730
LSU02740
LSU02750
LSU02760
```

LSU LOADER / SEGMENT 2 (RELOCATABLE)

```
                                        279  * THE FOLLOWING CODE ACCESSES THE DISC DEFINITION TABLE                LSU02780
                                        280  * AND LOADS THE SELCH, CONTROLER, AND DEVICE TYPE                      LSU02790
                                        281  *                                                                     LSU02800
          0000 00C6:I                   282  SET.IO   EQU   *                SET-UP TO READ OPERATING SYSTEM.      LSU02810
 0000C6:I 48F0 8972 =000A3C:I          283           LH    R15,TBNTRY       CALCULATE INDEX INTO DEVICE TABLE.    LSU02820
 0000CA:I 11F3                         284           SLLS  R15,3            :                                     LSU02830
 0000CC:I E6FF 85CA =00069A:I          285           LA    R15,DTABLE(R15)  GET ADDRESS OF REQUESTED ENTRY.       LSU02840
 0000D0:I 732F 0006                    286           LHL   R2,6(R15)        GET SELCH ADDRESS (OR FLOPPY #).      LSU02850
 0000D4:I 733F 0004                    287           LHL   R3,4(R15)        GET CONTROLLER ADDRESS.               LSU02860
 0000D8:I 734F 0000                    288           LHL   R4,0(R15)        GET DEVICE ADDRESS.                   LSU02870
 0000DC:I 735F 0002                    289           LHL   R5,2(R15)        GET DEVICE CODE.                      LSU02880
 0000E0:I C550 0038                    290           CLHI  R5,X'38'         IF DEVICE CODE IS < OR = X'38'        LSU02890
 0000E4:I 4280 80EC =0001D4:I          291           BL    CK.DISC          THEN DEVICE IS DISC.                  LSU02900
          0000 00E8:I                   292  MAGTAPE  EQU   *                                                     LSU02910
 0000E8:I 2551                         293           LCS   R5,1             SET MAG TAPE SWITCH.                  LSU02920
 0000EA:I 24E0                         294           LIS   R14,0            SET SWITCH TO INDICATE                LSU02930
 0000EC:I 40E0 8954 =000A44:I          295           STH   R14,SWITCH       READ L.I.B.                           LSU02940
 0000F0:I E6E0 81E0 =0002D4:I          296           LA    R14,OS.SIZE      GET VECTOR ADDRESS.                   LSU02950
 0000F4:I DE40 86BD =0007B5:I          297           OC    R4,MTCLEAR       CLEAR DEVICE.                         LSU02960
 0000F8:I 4240 83C6 =0004C2:I          298           BTC   4,DU            IF FALSE SYNC - NOT THERE.            LSU02970
 0000FC:I 9D4F                         299           SSR   R4,R15           IS DEVICE STILL AVAILABLE?            LSU02980
 0000FE:I 4210 83C0 =0004C2:I          300           BTC   1,DU            NO, THEN ERROR.                       LSU02990
 000102:I DE40 86B1 =0007B7:I          301           OC    R4,MTREWD        REWIND THE TAPE.                      LSU03000
 000106:I D000 88F2 =0009FC:I          302           STM   R0,RSAVE         SAVE ALL REGISTERS.                   LSU03010
 00010A:I 01F1                         303           BALR  R15,R1           OUTPUT "FILEMARKS=".                  LSU03020
 00010C:I 0771                         304           DC    Z(FMKS-LODRSTRT) :                                     LSU03030
 00010E:I 2400                         305           LIS   R0,0             INITIALIZE COUNT.                     LSU03040
          0000 0110:I                   306  GET.FMKS EQU   *                                                     LSU03050
 000110:I 41E0 843C =000550:I          307           BAL   R14,GETC         GET # OF FILEMARKS TO SKIP.           LSU03060
*000114:I 2115      =00011E:I          308           BM    END.FMKS         EXIT IF CARRIAGE RETURN DETECTED.     LSU03070
 000116:I 2601                         309           AIS   R0,1             INCREMENT COUNT.                      LSU03080
 000118:I C500 0003                    310           CLHI  R0,3             IS IT 3 YET?                          LSU03090
*00011C:I 2036      =000110:I          311           BNE   GET.FMKS         NO, GET NEXT CHARACTER.               LSU03100
          0000 011E:I                   312  END.FMKS EQU   *                                                     LSU03110
 00011E:I 41E0 8498 =0005BA:I          313           BAL   R14,ASC.HEX      CONVERT COUNT TO HEX.                 LSU03120
 000122:I 5840 88E6 =000A0C:I          314           L     R4,RSAVE+16      GET DEVICE NUMBER.                    LSU03130
          0000 0126:I                   315  SKIP.FM  EQU   *                                                     LSU03140
 000126:I 2771                         316           SIS   R7,1             ANY FILEMARKS LEFT?                   LSU03150
*000128:I 2118      =000138:I          317           BM    FMKS.DON         NO, THEN DON'T SKIP ANY MORE.         LSU03160
          0000 012A:I                   318  WAIT.FM  EQU   *                                                     LSU03170
 00012A:I 9D4F                         319           SSR   R4,R15           WAIT FOR NO MOTION.                   LSU03180
 00012C:I C4F0 0010                    320           NHI   R15,X'10'        :                                     LSU03190
*000130:I 2233      =00012A:I          321           BZ    WAIT.FM          :                                     LSU03200
 000132:I DE40 867E =0007B4:I          322           OC    R4,MTSKIP        SKIP 1 FILEMARK.                      LSU03210
*000136:I 2208      =000126:I          323           B     SKIP.FM          CONTINUE UNTIL COUNTED OUT.           LSU03220
          0000 0138:I                   324  FMKS.DON EQU   *                                                     LSU03230
 000138:I D100 88C0 =0009FC:I          325           LM    R0,RSAVE         RESTORE ALL REGISTERS.                LSU03240
 00013C:I E670 87B8 =0008F8:I          326           LA    R7,LIBBUFF       YES, GET BUFFER START ADDRESS.        LSU03250
 000140:I E680 88B3 =0009F7:I          327           LA    R8,LIBBUFFE      :    GET BUFFER END ADDRESS.          LSU03260
*000144:I                              328           B     MAG.READ         GO TO MAG TAPE HANDLER.               LSU03270
```

LSU LOADER / SEGMENT 2 (RELOCATABLE)

```
                                                330  *        MAGNETIC TAPE OS-HANDLER                                                LSU03290
                                                331  *                                                                                LSU03300
                                                332  *   UPON FIRST ENTRY, WILL READ FIRST BLOCK FOR VOLUME                            LSU03310
                                                333  *   DESCRIPTOR CHECK.                                                            LSU03320
                                                334  *      REG 7    -    START OF BUFFER ADDRESS                                      LSU03330
                                                335  *      REG 8    -    END OF BUFFER ADDRESS                                        LSU03340
                                                336  *      SWITCH   -    CONTAINS 0 (ZERO)                                            LSU03350
                                                337  *                                                                             LSU03360
                                                338  *   SECOND ENTRY WILL READ ANY ADDITIONAL LIB'S TO LIBBUF                         LSU03370
                                                339  *   TO BY-PASS THEM. THEN OS WILL BE STORED FROM LOC 0.                           LSU03380
                                                340  *      SWITCH   -    CONTAINS 1                                                LSU03390
                                                341  *                                                                             LSU03400
          0000 0144:I                           342  MAG.READ EQU   *                                                             LSU03410
 000144:I 9D4F                                  343           SSR   R4,R15            WAIT FOR 'NO MOTION' ON TAPE.          LSU03420
 000146:I C3F0 0010                             344           THI   R15,X'10'         :                                      LSU03430
*00014A:I 2233       =000144:I                 345           BZ    MAG.READ          :                                      LSU03440
 00014C:I 4100 831C =00046C:I                   346           BAL   R0,ADSELCH        ADDRESS THE SELCH.                     LSU03450
 000150:I 4800 88FC =000A44:I                   347           LH    R0,SWITCH         CHECK PROGRAM SWITCH.                  LSU03460
 000154:I 2701                                  348           SIS   R0,1              :                                      LSU03470
 000156:I 4210 8046 =0001A0:I                   349           BM    READ.MAG          IF SWITCH WAS 0 THEN READ FIRST LIB.   LSU03480
 00015A:I 4220 8026 =000184:I                   350           BP    MAGRD.OS          IF SWITCH WAS 2 THEN READ OS.          LSU03490
                                                351  *                               ELSE SWITCH WAS 1, SKIP L.I.B.'S.      LSU03500
 00015E:I 4800 88EA =000A4C:I                   352           LH    R0,NUM.LIBS       GET # OF LIB'S TO SKIP.                LSU03510
*000162:I 2339       =000174:I                 353           BZ    AMAGTE            IF NONE, GO READ O.S.                  LSU03520
 000164:I 41E0 8038 =0001A0:I                   354           BAL   R14,READ.MAG      ELSE, READ A LOADER INFO BLOCK.        LSU03530
 000168:I 2701                                  355           SIS   R0,1              DECREMENT COUNT                        LSU03540
 00016A:I 4000 88DE =000A4C:I                   356           STH   R0,NUM.LIBS       NO, SAVE COUNTER                       LSU03550
*00016E:I 2333       =000174:I                 357           BZ    AMAGTE            FINISHED?                              LSU03560
 000170:I 4300 FFDC =000144:I                   358           B     MAG.READ          GO READ NEXT LIB                       LSU03570
          0000 0174:I                           359  AMAGTE   EQU   *                                                             LSU03580
 000174:I 2402                                  360           LIS   R0,2              SET SWITCH TO INDICATE                 LSU03590
 000176:I 4000 88CA =000A44:I                   361           STH   R0,SWITCH         READ O.S.                              LSU03600
*00017A:I 2470                                  362           LI    R7,0              GET BEGINNING OF MEMORY                LSU03610
*00017C:I C880 00FF                             363           LI    R8,255            THRU 256 BYTES                         LSU03620
 000180:I 4300 FFC0 =000144:I                   364           B     MAG.READ          GO READ FIRST OS BLOCK                 LSU03630
                                                365  *                                                                             LSU03640
          0000 0184:I                           366  MAGRD.OS EQU   *                                                             LSU03650
 000184:I 41E0 8018 =0001A0:I                   367           BAL   R14,READ.MAG      READ 1 SECTOR OF O.S.                  LSU03660
 000188:I 5580 88BC =000A48:I                   368           CL    R8,OS.END         END OF LOAD?                           LSU03670
 00018C:I 4330 81D0 =000360:I                   369           BE    EXEC.OS           YES, EXECUTE THE O.S.                  LSU03680
 000190:I 4380 8336 =0004CA:I                   370           BNL   UNRE              NO, THEN ERROR.                        LSU03690
*000194:I CA70 0100                             371           AI    R7,256            INCREMENT START ADDRESS.               LSU03700
*000198:I CA80 0100                             372           AI    R8,256            INCREMENT END ADDRESS.                 LSU03710
 00019C:I 4300 FFA4 =000144:I                   373           B     MAG.READ          GO SET NEXT READ                       LSU03720
                                                374  *                                                                             LSU03730
          0000 01A0:I                           375  READ.MAG EQU   *                                                             LSU03740
 0001A0:I DE40 8612 =0007B6:I                   376           OC    R4,MTREAD         ISSUE READ CMD TO MAG TAPE.            LSU03750
 0001A4:I DE20 8611 =0007B9:I                   377           OC    R2,SHSORD         ISSUE READ CMD TO SELCH.               LSU03760
 0001A8:I 9D4F                                  378           SSR   R4,R15            IF NOT FALSE SYNC, CONFIG ERROR.       LSU03770
 0001AA:I C5F0 0004                             379           CLHI  R15,X'04'         :                                      LSU03780
 0001AE:I 4230 8320 =0004D2:I                   380           BNE   CNFG              :                                      LSU03790
          0000 01B2:I                           381  WAIT.MAG EQU   *                                                             LSU03800
 0001B2:I 9D2F                                  382           SSR   R2,R15            GET STATUS AND                         LSU03810
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

```
0001B4:I  2081      =0001B2:I   383   BTBS  BSY,WAIT.MAG     LOOP UNTIL NOT BUSY.                  LSU03820
0001B6:I  DE20 85FE =0007B8:I   384   OC    R2,SHCLEAR       CLEAR THE SELCH.                      LSU03830
0001BA:I  9B23                  385   RDR   R2,R3            GET 1ST BYTE OF FINAL ADDRESS.        LSU03840
0001BC:I  9926                  386   RHR   R2,R6            GET LAST 2 BYTES OF FINAL ADDRESS.    LSU03850
0001BE:I  3433                  387   EXHR  R3,R3            COMBINE BOTH SECTIONS TO              LSU03860
0001C0:I  0A63                  388   AR    R6,R3            GET FINAL ADDRESS.                    LSU03870
0001C2:I  0568                  389   CLR   R6,R8            FINAL ADDRESS = END ADDRESS?          LSU03880
0001C4:I  033F                  390   BER   R14              YES, RETURN TO CALLER.                LSU03890
0001C6:I  9D4F                  391   SSR   R4,R15           NO, GET STATUS OF TAPE.               LSU03900
0001C8:I  C3F0 0040             392   THI   R15,X'40'        NO, END-OF-FILE?                      LSU03910
0001CC:I  4230 8190 =000360:I   393   BNZ   EXEC.OS          YES, EXECUTE THE O.S.                 LSU03920
0001D0:I  4300 82F6 =0004CA:I   394   B     UNRE             ELSE, UNRECOVERABLE ERROR.            LSU03930
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

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                0000 01D4:I                396  CK.DISC  EQU   *                                                    LSU03950
 0001D4:I       CB50 0034                  397           SHI   R5,X'34'          CALCULATE INDEX TO SECTOR TABLE.  LSU03960
*0001D8:I       2113       =0001DE:I       398           BM    CK.DISC1         IF < 0 THEN 0.                   LSU03970
 0001DA:I       1151                       399           SLLS  R5,1             ELSE MULTIPLY BY 2.              LSU03980
*0001DC:I       2302       =0001E0:I       400           B     VD.READ          GO READ VOLUME DESCRIPTOR.       LSU03990
                                           401  *                                                                 LSU04000
                0000 01DE:I                402  CK.DISC1 EQU   *                                                    LSU04010
 0001DE:I       2450                       403           LIS   R5,0             SET INDEX TO 0 (2.5 OR 5).       LSU04020
*0001E0:I                                  404           B     VD.READ          GO READ VOLUME DESCRIPTOR.       LSU04030
                                           405  *                                                                 LSU04040
                0000 01E0:I                406  VD.READ  EQU   *               READ VOLUME DESCRIPTOR.          LSU04050
 0001E0:I       E670 8610 =0007F4:I        407           LA    R7,VDBUF         GET BUFFER START ADDRESS.        LSU04060
 0001E4:I       E680 870B =0008F3:I        408           LA    R8,VDBUFE        GET BUFFER END ADDRESS.          LSU04070
 0001E8:I       24C0                       409           LIS   R12,0            SET LOGICAL SECTOR NO TO 0       LSU04080
 0001EA:I       41E0 8176 =000364:I        410           BAL   R14,READ         READ VOLUME DESCRIPTOR.          LSU04090
 0001EE:I       D000 880A =0009FC:I        411           STM   R0,RSAVE         SAVE ALL REGISTERS.              LSU04100
 0001F2:I       5860 85FE =0007F4:I        412           L     R6,VD.VOL        GET VOLUME NAME,                 LSU04110
 0001F6:I       5060 8556 =000750:I        413           STA   R6,VOLFIL+4      AND STORE IN MESSAGE.            LSU04120
 0001FA:I       01F1                       414           BALR  R15,R1           OUTPUT "VOL=XXXX,FILE=".         LSU04130
 0001FC:I       0744                       415           DC    Z(VOLFIL-LODRSTRT) :                                LSU04140
 0001FE:I       F8E0 2020 2020             416           LI    R14,C'    '      SET FILE NAME TO BLANKS.         LSU04150
 000204:I       08FE                       417           LR    R15,R14          :                                LSU04160
 000206:I       D0E0 884A =000A54:I        418           STM   R14,FILENAME     :                                LSU04170
 00020A:I       50E0 884E =000A5C:I        419           ST    R14,EXT          SET EXTENSION TO BLANKS.         LSU04180
 00020E:I       2480                       420           LIS   R8,0             SET ACCOUNT # TO ZERO.           LSU04190
 000210:I       D280 884B =000A5F:I        421           STB   R8,EXT+3         :                                LSU04200
 000214:I       E650 883C =000A54:I        422           LA    R5,FILENAME      GET DESTINATION ADDR FOR FILENAME. LSU04210
                0000 0218:I                423  GET.FLNM EQU   *                                                    LSU04220
 000218:I       41E0 8334 =000550:I        424           BAL   R14,GETC         GET A CHARACTER.                 LSU04230
 00021C:I       4210 804A =00026A:I        425           BM    GET.FILE         EXIT IF CARRIAGE RETURN DETECTED. LSU04240
 000220:I       C570 002E                  426           CLHI  R7,C'.'          IS IT A PERIOD?                  LSU04250
*000224:I       2339       =000236:I       427           BE    GET.EXT          YES, GET EXTENSION.              LSU04260
 000226:I       C570 002F                  428           CLHI  R7,C'/'          NO, IS IT A SLASH?               LSU04270
 00022A:I       4330 8022 =000250:I        429           BE    GET.ACT          YES, GET ACCOUNT NUMBER.         LSU04280
 00022E:I       D275 0000                  430           STB   R7,0(R5)         NO, SAVE BYTE OF FILENAME.       LSU04290
 000232:I       2651                       431           AIS   R5,1             BUMP FILE NAME POINTER.          LSU04300
*000234:I       220E       =000218:I       432           B     GET.FLNM         AND GET NEXT CHARACTER.          LSU04310
                                           433  *                                                                 LSU04320
                0000 0236:I                434  GET.EXT  EQU   *                                                    LSU04330
 000236:I       E650 8822 =000A5C:I        435           LA    R5,EXT           GET DESTINATION ADDR FOR EXTENSION. LSU04340
                0000 023A:I                436  GET.EXT1 EQU   *                                                    LSU04350
 00023A:I       41E0 8312 =000550:I        437           BAL   R14,GETC         GET A CHARACTER.                 LSU04360
 00023E:I       4210 8028 =00026A:I        438           BM    GET.FILE         EXIT IF CARRIAGE RETURN DETECTED. LSU04370
 000242:I       C570 002F                  439           CLHI  R7,C'/'          IS IT A SLASH?                   LSU04380
*000246:I       2335       =000250:I       440           BE    GET.ACT          YES, THEN GET ACCOUNT.           LSU04390
 000248:I       D275 0000                  441           STB   R7,0(R5)         NO, STORE BYTE OF EXTENSION.     LSU04400
 00024C:I       2651                       442           AIS   R5,1             BUMP EXTENSION POINTER,          LSU04410
*00024E:I       220A       =00023A:I       443           B     GET.EXT1         AND GET NEXT CHARACTER.          LSU04420
                                           444  *                                                                 LSU04430
                0000 0250:I                445  GET.ACT  EQU   *                                                    LSU04440
 000250:I       2480                       446           LIS   R8,0             INITIALIZE CHARACTER STRING.     LSU04450
 000252:I       2400                       447           LIS   R0,0             INITIALIZE COUNT.                LSU04460
                0000 0254:I                448  GET.ACT1 EQU   *                                                    LSU04470
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 000254:I     41E0 82F8 =000550:I       449           BAL   R14,GETC            GET ACCOUNT NUMBER.                      LSU04480
*000258:I     2115      =000262:I       450           BM    ACT.END             EXIT IF CARRIAGE RETURN DETECTED.        LSU04490
 00025A:I     2601                      451           AIS   R0,1                BUMP COUNT.                              LSU04500
 00025C:I     C500 0003                 452           CLHI  R0,3                3 CHARACTERS YET?                        LSU04510
*000260:I     2036      =000254:I       453           BNE   GET.ACT1            NO, GET NEXT ONE.                        LSU04520
              0000 0262:I               454 ACT.END   EQU   *                                                          LSU04530
 000262:I     41E0 8354 =0005BA:I       455           BAL   R14,ASC.HEX         CONVERT ACCT # TO HEX.                   LSU04540
 000266:I     D270 87F5 =000A5F:I       456           STB   R7,EXT+3            STORE THE ACCOUNT NUMBER.                LSU04550
*00026A:I                              457           B     GET.FILE            GO SEE IF WE CAN FIND THE O.S.           LSU04560
                                       458 *                                                                          LSU04570
              0000 026A:I               459 GET.FILE  EQU   *                   SEARCH DIRECTORY FOR PROPER O.S.         LSU04580
 00026A:I     D100 878E =0009FC:I       460           LM    R0,RSAVE            RESTORE ALL REGISTERS.                   LSU04590
 00026E:I     58C0 858A =0007FC:I       461           LDA   R12,VD.FDP          IS THERE A DIRECTORY?                    LSU04600
 000272:I     4330 8046 =0002BC:I       462           BZ    NO.OS               NO, THEN ERROR.                          LSU04610
              0000 0276:I               463 READ.DIR  EQU   *                                                          LSU04620
 000276:I     E670 857A =0007F4:I       464           LA    R7,VDBUF            GET START ADDR (R8) = END ADDR.          LSU04630
 00027A:I     41E0 80E6 =000364:I       465           BAL   R14,READ            READ A DIRECTORY SECTOR.                 LSU04640
 00027E:I     E660 8576 =0007F8:I       466           LA    R6,VDBUF+4          GET POINTER TO 1ST DIRECTORY ENTRY.      LSU04650
 000282:I     2405                      467           LIS   R0,5                INITIALIZE LOOP COUNTER.                 LSU04660
              0000 0284:I               468 CK.ENTRY  EQU   *                                                          LSU04670
 000284:I     D376 0024                 469           LB    R7,DIR.ATRB(R6)     GET ATTRIBUTE INFORMATION.               LSU04680
 000288:I     C370 0010                 470           THI   R7,DIRA.ACM         IS THIS ENTRY ACTIVE.                    LSU04690
*00028C:I     233F      =0002AA:I       471           BZ    NEXT.DIR            NO, CHECK NEXT ONE.                      LSU04700
 00028E:I     C370 00E0                 472           THI   R7,X'E0'            YES, IS IT A CONTIGUOUS FILE?            LSU04710
*000292:I     213C      =0002AA:I       473           BNZ   NEXT.DIR            NO, CHECK NEXT ENTRY.                    LSU04720
 000294:I     D1D0 87BC =000A54:I       474           LM    R13,FILENAME        YES, GET FILENAME.EXT/ACT.               LSU04730
 000298:I     55D6 0000                 475           CL    R13,DIR.FNM(R6)     IS IT POSSIBLY THIS FILE?                LSU04740
*00029C:I     2137      =0002AA:I       476           BNE   NEXT.DIR            NO, CHECK NEXT ENTRY.                    LSU04750
 00029E:I     55E6 0004                 477           CL    R14,DIR.FNM+4(R6)   YES, DOES THE 2ND HALF MATCH?           LSU04760
 0002A2:I     2134      =0002AA:I       478           BNES  NEXT.DIR            NO, CHECK NEXT ENTRY?                    LSU04770
 0002A4:I     55F6 0008                 479           CL    R15,DIR.EXT(R6)     YES, PROPER EXTENSION/ACCT?              LSU04780
*0002A8:I     233C      =0002C0:I       480           BE    OS.FOUND            YES, THEN WE'VE FOUND THE O.S.           LSU04790
              0000 02AA:I               481 NEXT.DIR  EQU   *                                                          LSU04800
 0002AA:I     CA60 0030                 482           AHI   R6,48               NO, BUMP DIRECTORY POINTER.              LSU04810
 0002AE:I     2701                      483           SIS   R0,1                DECREMENT THE ENTRY COUNTER.             LSU04820
 0002B0:I     4230 FFD0 =000284:I       484           BNZ   CK.ENTRY            IF NOT DONE, CHECK NEXT ENTRY.           LSU04830
 0002B4:I     58C0 853C =0007F4:I       485           LDA   R12,VDBUF           WAS THIS THE LAST DIRECTORY ENTRY?       LSU04840
 0002B8:I     4230 FFBA =000276:I       486           BNZ   READ.DIR            NO, GET THE NEXT ONE.                    LSU04850
              0000 02BC:I               487 NO.OS     EQU   *                   YES, THEN O.S. NOT FOUND.                LSU04860
 0002BC:I     4300 81FA =0004BA:I       488           B     FILNTFND            INDICATE O.S. NOT FOUND.                 LSU04870
                                       489 *                                                                          LSU04880
              0000 02C0:I               490 OS.FOUND  EQU   *                   O.S. FOUND - DETERMINE IT'S SIZE.        LSU04890
 0002C0:I     58C6 000C                 491           LDA   R12,DIR.FLBA(R6)    PICK UP FILE 1ST LBA                     LSU04900
                                       492 *                                                                          LSU04910
                                       493 * READ IN FIRST LIB RECORD TO DETERMINE NUMBER TO SKIP                      LSU04920
                                       494 *                                                                          LSU04930
 0002C4:I     5060 862C =0008F4:I       495           ST    R6,DIRSAVE          SAVE DIRECTORY POINTER                   LSU04940
 0002C8:I     E670 862C =0008F8:I       496           LA    R7,LIBBUFF          POINT TO START OF BUFFER                 LSU04950
 0002CC:I     E680 8727 =0009F7:I       497           LA    R8,LIBBUFFF         POINT TO END OF BUFFER                   LSU04960
 0002D0:I     41E0 8090 =000364:I       498           BAL   R14,READ            GET LIB RECORD                           LSU04970
              0000 02D4:I               499 OS.SIZE   EQU   *                                                          LSU04980
 0002D4:I     D3F0 8621 =0008F9:I       500           LB    R15,LIBBUFF+LIB.NLIB GET # OF L.I.B.'S                   LSU04990
 0002D8:I     0855                      501           LR    R5,R5               MAG TAPE O.S.?                           LSU05000
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

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*0002DA:I     2317      =0002E8:I      502          BNM   DISC.OS              NO, THEN MUST BE DISC.              LSU05010
 0002DC:I     5880 8624 =000904:I      503          L     R8,LIBBUFF+LIB.SEGS   GET SEGMENT SIZE.                LSU05020
 0002E0:I     2401                     504          LIS   R0,1                 SET SWITCH TO BYPASS LIB'S          LSU05030
 0002E2:I     4000 875E =000A44:I      505          STH   R0,SWITCH            IF MORE THAN ONE.                   LSU05040
*0002E6:I     2309      =0002F8:I      506          B     CALC.SIZ             GO COMPUTE OS SIZE.                 LSU05050
                                       507  *                                                                     LSU05060
              0000 02E8:I              508  DISC.OS  EQU   *                                                       LSU05070
 0002E8:I     5860 8608 =0008F4:I      509          L     R6,DIRSAVE           RESTORE DIRECTORY POINTER           LSU05080
 0002EC:I     58C6 000C                510          L     R12,DIR.FLBA(R6)     GET 1ST SECTOR # IN FILE.           LSU05090
 0002F0:I     5886 0010                511          L     R8,DIR.LLBA(R6)      GET LAST SECTOR # IN FILE.          LSU05100
 0002F4:I     0B8C                     512          SR    R8,R12               GET SIZE OF O.S. IN SECTORS.        LSU05110
 0002F6:I     0ACF                     513          AR    R12,R15              ADJUST FOR L.I.B RECORDS.           LSU05120
              0000 02F8:I              514  CALC.SIZ EQU   *                                                       LSU05130
 0002F8:I     27F1                     515          SIS   R15,1                ALLOW FOR L.I.B. ALREADY READ.      LSU05140
 0002FA:I     40F0 874E =000A4C:I      516          STH   R15,NUM.LIBS         SAVE REMAINING # OF L.I.B.'S.       LSU05150
 0002FE:I     0B8F                     517          SR    R8,R15               ADJUST SIZE FOR L.I.B. RECORDS.     LSU05160
 000300:I     1188                     518          SLLS  R8,8                 SECTORS*256 = BYTES.                LSU05170
 000302:I     2781                     519          SIS   R8,1                 CALCULATE END ADDR FOR MAG READ.    LSU05180
 000304:I     5080 8740 =000A48:I      520          ST    R8,OS.END            SAVE BYTE LENGTH OF O.S.            LSU05190
 000308:I     2681                     521          AIS   R8,1                 READJUST FOR MEMORY TEST.           LSU05200
                                       522  *                                                                     LSU05210
                                       523  * TEST FROM TOP OF LOADER TO TOP OF OS                               LSU05220
                                       524  *                                                                     LSU05230
 00030A:I     D000 86EE =0009FC:I      525          STM   R0,RSAVE             SAVE REGISTERS                      LSU05240
*00030E:I     CA80 0A58                526          AI    R8,LODREND-LODRSTRT  ALLOW FOR LOADER RELOCATION         LSU05250
 000312:I     0828                     527          LR    R2,R8                GET END ADDRESS.                    LSU05260
 000314:I     E6D0 8748 =000A60:I      528          LA    R13,LODREND          GET START ADDRESS.                  LSU05270
 000318:I     50D0 8734 =000A50:I      529          ST    R13,ENDLODR          SAVE FOR USE AFTER RELOCATION.      LSU05280
 00031C:I     41E0 82DA =0005FA:I      530          BAL   R14,MEM.TEST         TEST MEMORY                         LSU05290
                                       531  *                                                                     LSU05300
                                       532  * RELOCATE LOADER ABOVE O.S.                                          LSU05310
                                       533  *                                                                     LSU05320
*000320:I     CB80 0A58                534          SI    R8,LODREND-LODRSTRT  CORRECT UPPER LIMIT                 LSU05330
 000324:I     E620 FCE0 =000008:I      535          LA    R2,LODRSTRT          LOAD START ADDRESS                  LSU05340
*000328:I     C830 0A58                536          LI    R3,LODREND-LODRSTRT  GET LENGTH OF MOVE.                 LSU05350
              0000 032C:I              537  MOVE.LDR EQU   *                                                       LSU05360
 00032C:I     5802 4300 0000           538          L     R0,0(R2,R3)          LOAD DATA                           LSU05370
 000332:I     5008 4300 0000           539          ST    R0,0(R8,R3)          STORE DATA                          LSU05380
 000338:I     2734                     540          SIS   R3,4                 DECREMENT LENGTH.                   LSU05390
*00033A:I     2217      =00032C:I      541          BNM   MOVE.LDR             AND CONTINUE UNITL COUNTED OUT.     LSU05400
 00033C:I     D100 86BC =0009FC:I      542          LM    R0,RSAVE             RESTORE REGISTERS.                  LSU05410
*000340:I     CA80 033E                543          AAI   R8,GET.OS-LODRSTRT   GET ADDRESS OF RELOCATED LOADER.    LSU05420
 000344:I     0308                     544          BR    R8                   GO TO RELOCATED LOADER.             LSU05430
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

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                0000 0346:I                546  GET.OS   EQU   *                                                    LSU05450
000346:I        D000 86B2 =0009FC:I        547           STM   R0,RSAVE          SAVE ALL REGISTERS.              LSU05460
00034A:I                                   548           IFZ   TEST                                             LSU05470
00034A:I        24D0                       549           LIS   R13,0             GET START ADDRESS.               LSU05480
                                           550           ELSE                                                   LSU05490
                                           551           LA    R13,X'A00'        GET START ADDRESS.               LSU05500
                                           552           ENDC                                                   LSU05510
00034C:I        5820 8700 =000A50:I        553           L     R2,ENDLODR        GET END ADDRESS.                 LSU05520
000350:I        41E0 82A6 =0005FA:I        554           BAL   R14,MEM.TEST      TEST MEMORY THAT HELD LOADER.    LSU05530
000350:I                                   555           IFNZ  TEST                                             LSU05540
                                           556           LIS   R13,0             GET START ADDRESS.               LSU05550
                                           557           LA    R2,X'2FC'         GET END ADDRESS.                 LSU05560
                                           558           BAL   R14,MEM.TEST      TEST LOW MEMORY.                 LSU05570
                                           559           ENDC                                                   LSU05580
000354:I        D100 86A4 =0009FC:I        560           LM    R0,RSAVE          RESTORE ALL REGISTERS.           LSU05590
000358:I        2781                       561           SIS   R8,1              GET END ADDRESS OF O.S.           LSU05600
00035A:I        2470                       562           LIS   R7,0              GET START ADDRESS OF O.S.         LSU05610
00035C:I        41E0 8004 =000364:I        563           BAL   R14,READ          GO READ THE O.S.                 LSU05620
                0000 0360:I                564  EXEC.OS  EQU   *                                                    LSU05630
000360:I        4300 0060                  565           B     OS.START          EXECUTE THE O.S.                 LSU05640
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

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                0000 0364:I                 567 RFAD     EQU   *                                                    LSU05660
000364:I        0855                        568          LR    R5,R5              MAG TAPE O.S.?                    LSU05670
000366:I        4210 FDDA =000144:I         569          BM    MAG.READ           YES, THEN READ FROM MAG TAPE.     LSU05680
00036A:I        C550 0006                   570          CLHI  R5,Y'37'-X'34'**2  NO, IS IT A FLOPPY DISC?          LSU05690
00036E:I        4330 8118 =00048A:I         571          BF    FLP.READ           YES, GO TO FLOPPY READ ROUTINE.   LSU05700
000372:I        08AC                        572          LR    R10,R12            NO, SET-UP CYLINDER:TRACK:SECTOR. LSU05710
000374:I        4DA5 8448 =0007C0:I         573          DH    R10,SECCYL(R5)                                       LSU05720
000378:I        089B                        574          LR    R9,R11             (R9) = CYLINDER.                  LSU05730
00037A:I        4DA5 8448 =0007C6:I         575          DH    R10,SECTRK(R5)     (R10) = SECTOR.                   LSU05740
                                            576 *                                  (R11) = TRACK.                    LSU05750
00037E:I        0855                        577          LR    R5,R5              IS IT 67 MB OR LARGER?            LSU05760
000380:I        4220 8038 =0003BC:I         578          BP    RDSK2                                                LSU05770
                                            579 *                                                                   LSU05780
                                            580 * 2.5 OR 10 MB DISK INPUT ROUTINE                                   LSU05790
                                            581 *                                                                   LSU05800
000384:I        DE30 8430 =0007B8:I         582          OC    R3,CTRESET         RESET CONTROLLER                  LSU05810
000388:I        4240 8136 =0004C2:I         583          BTC   4,DU               IF FALSE SYNC - NO CONTROLLER.    LSU05820
                0000 038C:I                 584 WAIT10   EQU   *                                                    LSU05830
00038C:I        9D3F                        585          SSR   R3,R15             GET CONTROLLER STATUS             LSU05840
00038E:I        2221      =00038C:I         586          BFBS  2,WAIT10           AND WAIT FOR IDLE.                LSU05850
                0000 0390:I                 587 WAIT15   EQU   *                                                    LSU05860
000390:I        9D4F                        588          SSR   R4,R15             GET STATUS OF DEVICE.             LSU05870
000392:I        4210 812C =0004C2:I         589          BTC   1,DU               IF UNAVAILABLE, THEN ERROR.       LSU05880
000396:I        C3F0 0010                   590          THI   R15,X'10'                                            LSU05890
*00039A:I       2035      =000390:I         591          BNZ   WAIT15                                               LSU05900
00039C:I        11B5                        592          SLLS  R11,5                                                LSU05910
00039E:I        06AB                        593          OR    R10,R11                                              LSU05920
                0000 03A0:I                 594 RDKLOOP1 EQU   *                                                    LSU05930
0003A0:I        9849                        595          WHR   R4,R9              SEND CYLINDER # TO DISC.          LSU05940
0003A2:I        4240 811C =0004C2:I         596          BTC   4,DU               IF FALSE SYNC - NO DEVICE.        LSU05950
0003A6:I        DE40 8411 =0007BB:I         597          OC    R4,D1SEEK          ELSE, ISSUE A SEEK.               LSU05960
                0000 03AA:I                 598 WAIT11   EQU   *                                                    LSU05970
0003AA:I        9D3F                        599          SSR   R3,R15             GET CONTROLLER STATUS             LSU05980
0003AC:I        2221      =0003AA:I         600          BFBS  2,WAIT11           AND WAIT FOR IDLE.                LSU05990
                0000 03AE:I                 601 WAIT12   EQU   *                                                    LSU06000
0003AE:I        9D4F                        602          SSR   R4,R15             GET DEVICE STATUS.                LSU06010
0003B0:I        4270 8116 =0004CA:I         603          BTC   7,UNRE             IF "SEEK INCOMPLETE" - ERROR.     LSU06020
0003B4:I        2083      =0003AE:I         604          BTBS  BSY,WAIT12         ELSE, WAIT FOR DISC READY.        LSU06030
0003B6:I        4160 805E =000418:I         605          BAL   R6,DKCOMMON        GO TO DISC READ ROUTINE.          LSU06040
*0003BA:I       220D      =0003A0:I         606          B     RDKLOOP1           READ NEXT CYLINDER.               LSU06050
                                            607 *                                                                   LSU06060
                0000 03BC:I                 608 RDSK2    EQU   *                  SET-UP READ FOR 67MB OR 256MB DISC. LSU06070
0003BC:I        9D4F                        609          SSR   R4,R15             GET STATUS OF DEVICE.             LSU06080
0003BE:I        C3F0 0019                   610          THI   R15,X'19'          SAFE? READY? ON-LINE?             LSU06090
0003C2:I        4230 8104 =0004CA:I         611          BNZ   UNRE               NO, ERROR.                        LSU06100
0003C6:I        C5F0 0004                   612          CLHI  R15,X'04'          IS DEVICE AVAILABLE?              LSU06110
0003CA:I        4330 80F4 =0004C2:I         613          BE    DU                 NO, ERROR.                        LSU06120
                0000 03CE:I                 614 RDKLOOP2 EQU   *                                                    LSU06130
0003CE:I        DE40 83EA =0007BC:I         615          OC    R4,D2RATTN         RESET ATTENTION FLIP FLOP         LSU06140
                0000 03D2:I                 616 WAIT21   EQU   *                                                    LSU06150
0003D2:I        9D3F                        617          SSR   R3,R15             GET CONTROLLER STATUS.            LSU06160
0003D4:I        C5F0 0004                   618          CLHI  R15,X'04'          FALSE SYNC?                       LSU06170
0003D8:I        4330 80E6 =0004C2:I         619          BE    DU                 YES, THEN ERROR.                  LSU06180
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

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0003DC:I     2225      =0003D2:I       620            BFBS  2,WAIT21          NO, WAIT FOR CONTROLLER IDLE.          LSU06190
0003DE:I     9849                      621            WHR   R4,R9              SEND CYLINDER # TO DEVICE.             LSU06200
0003E0:I     DE40 83DA =0007BE:I       622            OC    R4,D2SETCYL        SET CYLINDER.                          LSU06210
             0000 03E4:I               623  WAIT22    EQU   *                                                         LSU06220
0003E4:I     9D3F                      624            SSR   R3,R15             GET CONTROLLER STATUS                  LSU06230
0003E6:I     2221      =0003E4:I       625            BFBS  2,WAIT22           AND WAIT FOR IDLE.                     LSU06240
0003E8:I     DE40 83D1 =0007BD:I       626            OC    R4,D2RHEAD         CLEAR HEAD REGISTER.                   LSU06250
             0000 03EC:I               627  WAIT23    EQU   *                                                         LSU06260
0003EC:I     9D3F                      628            SSR   R3,R15             GET CONTROLLER STATUS                  LSU06270
0003EE:I     2221      =0003EC:I       629            BFBS  2,WAIT23           AND WAIT FOR IDLE.                     LSU06280
0003F0:I     984B                      630            WHR   R4,R11             SEND HEAD # TO DEVICE.                 LSU06290
0003F2:I     DE40 83C9 =0007BF:I       631            OC    R4,D2SETHED        SET HEAD.                              LSU06300
             0000 03F6:I               632  WAIT24    EQU   *                                                         LSU06310
0003F6:I     9D3F                      633            SSR   R3,R15             GET CONTROLLER STATUS                  LSU06320
0003F8:I     2221      =0003F6:I       634            BFBS  2,WAIT24           AND WAIT FOR IDLE.                     LSU06330
0003FA:I     DE40 83BD =0007BB:I       635            OC    R4,D2SEEK          ISSUE A SEEK.                          LSU06340
             0000 03FE:I               636  WAIT25    EQU   *                                                         LSU06350
0003FE:I     9D3F                      637            SSR   R3,R15             GET CONTROLLER STATUS                  LSU06360
000400:I     2221      =0003FE:I       638            BFBS  2,WAIT25           AND WAIT FOR IDLE.                     LSU06370
             0000 0402:I               639  WAIT26    EQU   *                                                         LSU06380
000402:I     9D4F                      640            SSR   R4,R15             GET DEVICE STATUS                      LSU06390
000404:I     2081      =000402:I       641            BTBS  BSY,WAIT26         AND WAIT FOR NOT BUSY.                 LSU06400
000406:I     C3F0 0053                 642            THI   R15,X'53'          UNSAFE? SEEK INC? NOT READY?           LSU06410
00040A:I     4230 80BC =0004CA:I       643            BNZ   UNRE               IF ANY, THEN ERROR.                    LSU06420
00040E:I     06DB                      644            LR    R13,R11            ELSE, GET TRACK #,                     LSU06430
000410:I     11DA                      645            SLLS  R13,10             AND COMBINE WITH CYLINDER.             LSU06440
000412:I     06D9                      646            OR    R13,R9             :                                      LSU06450
000414:I     E660 FFB6 =0003CE:I       647            LA    R6,RDKLOOP2        GET RETURN ADDRESS,                    LSU06460
*000418:I                              648            B     DKCOMMON           AND READ FROM THE DISC.                LSU06470
                                       649  *                                                                         LSU06480
             0000 0418:I               650  DKCOMMON  EQU   *                  COMMON DISC READ ROUTINE.              LSU06490
000418:I     4100 8050 =00046C:I       651            BAL   R0,ADSELCH         ADDRESS THE SELCH.                     LSU06500
00041C:I     0855                      652            LR    R5,R5              IS DISC 67MB OR LARGER?                LSU06510
00041F:I     2124      =000426:I       653            BPS   COMN1             YES.                                   LSU06520
000420:I     9849                      654            WHR   R4,R9              NO, SEND THE CYLINDER #.               LSU06530
000422:I     9A3A                      655            WDR   R3,R10             :   SEND THE SECTOR #.                 LSU06540
*000424:I    2303      =00042A:I       656            B     COMN2                                                    LSU06550
                                       657  *                                                                         LSU06560
             0000 0426:I               658  COMN1     EQU   *                                                         LSU06570
000426:I     9A3A                      659            WDR   R3,R10                                                   LSU06580
000428:I     983D                      660            WHR   R3,R13                                                   LSU06590
             0000 042A:I               661  COMN2     EQU   *                                                         LSU06600
00042A:I     DE30 838C =0007BA:I       662            OC    R3,CTREAD          READ -> CTRL                           LSU06610
00042E:I     DE20 8387 =0007B9:I       663            OC    R2,SHGORD          GO & READ -> SELCH                     LSU06620
000432:I     9D3F                      664            SSR   R3,R15             IF NOT FALSE SYNC ON CONTROLLER,       LSU06630
000434:I     C5F0 0004                 665            CLHI  R15,X'04'          THEN CONFIG ERROR.                     LSU06640
000438:I     4230 8096 =0004D2:I       666            BNE   CNFG               :                                      LSU06650
             0000 043C:I               667  WAIT31    EQU   *                                                         LSU06660
00043C:I     9D2F                      668            SSR   R2,R15             WAIT FOR SELCH NOT BUSY.               LSU06670
00043E:I     2081      =00043C:I       669            BTBS  BSY,WAIT31         :                                      LSU06680
000440:I     DE20 8374 =0007B8:I       670            OC    R2,SHCLEAR         CLEAR THE SELCH.                       LSU06690
000444:I     9B20                      671            RDR   R2,R0              READ 1ST BYTE OF END ADR (0:23<-0)     LSU06700
000446:I     992D                      672            RHR   R2,R13             READ THE REST OF END ADR (0:16<-0)     LSU06710
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

```
000448:I  3400                          673          EXHR  R0,R0      SHIFT 1ST BYTE LEFT BY 1 HALFWORD.      LSU06720
00044A:I  060D                          674          OR    R0,R13     GET FULL ENDING ADDRESS.                LSU06730
          0000 044C:I                   675  WAIT32  EQU   *                                                   LSU06740
00044C:I  9D3F                          676          SSR   R3,R15     GET CONTROLLER STATUS                   LSU06750
00044E:I  2221      =00044C:I           677          BFBS  2,WAIT32   AND WAIT FOR IDLE.                      LSU06760
000450:I  4210 8076 =0004CA:I           678          BTC   1,UNRE     IF DATA TRANSFER ERROR - ERROR.         LSU06770
000454:I  C3F0 0010                     679          TBI   R15,X'10'  CYLINDER OVERFLOW?                      LSU06780
000458:I  033E                          680          BZR   R14        NO, RETURN                              LSU06790
00045A:I  0B07                          681          SR    R0,R7      YES, GET LENGTH OF DATA BLOCK READ.     LSU06800
00045C:I  2604                          682          AIS   R0,4       :                                       LSU06810
00045E:I  C400 FF00                     683          NHI   R0,X'FF00' ADJUST TO 256-BYTE BOUNDARY.            LSU06820
000462:I  0A70                          684          AR    R7,R0      GET NEW START ADDRESS.                  LSU06830
000464:I  2691                          685          AIS   R9,1       INCREMENT CYLINDER NUMBER.              LSU06840
000466:I  24A0                          686          LIS   R10,0      INITIALIZE SECTOR.                      LSU06850
000468:I  24B0                          687          LIS   R11,0      INITIALIZE TRACK.                       LSU06860
00046A:I  0306                          688          BR    R6         SET-UP TO READ AGAIN.                   LSU06870
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

```
            0000 046C:I                690  ADSELCH  EQU   *                ADDRESS SELCH SUBROUTINE.          LSU06890
00046C:I    DE20 8348 =0007B8:I        691           OC    R2,SHCLEAR       CLEAR THE SELCH.                   LSU06900
000470:I    4240 804E =0004C2:I        692           BTC   4,DU             IF FALSE SYNC, SELCH NOT THERE.    LSU06910
            0000 0474:I                693  SLC.WAIT EQU   *                                                   LSU06920
000474:I    9D2F                       694           SSR   R2,R15           GET SELCH STATUS AND               LSU06930
000476:I    2C81      =000474:I        695           BTBS  BSY,SLC.WAIT     LOOP UNTIL NOT BUSY.               LSU06940
000478:I    3477                       696           EXHR  R7,R7            SEND START ADDRESS TO SELCH.       LSU06950
00047A:I    9A27                       697           WDR   R2,R7            :                                  LSU06960
00047C:I    3477                       698           EXHR  R7,R7            :                                  LSU06970
00047E:I    9827                       699           WHR   R2,R7            :                                  LSU06980
000480:I    3488                       700           EXHR  R8,R8            SEND END ADDRESS TO SELCH.         LSU06990
000482:I    9A28                       701           WDR   R2,R8            :                                  LSU07000
000484:I    3488                       702           EXHR  R8,R8            :                                  LSU07010
000486:I    9828                       703           WHR   R2,R8            :                                  LSU07020
000488:I    0300                       704           BR    R0               RETURN TO CALLER.                  LSU07030
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                0000 048A:I                706  FLP.READ EQU   *                FLOPPY READ ROUTINE.                LSU07050
 00048A:I       9D4F                       707           SSR   R4,R15           IF FLOPPY NOT IDLE                  LSU07060
 00048C:I       4320 8032 =0004C2:I        708           BFC   2,DU            THEN ERROR.                         LSU07070
 000490:I       CACC 0001                  709           AHI   R12,1(R12)      CALCULATE RECORD NUMBER,            LSU07080
 000494:I       984C                       710           WHR   R4,R12          AND SEND IT TO THE FLOPPY.          LSU07090
 000496:I       4240 6028 =0004C2:I        711           BTC   4,DU            IF FALSE SYNC - NO DEVICE.          LSU07100
 00049A:I       C8F2 0001                  712           LHI   R15,1(R2)       GET THE READ COMMAND,               LSU07110
 00049E:I       9E4F                       713           OCR   R4,R15          AND SEND IT TO THE FLOPPY.          LSU07120
 0004A0:I       0B78                       714           SR    R7,R8           GET BUFFER INDEX.                   LSU07130
                0000 04A2:I                715  FLP.DATA EQU   *                                                   LSU07140
 0004A2:I       9D4F                       716           SSR   R4,R15          GET STATUS.                         LSU07150
*0004A4:I       2081       =0004A2:I       717           BTC   BSY,FLP.DATA    LOOP UNITL NOT BUSY.                LSU07160
 0004A6:I       DB48 4700 0000             718           RD    R4,0(R8,R7)     READ A BYTE.                        LSU07170
 0004AC:I       2671                       719           AIS   R7,1            BUMP BUFFER INDEX,                  LSU07180
*0004AF:I       2226       =0004A2:I       720           BNT   FLP.DATA        AND READ UNTIL COUNTED OUT.         LSU07190
 0004B0:I       24F7                       721           LIS   R15,7           ISSUE STOP COMMAND.                 LSU07200
 0004B2:I       9E4F                       722           OCR   R4,R15          :                                   LSU07210
                0000 04B4:I                723  FLP.WAIT EQU   *                                                   LSU07220
 0004B4:I       9D4F                       724           SSR   R4,R15          GET THE STATUS AND                  LSU07230
 0004B6:I       2221       =0004B4:I       725           BFBS  2,FLP.WAIT      WAIT UNTIL IDLE.                    LSU07240
 0004B8:I       C30E                       726           BR    R14                                               LSU07250
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

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                                                  728  * ERROR ROUTINES                                                                LSU07270
                                                  729  *                                                                               LSU07280
                                                  730  * FILE NOT FOUND                                                                 LSU07290
                                                  731  *                                                                               LSU07300
                                                  732  FILNTFND EQU   *                                                                LSU07310
          0000 04BA:I                             733           BALR  R15,R1              OUTPUT "FILE NOT FOUND".                    LSU07320
 0004BA:I 01F1                                    734           DC    Z(MSG3-LODRSTRT)    :                                           LSU07330
 0004BC:I 0789                                    735           B     ERROR               COMMON ERROR ROUTINE                        LSU07340
 0004BE:I 4300 8048 =00050A:I                     736  *                                                                               LSU07350
                                                  737  DU       EQU   *                                                                LSU07360
          0000 04C2:I                             738           LI    R7,C'DU  '          SET-UP ERROR MESSAGE.                       LSU07370
 0004C2:I F870 4455 2020                          739           B     IOERROR             :                                           LSU07380
*0004C8:I 2308       =0004D8:I                   740  *                                                                               LSU07390
                                                  741  UNRE     EQU   *                                                                LSU07400
          0000 04CA:I                             742           LI    R7,C'UNRE'          UNRECOVERABLE ERROR.                        LSU07410
 0004CA:I F870 554F 5245                          743           B     IOERROR             :                                           LSU07420
*0004D0:I 2304       =0004D8:I                   744  *                                                                               LSU07430
                                                  745  CNFG     EQU   *                                                                LSU07440
          0000 04D2:I                             746           LI    R7,C'CNFG'          CONFIGURATION ERROR.                        LSU07450
 0004D2:I F870 434E 4647                          747           B     IOERROR             :                                           LSU07460
*0004D8:I                                         748  *                                                                               LSU07470
                                                  749  IOERROR  EQU   *                   I/O ERROR MESSAGE.                          LSU07480
          0000 04D8:I                             750           ST    R7,IO.TYPE          COMPLETE THE MESSAGE.                       LSU07490
 0004D8:I 5070 82B0 =00078C:I                     751           BALR  R15,R1              OUTPUT "I/O ERROR...."                      LSU07500
 0004DC:I C1F1                                    752           DC    Z(MSG1-LODRSTRT)    :                                           LSU07510
 0004DE:I C77C                                    753           B     ERROR               GO TO COMMON ERROR ROUTINE                  LSU07520
 0004E0:I 4300 8026 =00050A:I                     754  *                                                                               LSU07530
                                                  755  MEM.ERR  EQU   *                   MEMORY TEST FAILED.                         LSU07540
          0000 04E4:I                             756           LR    R15,R13             GET LEAST SIGNIFICANT BYTE.                 LSU07550
 0004E4:I 08FD                                    757           SRL   R13,8               SHIFT IT OFF.                               LSU07560
*0004E6:I 10D8                                    758           BAL   R14,HEX.ASC         CONVERT IT TO ASCII.                        LSU07570
 0004E8:I 41E0 8094 =000580:I                     759           STH   R15,MFAD+4          SAVE FOR ERROR MESSAGE.                     LSU07580
 0004EC:I 40FC 82C0 =0007B0:I                     760           LR    R15,R13             GET MIDDLE BYTE OF ADDRESS.                 LSU07590
 0004F0:I 08FD                                    761           SRL   R13,8               SHIFT IT OFF.                               LSU07600
*0004F2:I 10D8                                    762           BAL   R14,HEX.ASC         CONVERT IT TO ASCII.                        LSU07610
 0004F4:I 41E0 8088 =000580:I                     763           STH   R15,MFAD+2          SAVE IT FOR ERROR MESSAGE.                  LSU07620
 0004F8:I 40FC 82B2 =0007AE:I                     764           LR    R15,R13             GET MOST SIGNIFICANT BYTE OF ADDR.          LSU07630
 0004FC:I 08FD                                    765           BAL   R14,HEX.ASC         CONVERT IT TO ASCII.                        LSU07640
 0004FE:I 41E0 807E =000580:I                     766           STH   R15,MFAD            STORE IT FOR ERROR MESSAGE.                 LSU07650
 000502:I 40F0 82A6 =0007AC:I                     767           BALR  R15,R1              OUTPUT "MEMCHK ERR NNNNNN".                 LSU07660
 000506:I 01F1                                    768           DC    Z(MSG6-LODPSTRT)    :                                           LSU07670
 000508:I 0799                                    769           B     ERROR               GO TO COMMON                                LSU07680
*00050A:I                                         770  *                                                                               LSU07690
                                                  771  *       COMMON ERROR ROUTINE                                                    LSU07700
                                                  772  *                                                                               LSU07710
          0000 050A:I                             773  ERROR    EQU   *                                                                LSU07720
 00050A:I E600 FAFA =000008:I                     774           LA    R0,LODRSTRT         GET BASE ADDRESS OF LOADER.                 LSU07730
*00050E:I C500 1000                               775           CLI   R0,LSUADDR          HAS IT BEEN MOVED YET?                      LSU07740
 000512:I 0330                                    776           BER   R0                  NO, RESTART.                                LSU07750
 000514:I                                         777           IFZ   TEST                                                            LSU07760
 000514:I 8800                                    778           HALT                      YES, THEN JUST HALT.                        LSU07770
                                                  779           ENDC                                                                  LSU07780
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

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                0000 0516:I
000516:I        486F 0000                781 MSG       EQU   *                OUTPUT MESSAGE TO CONSOLE.                LSU07800
000518:I        26F2                     782           LH    R6,0(R15)        GET MESSAGE ADDRESS.                      LSU07810
00051A:I        247D                     783           AIS   R15,2           GET RETURN ADDRESS.                       LSU07820
00051C:I        41E0 8018 =00053A:I      784           LIS   R7,CR            OUTPUT CARRIAGE RETURN.                   LSU07830
00051E:I        41E0 8018 =00053A:I      785           BAL   R14,PUTC         :                                         LSU07840
000520:I        247A                     786           LIS   R7,LF            OUTPUT LINE FEED.                         LSU07850
000522:I        41E0 8012 =00053A:I      787           BAL   R14,PUTC         :                                         LSU07860
                0000 0528:I              788 MSG.PUT   EQU   *                                                          LSU07870
000528:I        D376 FADC =000008:I      789           LB    R7,LODRSTRT(R6)  GET A CHARACTER,                          LSU07880
00052A:I        41E0 800A =00053A:I      790           BAL   R14,PUTC         AND OUTPUT IT.                            LSU07890
00052C:I        2661                     791           AIS   R6,1             BUMP THE MESSAGE POINTER.                 LSU07900
00052E:I        C570 00FF                792           CLHI  R7,X'FF'         WAS LAST CHARACTER A TERMINATOR?           LSU07910
*000530:I       2037      =000528:I      793           BNE   MSG.PUT          NO, OUTPUT NEXT CHARACTER.                LSU07920
000532:I        030F                     794           BR    R15              YES, RETURN TO CALLER.                    LSU07930
                                         795 *                                                                         LSU07940
                0000 053A:I              796 PUTC      EQU   *                OUTPUT 1 CHARACTER TO CONSOLE.             LSU07950
00053A:I        C840 0011                797           LHI   R4,X'11'         GET CONSOLE OUTPUT ADDRESS.               LSU07960
00053C:I        C800 00AB                798           LHI   R0,X'AB'         START THE CONSOLE.                        LSU07970
00053E:I        9E40                     799           OCR   R4,R0            :                                         LSU07980
                0000 0544:I              800 PUTC.L1   EQU   *                                                          LSU07990
000540:I        9D40                     801           SSR   R4,R0            LOOP TILL CONSOLE NOT BUSY.               LSU08000
000542:I        2081      =000540:I      802           BTBS  BSY,PUTC.L1      :                                         LSU08010
000544:I        9A47                     803           WDR   R4,R7            OUTPUT THE DATA.                          LSU08020
                0000 0546:I              804 PUTC.L2   EQU   *                                                          LSU08030
000546:I        9D40                     805           SSR   R4,R0            LOOP TILL CONSOLE NOT BUSY.               LSU08040
000548:I        2081      =000546:I      806           BTBS  BSY,PUTC.L2      :                                         LSU08050
00054A:I        030E                     807           BR    R14              RETURN TO CALLER.                         LSU08060
                                         808 *                                                                         LSU08070
                0000 054C:I              809 GETC      EQU   *                READ 1 CHARACTER FROM CONSOLE.             LSU08080
00054C:I        C8F0 00B9                810           LHI   R15,X'B9'        GET CONSOLE COMMAND.                      LSU08090
00054E:I        C840 0010                811           LHI   R4,X'10'         GET ADDRESS OF CONSOLE INPUT.             LSU08100
000550:I        9E4F                     812           OCR   R4,R15           OUTPUT COMMAND TO CONSOLE.                LSU08110
                0000 0552:I              813 GETC.BSY  EQU   *                                                          LSU08120
000552:I        9D4F                     814           SSR   R4,R15           LOOP UNTIL NOT BUSY.                      LSU08130
000554:I        2081      =000552:I      815           BTBS  BSY,GETC.BSY     :                                         LSU08140
000556:I        9B47                     816           RDR   R4,R7            READ A BYTE.                              LSU08150
000558:I        9D4F                     817           SSR   R4,R15           CHECK FOR FRAMING ERROR.                  LSU08160
00055A:I        C3F0 0020                818           THI   R15,X'20'        IF TRUE, THEN EITHER BREAK OR             LSU08170
00055E:I        4230 FA9E =000008:I      819           BNZ   LODRSTRT         BAD CHARACTER - RESTART.                  LSU08180
000562:I        C470 007F                820           NHI   R7,X'7F'         ASSURE 7 BITS.                            LSU08190
000566:I        C570 000D                821           CLHI  R7,CR            IS IT A CARRIAGE RETURN?                  LSU08200
*00056A:I       2133      =000578:I      822           BNE   GETC.OK          NO, PUT IT IN REGISTER.                   LSU08210
00056C:I        25F1                     823           LCS   R15,1            YES, SET RETURN TO MINUS.                 LSU08220
00056E:I        030E                     824           BR    R14              RETURN TO CALLER.                         LSU08230
                                         825 *                                                                         LSU08240
                0000 0570:I              826 GETC.OK   EQU   *                                                          LSU08250
000570:I        1188                     827           SLLS  R8,8             PACK CHARACTER INTO REGISTER.             LSU08260
000572:I        0687                     828           OR    R8,R7            :                                         LSU08270
000574:I        24F0                     829           LIS   R15,0            SET RETURN TO NON-MINUS.                  LSU08280
000576:I        030E                     830           BR    R14              RETURN TO CALLER.                         LSU08290
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                                    832  * CONVERSION ROUTINES.                                                    LSU08310
                                    833  *                                                                         LSU08320
          0000 0580:I               834  HEX.ASC  EQU   *          CONVERT HEX TO ASCII/HEX.                       LSU08330
000580:I  087F                      835           LR    R7,R15     SAVE ORIGINAL DIGITS.                          LSU08340
000582:I  10F4                      836           SRLS  R15,4      GET LEFTMOST DIGIT AND                         LSU08350
000584:I  41A0 800C =000594:I       837           BAL   R10,HEX01  CONVERT IT TO ASCII.                           LSU08360
000588:I  940F                      838           EXBR  R0,R15     SHIFT AND SAVE LEFTMOST CHARACTER.             LSU08370
00058A:I  08F7                      839           LR    R15,R7     GET RIGHTMOST DIGIT AND                        LSU08380
00058C:I  41A0 8004 =000594:I       840           BAL   R10,HEX01  CONVERT IT TO ASCII.                           LSU08390
000590:I  06F0                      841           OR    R15,R0     GET BOTH ASCII CHARACTERS.                     LSU08400
000592:I  030E                      842           BR    R14        RETURN TO CALLER.                              LSU08410
                                    843  *                                                                         LSU08420
          0000 0594:I               844  HEX01    EQU   *                                                        LSU08430
000594:I  C4F0 000F                 845           NHI   R15,X'F'                                                   LSU08440
000598:I  C6F0 0030                 846           OHI   R15,X'30'  SET DIGIT ZONE                                LSU08450
00059C:I  C9F0 003A                 847           CHI   R15,X'3A'                                                  LSU08460
0005A0:I  028A                      848           BLR   R10        RETURN TO CALLER IF NUMERIC.                   LSU08470
0005A2:I  26F7                      849           AIS   R15,7      ELSE, SET ALPHA ZONE,                          LSU08480
0005A4:I  030A                      850           BR    R10        AND RETURN TO CALLER.                          LSU08490
                                    851  *                                                                         LSU08500
          0000 05A6:I               852  X.CONV   EQU   *          CONVERT ASCII/HEX TO HEX.                      LSU08510
0005A6:I  CF80 0040                 853           SHI   R8,X'40'   STRIP OFF ALPHA ZONES.                         LSU08520
0005AA:I  2122       =0005AE:I      854           BPS   X.CONV1    POSSIBLY IN RANGE A - F?                       LSU08530
0005AC:I  2687                      855           AIS   R8,7        NO, THEN ASSUME 0 - 9.                         LSU08540
          0000 05AE:I               856  X.CONV1  EQU   *                                                        LSU08550
0005AE:I  2689                      857           AIS   R8,9        NORMALIZE FOR HEX DIGIT.                       LSU08560
0005B0:I  C580 0010                 858           CLHI  R8,X'10'   DOES RESULT EXCEED 15 (X'F')?                  LSU08570
0005B4:I  028E                      859           BLR   R14        NO, RETURN TO CALLER.                          LSU08580
0005B6:I  4300 FA4E =000008:I       860           B     LODRSTRT   YES, ERROR - RESTART.                          LSU08590
                                    861  *                                                                         LSU08600
          0000 05BA:I               862  ASC.HEX  EQU   *          CONVERT ASCII/DECIMAL TO HEX.                  LSU08610
0005BA:I  245A                      863           LIS   R5,10      INITIALIZE MULTIPLIER.                         LSU08620
0005BC:I  C890 0030                 864           LHI   R9,X'30'   MASK FOR ASCII CODED DECIMAL.                 LSU08630
0005C0:I  C8A0 00FF                 865           LHI   R10,X'FF'  MASK TO ISOLATE RIGHT BYTE.                    LSU08640
0005C4:I  2701                      866           SIS   R0,1       DECREMENT COUNT.                               LSU08650
*0005C6:I 2313       =0005CC:I      867           BNM   ASC.UNIT   IF NOT MINUS, CONVERT UNITS.                   LSU08660
0005C8:I  2470                      868           LIS   R7,0       ELSE SET VALUE TO ZERO,                        LSU08670
0005CA:I  030E                      869           BR    R14        AND RETURN TO CALLER.                          LSU08680
                                    870  *                                                                         LSU08690
          0000 05CC:I               871  ASC.UNIT EQU   *                                                        LSU08700
0005CC:I  0878                      872           LR    R7,R8      GET UNITS POSITION.                            LSU08710
0005CE:I  047A                      873           NR    R7,R10     :                                              LSU08720
0005D0:I  0B79                      874           SR    R7,R9      :                                              LSU08730
0005D2:I  2701                      875           SIS   R0,1       DECREMENT COUNT.                               LSU08740
*0005D4:I 211E       =0005F0:I      876           BM    END.CONV   IF MINUS, UNITS ONLY.                          LSU08750
0005D6:I  9468                      877           EXBR  R6,R8      GET TENS POSITION.                             LSU08760
0005D8:I  046A                      878           NR    R6,R10     :                                              LSU08770
0005DA:I  0B69                      879           SR    R6,R9      :                                              LSU08780
0005DC:I  0C65                      880           MHR   R6,R5      MULTIPLY IT BY 10.                             LSU08790
0005DE:I  0A76                      881           AR    R7,R6      ADD TO RESULT.                                 LSU08800
0005E0:I  2701                      882           SIS   R0,1       DECREMENT COUNT.                               LSU08810
*0005E2:I 2117       =0005F0:I      883           BM    END.CONV   IF MINUS, NO HUNDREDS.                         LSU08820
0005E4:I  3468                      884           EXBR  R6,R8      GET HUNDREDS POSITION.                         LSU08830
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

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0005E6:I     046A                      885           NR    R6,R10          :                                  LSU08840
0005E8:I     0B69                      886           SR    R6,R9           :                                  LSU08850
0005EA:I     0C65                      887           MHR   R6,R5           MULTIPLY IT BY 100.                LSU08860
0005EC:I     0C65                      888           MHR   R6,R5           :                                  LSU08870
0005EE:I     0A76                      889           AR    R7,R6           ADD TO RESULT.                     LSU08880
*0005F0:I                              890           B     END.CONV        CONVERSION DONE.                   LSU08890
                                       891  *                                                                LSU08900
             0000 05F0:I               892  END.CONV EQU   *                                                  LSU08910
0005F0:I     C570 0100                 893           CLHI  R7,256          IS NUMBER <= 255?                  LSU08920
0005F4:I     4380 FA10 =000008:I       894           BNL   LODRSTRT        NO, THEN ERROR - RESTART.          LSU08930
0005F8:I     03CE                      895           BR    R14             RETURN TO CALLER.                  LSU08940
```

LSU LOADER / SEGMENT 2 (RELOCATABLE)

```
                                    897  *                                   TEST MEMORY.                                LSU08960
          0000 05FA:I               898  MEM.TEST EQU   *                     ENTER WITH R13 = START ADDRESS.             LSU08970
                                    899  *                                                 R02 = END ADDRESS.            LSU08980
                                    900  *                                                                               LSU08990
                                    901  * WRITE ADDRESSES TO MEMORY.                                                    LSU09000
                                    902  *                                                                               LSU09010
 0005FA:I     50D0 83FA =0009F8:I   903           ST    R13,STARTA          SAVE START ADDRESS.                         LSU09020
          0000 05FE:I               904  WRT.ADR  EQU   *                                                               LSU09030
 0005FE:I     50DD 0000             905           ST    R13,0(R13)          STORE ADDRESS IN ITSELF.                    LSU09040
 000602:I     05D2                  906           CLR   R13,R2              AT END YET?                                 LSU09050
*000604:I     2383       =00060A:I  907           BNL   READ.SET            YES, READ THE ADDRESSES.                    LSU09060
 000606:I     26D4                  908           AIS   R13,4               BUMP THE POINTER,                           LSU09070
*000608:I     2205       =0005FE:I  909           B     WRT.ADR             AND WRITE NEXT ADDRESS.                     LSU09080
                                    910  *                                                                               LSU09090
                                    911  * READ ADDRESSES FROM MEMORY AND COMPARE.                                      LSU09100
                                    912  *                                                                               LSU09110
          0000 060A:I               913  READ.SET EQU   *                     SET-UP FOR READS.                           LSU09120
 00060A:I     58D0 83EA =0009F8:I   914           L     R13,STARTA          GET START ADDRESS.                          LSU09130
          0000 060E:I               915  READ.ADR EQU   *                                                               LSU09140
 00060E:I     583D 0000             916           L     R3,0(R13)           RETRIEVE DATA (ADDRESS?).                   LSU09150
 000612:I     05D3                  917           CLR   R13,R3              IS IT CORRECT?                              LSU09160
 000614:I     4230 FECC =0004E4:I   918           BNE   MEM.ERR             NO, THEN ABORT NOW.                         LSU09170
 000618:I     0803                  919           LR    P0,R3               ASSURE FROM MEMORY AND NOT CACHE.           LSU09180
 00061A:I                           920           IFZ   TEST                                                            LSU09190
 00061A:I     DF7D 0003             921           XSTB  3(R13)              :                                           LSU09200
                                    922           ENDC                                                                  LSU09210
 00061E:I     05D2                  923           CLR   R13,R2              AT END YET?                                 LSU09220
*000620:I     2383       =000626:I  924           BNL   WRC.SET             YES, WRITE ADDRESS COMPLEMENTS.             LSU09230
 000622:I     26D4                  925           AIS   R13,4               NO, BUMP ADDRESS POINTER.                   LSU09240
*000624:I     2208       =00060E:I  926           B     READ.ADR            AND CHECK NEXT LOCATION.                    LSU09250
                                    927  *                                                                               LSU09260
                                    928  * WRITE ADDRESS COMPLEMENT TO MEMORY.                                          LSU09270
                                    929  *                                                                               LSU09280
          0000 0626:I               930  WRC.SET  EQU   *                     SET-UP FOR WRITE ADDRESS COMPLEMENT.        LSU09290
*000626:I     2541                  931           LI    R4,-1               GET MASK FOR COMPLEMENT.                    LSU09300
 000628:I     58D0 83CC =0009F8:I   932           L     R13,STARTA          GET START ADDRESS.                          LSU09310
          0000 062C:I               933  WRC.ADR  EQU   *                                                               LSU09320
 00062C:I     083D                  934           LR    R3,R13              GET THE ADDRESS,                            LSU09330
 00062E:I     0734                  935           XR    R3,R4               COMPLEMENT IT.                              LSU09340
 000630:I     503D 0000             936           ST    R3,0(R13)           STORE ADDRESS COMPLEMENT                    LSU09350
 000634:I     05D2                  937           CLR   R13,R2              AT END YET?                                 LSU09360
*000636:I     2383       =00063C:I  938           BNL   RDC.SET             YES, READ ADDRESS COMPLEMENTS.              LSU09370
 000638:I     26D4                  939           AIS   R13,4               NO, BUMP ADDRESS POINTER.                   LSU09380
*00063A:I     2207       =00062C:I  940           B     WRC.ADR             AND WRITE NEXT LOCATION.                    LSU09390
                                    941  *                                                                               LSU09400
                                    942  * READ ADDRESS COMPLEMENT FROM MEMORY AND COMPARE.                            LSU09410
                                    943  *                                                                               LSU09420
          0000 063C:I               944  RDC.SET  EQU   *                     SET-UP FOR READ ADDRESS COMPLEMENT.         LSU09430
 00063C:I     58D0 83B8 =0009F8:I   945           L     R13,STARTA          GET START ADDRESS.                          LSU09440
          0000 0640:I               946  RDC.ADR  EQU   *                                                               LSU09450
 000640:I     580D 0000             947           L     R0,0(R13)           RETRIEVE DATA (ADDRESS COMPLEMENT?).        LSU09460
 000644:I     0704                  948           XR    R0,R4               COMPLEMENT IT.                              LSU09470
 000646:I     050D                  949           CLR   R0,R13              IS IT CORRECT?                              LSU09480
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LSU LOADER / SEGMENT 2 (RELOCATABLE)

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000648:I  4230 FE98 =0004E4:I      950          BNE   MEM.ERR          NO, THEN ABORT NOW.                    LSU09490
00064C:I  0704                     951          XR    R0,R4            ASSURE FROM MEMORY AND NOT CACHE.      LSU09500
00064E:I                           952          IFZ   TEST                                                    LSU09510
00064E:I  DF7D 0003                953          XSTB  3(R13)           :                                      LSU09520
                                   954          ENDC                                                          LSU09530
000652:I  05D2                     955          CLR   R13,R2           AT END YET?                            LSU09540
*000654:I 2383       =00065A:I     956          BNL   PAT.MTCH         YES, TRY PATTERN MATCHING NOW.         LSU09550
000656:I  26D4                     957          AIS   R13,4            NO, BUMP ADDRESS POINTER.              LSU09560
*000658:I 220C       =000640:I     958          B     RDC.ADR          AND CHECK NEXT LOCATION.               LSU09570
                                   959  *                                                                     LSU09580
                                   960  * TEST WITH DATA PATTERNS.                                           LSU09590
                                   961  *                                                                     LSU09600
          0000 065A:I              962  PAT.MTCH EQU  *                                                       LSU09610
00065A:I  C840 0024                963          LHI   R4,36            INITIALIZE INDEX TO PATTERN TABLE.     LSU09620
          0000 065E:I              964  PAT.NEW  EQU  *                 GET NEW PATTERN.                       LSU09630
00065E:I  58D0 8396 =0009F8:I      965          L     R13,STARTA       GET START ADDRESS.                     LSU09640
000662:I  5804 8166 =0007CC:I      966          L     R0,PATTERNA(R4)  GET A PATTERN.                         LSU09650
          0000 0666:I              967  PAT.WRT  EQU  *                                                       LSU09660
000666:I  500D 0000                968          ST    R0,0(R13)        STORE THE PATTERN.                     LSU09670
00066A:I  05D2                     969          CLR   R13,R2           AT END YET?                            LSU09680
*00066C:I 2383       =000672:I     970          BNL   PAT.RDST         YES, READ THEM BACK.                   LSU09690
00066E:I  26D4                     971          AIS   R13,4            NO, BUMP ADDRESS POINTER,              LSU09700
*000670:I 2205       =000666:I     972          B     PAT.WRT          AND WRITE AT NEXT LOCATION.            LSU09710
                                   973  *                                                                     LSU09720
          0000 0672:I              974  PAT.RDST EQU  *                 SET-UP TO READ PATTERN.                LSU09730
000672:I  58D0 8382 =0009F8:I      975          L     R13,STARTA       GET START ADDRESS.                     LSU09740
          0000 0676:I              976  PAT.READ EQU  *                                                       LSU09750
000676:I  583D 0000                977          L     R3,0(R13)        RETRIEVE THE PATTERN.                  LSU09760
00067A:I  0530                     978          CLR   R3,R0            IS IT VALID?                           LSU09770
00067C:I  4230 FE64 =0004E4:I      979          BNE   MEM.ERR          NO, THEN ABORT NOW.                    LSU09780
000680:I                           980          IFZ   TEST                                                    LSU09790
000680:I  DF7D 0003                981          XSTB  3(R13)           SHUT OFF CACHE.                        LSU09800
                                   982          ENDC                                                          LSU09810
000684:I  2744                     983          SIS   R4,4             YES, DECREMENT PATTERN INDEX,          LSU09820
000686:I  05D2                     984          CLR   R13,R2           AT END YET?                            LSU09830
*000688:I 2305       =000692:I     985          BNL   PAT.CKND         YES, SEE IF ALL PATTERNS USED.         LSU09840
00068A:I  50ED 0000                986          ST    R14,0(R13)       ASSURE DATA BUS CLEAN.                 LSU09850
00068E:I  26D4                     987          AIS   R13,4            NO, BUMP ADDRESS POINTER.              LSU09860
*000690:I 220D       =000676:I     988          B     PAT.READ         AND CHECK NEXT LOCATION.               LSU09870
                                   989  *                                                                     LSU09880
          0000 0692:I              990  PAT.CKND EQU  *                                                       LSU09890
000692:I  2744                     991          SIS   R4,4             DECREMENT PATTERN INDEX.               LSU09900
000694:I  4310 FFC6 =00065E:I      992          BNM   PAT.NEW          AND LOOP UNTIL ALL PATTERNS USED.      LSU09910
000698:I  030E                     993          BR    R14              RETURN TO CALLER WHEN THRU.            LSU09920
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                                    995  * DEVICE TABLE FOR CONVERTING MNEMONICS TO ADDRESSES                    LSU09940
                                    996  *                                                                       LSU09950
000698:I                            997          IFO    *                                                       LSU09960
                                    998          DB     0                                                       LSU09970
                                    999          ENDC                                                           LSU09980
            0000 069A:I            1000  DTABLE EQU    *                                                       LSU09990
00069A:I    0085                   1001  MAG85  DC     X'85',X'40',X'00',X'F0'                                 LSU10000
00069C:I    0040
00069E:I    0000
0006A0:I    00F0
0006A2:I    00C5                   1002  MAGC5  DC     X'C5',X'41',X'00',X'F0'                                 LSU10010
0006A4:I    0041
0006A6:I    0000
0006A8:I    00F0
0006AA:I    00C6                   1003  MB5R   DC     X'C6',X'33',X'B6',X'F0'                                 LSU10020
0006AC:I    0033
0006AE:I    00B6
0006B0:I    00F0
0006B2:I    00C7                   1004  MB5F   DC     X'C7',X'32',X'B6',X'F0'                                 LSU10030
0006B4:I    0032
0006B6:I    00B6
0006B8:I    00F0
0006BA:I    00EC                   1005  MB67   DC     X'EC',X'35',X'EB',X'F0'                                 LSU10040
0006BC:I    0035
0006BE:I    00EB
0006C0:I    00F0
0006C2:I    00E6                   1006  MB256  DC     X'E6',X'36',X'E5',X'F0'                                 LSU10050
0006C4:I    0036
0006C6:I    00E5
0006C8:I    00F0
0006CA:I    00C1                   1007  FLPY   DC     X'C1',X'37',X'00',X'00'                                 LSU10060
0006CC:I    0037
0006CE:I    0000
0006D0:I    0000
0006D2:I    0000                   1008  OTHR   DC     X'0',X'0',X'0',X'0'                                     LSU10070
0006D4:I    0000
0006D6:I    0000
0006D8:I    0000
                                   1009  *                                                                       LSU10080
            0000 06DA:I            1010  ADDRTABL EQU  *                                                       LSU10090
0006DA:I    0753                   1011        DC     Z(DNUM-LODRSTRT)                                        LSU10100
0006DC:I    0759                   1012        DC     Z(CODE-LODRSTRT)                                        LSU10110
0006DE:I    075F                   1013        DC     Z(CTLR-LODRSTRT)                                        LSU10120
0006E0:I    0765                   1014        DC     Z(SLCH-LODRSTRT)                                        LSU10130
0006E2:I    076B                   1015        DC     Z(DRNO-LODRSTRT)                                        LSU10140
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                                    1017  * MESSAGES                                                    LSU10160
                                    1018  *                                                             LSU10170
0006E4:I    3332 3030 204C 5355     1019  ID        DB    C'3200 LSU LOADER R00-00',X'FF'               LSU10180
0006EC:I    204C 4F41 4445 5220
0006F4:I    5230 302D 3030 FF
                                    1020  *                                                             LSU10190
0006FB:I                            1021        IFO   *                                               LSU10200
0006FB:I    00                      1022        DB    0                                               LSU10210
                                    1023        ENDC                                                  LSU10220
0006FC:I                            1024        CNOP  4                                               LSU10230
            0000 06FC:I             1025  MENU  EQU   *                                               LSU10240
0006FC:I    4445 5653 2020 0D0A     1026        DB    C'DEVS  ',CR,LF                                 LSU10250
            0000 0704:I             1027  DEVTABLE EQU  *                                             LSU10260
000704:I    4D47 3835 2020 0D0A     1028        DB    C'MG85  ',CR,LF                                 LSU10270
00070C:I    4D47 4335 2020 0D0A     1029        DB    C'MGC5  ',CR,LF                                 LSU10280
000714:I    4453 3552 2020 0D0A     1030        DB    C'DS5R  ',CR,LF                                 LSU10290
00071C:I    4453 3546 2020 0D0A     1031        DB    C'DS5F  ',CR,LF                                 LSU10300
000724:I    4453 3637 2020 0D0A     1032        DB    C'DS67  ',CR,LF                                 LSU10310
00072C:I    4432 3536 2020 0D0A     1033        DB    C'D256  ',CR,LF                                 LSU10320
000734:I    464C 5059 2020 0D0A     1034        DB    C'FLPY  ',CR,LF                                 LSU10330
00073C:I    4F54 4852 2020 0D0A     1035  OTHER DB    C'OTHR  ',CR,LF                                 LSU10340
            0000 0744:I             1036  DEVTBLND EQU  *                                             LSU10350
000744:I    4445 5649 4345 3DFF     1037        DB    C'DEVICE=',X'FF'                                LSU10360
00074C:I                            1038        IFO   *                                               LSU10370
                                    1039        DB    0                                               LSU10380
                                    1040        ENDC                                                  LSU10390
00074C:I                            1041        CNOP  4                                               LSU10400
            0000 074C:I             1042  VOLFIL  EQU   *                                             LSU10410
00074C:I    564F 4C3D 5858 5858     1043        DB    C'VOL=XXXX,FILE=',X'FF'                         LSU10420
000754:I    2C46 494C 453D FF
00075B:I    4445 5623 3DFF          1044  DNUM  DB    C'DEV#=',X'FF'                                  LSU10430
000761:I    434F 4445 3DFF          1045  CODE  DB    C'CODE=',X'FF'                                  LSU10440
000767:I    4354 4C52 3DFF          1046  CTLR  DB    C'CTLR=',X'FF'                                  LSU10450
00076D:I    534C 4348 3DFF          1047  SLCH  DB    C'SLCH=',X'FF'                                  LSU10460
000773:I    4452 5623 3DFF          1048  DRNO  DB    C'DRV#=',X'FF'                                  LSU10470
                                    1049  *                                                           LSU10480
            0000 0779:I             1050  FMKS  EQU   *                                               LSU10490
000779:I    4649 4C45 4D41 524B     1051        DB    C'FILEMARKS=',X'FF'                             LSU10500
000781:I    533D FF
                                    1052  *                                                           LSU10510
000784:I                            1053        IFO   *                                               LSU10520
                                    1054        DB    0                                               LSU10530
                                    1055        ENDC                                                  LSU10540
000784:I                            1056        CNOP  4                                               LSU10550
000784:I    494F 4552 524F 5220     1057  MSG1  DB    C'IOERROR '                                     LSU10560
00078C:I    5858 5858 FF            1058  IO.TYPE DB  C'XXXX',X'FF'                                   LSU10570
000791:I    4649 4C45 204E 4F54     1059  MSG3  DB    C'FILE NOT FOUND',X'FF'                         LSU10580
000799:I    2046 4F55 4E44 FF
0007A0:I                            1060        IFE   *                                               LSU10590
0007A0:I    00                      1061        DB    0                                               LSU10600
                                    1062        ENDC                                                  LSU10610
0007A1:I    4D45 4D54 5354 2045     1063  MSG6  DB    C'MEMTST ERR '                                  LSU10620
0007A9:I    5252 20
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0007AC:I     5858 5959 5A5A FF        1064  MFAD     DB    C'XXYYZZ',X'FF'                                    LSU10630
                                      1065  *                                                                LSU10640
0007B3:I                              1066            IFZ   TEST                                             LSU10650
0007B3:I     EE                       1067  COM2     DB    X'EE'              PASLA, 8-BIT, HI SPD, 2 STOP, EVEN  LSU10660
                                      1068            ELSE                                                   LSU10670
                                      1069  COM2     DB    X'38'              PASLA, 8-BIT, LO SPD, 2 STOP, NO PAR LSU10680
                                      1070            ENDC                                                   LSU10690
0007B4:I     A3                       1071  MTSKIP   DB    X'A3'              SKIP FILEMARK (MAG TAPE).           LSU10700
0007B5:I     A0                       1072  MTCLEAR  DB    X'A0'              CLEAR CONTROL UNIT (MAG TAPE).      LSU10710
0007B6:I     A1                       1073  MTREAD   DB    X'A1'              READ COMMAND (MAG TAPE).            LSU10720
0007B7:I     B8                       1074  MTREWD   DB    X'B8'              REWIND COMMAND (MAG TAPE).          LSU10730
0007B8:I     48                       1075  SHCLEAR  DB    X'48'              SELCH CLEAR COMMAND.                LSU10740
0007B9:I     70                       1076  SHGORD   DB    X'70'              SELCH READ/GO COMMAND               LSU10750
             0000 07B8:I              1077  CTRESET  EQU   SHCLEAR           CONTROLLER RESET COMMAND            LSU10760
0007BA:I     C1                       1078  CTREAD   DB    X'C1'                                                  LSU10770
                                      1079  * DISC COMMANDS                                                    LSU10780
0007BB:I     C2                       1080  D1SEEK   DB    X'C2'                                                  LSU10790
             0000 07BB:I              1081  D2SEEK   EQU   D1SEEK                                                LSU10800
0007BC:I     C8                       1082  D2RATTN  DB    X'C8'                                                  LSU10810
0007BD:I     C4                       1083  D2RHEAD  DB    X'C4'                                                  LSU10820
0007BE:I     D0                       1084  D2SETCYL DB    X'D0'                                                  LSU10830
0007BF:I     E0                       1085  D2SETHED DB    X'E0'                                                  LSU10840
0007C0:I                              1086            IFO   *                                                  LSU10850
                                      1087            DB    0                                                  LSU10860
                                      1088            ENDC                                                   LSU10870
                                      1089  *                                                                LSU10880
0007C0:I     0030                     1090  SECCYL   DC    H'48'              <= 10                               LSU10890
0007C2:I     0140                     1091            DC    H'320'             67                                  LSU10900
0007C4:I     04C0                     1092            DC    H'1216'            256                                 LSU10910
                                      1093  *                                                                LSU10920
0007C6:I     0018                     1094  SECTRK   DC    H'24'              <= 10                               LSU10930
0007C8:I     0040                     1095            DC    H'64'              67                                  LSU10940
0007CA:I     0040                     1096            DC    H'64'              256                                 LSU10950
                                      1097  *                                                                LSU10960
0007CC:I                              1098            CNOP  4                                                  LSU10970
0007CC:I     0000 0000                1099  PATTERNA DCY   0,11111111,33333333,77777777                       LSU10980
0007D0:I     1111 1111
0007D4:I     3333 3333
0007D8:I     7777 7777
0007DC:I     FFFF 0000                1100            DCY   FFFF0000,FFFF,F000F000,FF00FF00                  LSU10990
0007F0:I     0000 FFFF
0007E4:I     F000 F000
0007E8:I     FF00 FF00
0007EC:I     FFF0 FFF0                1101            DCY   FFF0FFF0,FFFFFFFF                                LSU11000
0007F0:I     FFFF FFFF
                                      1102  *                                                                LSU11010
             0000 07EC                1103  LENGTH   EQU   *-LODRSTRT                                         LSU11020
0007F4:I                              1104            CNOP  4                                                  LSU11030
             0000 07F4:I              1105  VDBUF    EQU   *                                                  LSU11040
             0000 08F3:I              1106  VDBUFE   EQU   VDBUF+255                                          LSU11050
             0000 07F4:I              1107  VD.VOL   EQU   VDBUF                                              LSU11060
             0000 07F8:I              1108  VD.ATRB  EQU   VD.VOL+4                                           LSU11070
             0000 07FC:I              1109  VD.FDP   EQU   VD.ATRB+4                                          LSU11080
```

LSU LOADER / SEGMENT 2 (RELOCATABLE)

```
0000 0800:I              1110  VD.OSP    EQU   VD.FDP+4                    LSU11090
0000 0804:I              1111  VD.OSS    EQU   VD.OSP+4                    LSU11100
0000 0808:I              1112  VD.MAP    EQU   VD.OSS+4                    LSU11110
0000 08F4:I              1113  DIRSAVE   EQU   VDBUFE+1                    LSU11120
0000 08F8:I              1114  LIBBUFF   EQU   DIRSAVE+4                   LSU11130
0000 09F7:I              1115  LIBBUFFE  EQU   LIBBUFF+255                 LSU11140
0000 09F8:I              1116  STARTA    EQU   LIBBUFFE+1                  LSU11150
0000 09FC:I              1117  RSAVE     EQU   STARTA+4                    LSU11160
0000 0A3C:I              1118  TBNTRY    EQU   RSAVE+64                    LSU11170
0000 0A40:I              1119  TPOFF     EQU   TBNTRY+4                    LSU11180
0000 0A44:I              1120  SWITCH    EQU   TPOFF+4                     LSU11190
0000 0A48:I              1121  OS.END    EQU   SWITCH+4                    LSU11200
0000 0A4C:I              1122  NUM.LIBS  EQU   OS.END+4                    LSU11210
0000 0A50:I              1123  ENDLODR   EQU   NUM.LIBS+4                  LSU11220
0000 0A54:I              1124  FILENAME  EQU   ENDLODR+4                   LSU11230
0000 0A5C:I              1125  EXT       EQU   FILENAME+8                  LSU11240
0000 0A60:I              1126  LODREND   EQU   EXT+4                       LSU11250
```

SYMBOL TABLE / CROSS-REFERENCE

0007F4:I	1128	END	LSU11270

SYMBOL TABLE & CROSS REFERENCE LIST

ASSEMBLED BY CAL/32 03-338R00-00

START OPTIONS: CROSS SQUEZ ERS

NO CAL ERRORS
NO CAL WARNINGS
5 PASSES

TABLE SPACE USED : 8K DISC SECTORS : 0

ABSTOP	0000 0000												
ACT.END	0000 0262:I	450	454*										
ADC	0000 0004												
ADDRTABL	0000 06DA:I	231	1010*										
ADSELCH	0000 046C:I	346	651	690*									
AMAGTE	0000 0174:I	353	357	359*									
APF.EXEC	0000 0001	110*											
APF.READ	0000 0004	110*											
APF.WRIT	0000 0002	110*											
ASC.HEX	0000 05BA:I	313	455	862*									
ASC.UNIT	0000 05CC:I	867	871*										
BINDV	0000 0078	113*											
BMP.ITEM	0000 00BC:I	253	265	269	271	273*							
BSY	0000 0008	117*	383	604	641	669	695	717	802	806	815		
CALC.SIZ	0000 02F8:I	506	514*										
CHK.ITEM	0000 0080:I	239	245*										
CK.DISC	0000 01D4:I	291	396*										
CK.DISC1	0000 01DE:I	398	402*										
CK.ENTRY	0000 0284:I	468*	484										
CK.NAME	0000 002E:I	206*	211										
CNFG	0000 04D2:I	380	566	745*									
CODE	0000 0761:I	1012	1045*										
COM2	0000 07B3:I	192	1067*										
COMN1	0000 0426:I	653	658*										
COMN2	0000 042A:I	656	661*										
CR	0000 000D	115*	784	821	1026	1028	1029	1030	1031	1032	1033	1034	1035
CTLR	0000 0767:I	1013	1046*										
CTREAD	0000 07BA:I	662	1078*										
CTRESET	0000 07B8:I	582	1077*										
D1SEEK	0000 07BB:I	597	1080*	1081									
D2RATTN	0000 07BC:I	615	1082*										
D2RHEAD	0000 07BD:I	626	1083*										
D2SEEK	0000 07BB:I	635	1081*										
D2SETCYL	0000 07BE:I	622	1084*										
D2SETHED	0000 07BF:I	631	1085*										
DEVTABLE	0000 0704:I	204	216	1027*									
DEVTBLND	0000 0744:I	205	1036*										
DIR	0000 0030	109*	109										
DIR.ACT	0000 000B	109*											
DIR.ATRB	0000 0024	109*	469										
DIR.BKSZ	0000 0025	109*											
DIR.CSEC	0000 0028	109*											
DIR.DATE	0000 0018	109*											

SYMBOL TABLE & CROSS REFERENCE LIST

```
DIR.EXT    0000 0008          109*   479
DIR.FLBA   0000 000C          109*   491   510
DIR.FNM    0000 0000          109*   475   477
DIR.INBS   0000 0026          109*
DIR.KEYS   0000 0014          109*
DIR.LLBA   0000 0010          109*   511
DIR.LRCL   0000 0016          109*
DIR.LUSE   0000 001C          109*
DIR.PSWD   0000 002C          109*
DIR.PVOL   0000 002C          109*
DIR.RCNT   0000 0022          109*
DIR.RKEY   0000 0015          109*
DIR.RSAS   0000 00F4          109*
DIR.WCNT   0000 0020          109*
DIR.WKEY   0000 0014          109*
DIRA.ACB   0000 0003          109*
DIRA.ACM   0000 0010          109*   470
DIRA.ALB   0000 0007          109*
DIRA.ALM   0000 0001          109*
DIRA.FTM   0000 00E0          109*
DIRA.UPB   0000 0006          109*
DIRA.UPM   0000 0002          109*
DIRSAVE    0000 08F4:I        495    509   1113*  1114
DISC.OS    0000 02E8:I        502    508*
DKCOMMON   0000 0418:I        605    648    650*
DNUM       0000 075B:I       1011   1044*
DRNO       0000 0773:I       1015   1048*
DTABLE     0000 069A:I        256    258    285   1000*
DU         0000 04C2:I        298    300    583    589    596    613    619    692    708    711    737*
END.CODE   0000 00AA:I        259    263*
END.CONV   0000 05F0:I        876    883    890    892*
ENL.FMKS   0000 011E:I        308    312*
ENDLOOP    0000 0A50:I        529    553   1123*  1124
ERROR      0000 050A:I        735    753    769    773*
EXEC.OS    0000 0360:I        369    393    564*
EXT        0000 0A5C:I        419    421    435    456   1125*  1126
FILENAME   0000 0A54:I        418    422    474   1124*  1125
FILNTFND   0000 04BA:I        488    732*
FLP.DATA   0000 04A2:I        715*   717    720
FLP.READ   0000 048A:I        571    706*
FLP.WAIT   0000 04B4:I        723*   725
FLPY       0000 06CA:I       1007*
FMKS       0000 0779:I        304   1050*
FMKS.DON   0000 0138:I        317    324*
FOUND.NM   0000 003E:I        208    214*
GET.ACT    0000 0250:I        429    440    445*
GET.ACT1   0000 0254:I        448*   453
GET.EXT    0000 0236:I        427    434*
GET.EXT1   0000 023A:I        436*   443
GET.FILE   0000 026A:I        425    438    457    459*
GET.FLNM   0000 0218:I        423*   432
GET.FMKS   0000 0110:I        306*   311
GET.ITEM   0000 006E:I        236*   243
```

SYMBOL TABLE & CROSS REFERENCE LIST

```
GET.OS     0000 0346:I          543   546*
GETC       0000 0550:I          202   238   307   424   437   449   809*
GETC.BSY   0000 055A:I          813*  815
GETC.OK    0000 0578:I          822   826*
GETNAME    0000 0020:I          201*  203
HEX.ASC    0000 0580:I          758   762   765   834*
HEXC1      0000 0594:I          837   840   844*
ID         0000 06E4:I          197   1019*
IMPTOP     0000 07F4:I
IO.TYPE    0000 078C:I          750   1058*
IOERROR    0000 04D8:I          739   743   747   749*
LADC       0000 0002
LCE        0000 0010            110*  110
LCE.ADDR   0000 000C            110*
LCE.NAME   0000 0000            110*
LCE.SIZE   0000 0008            110*
LCE.TYPE   0000 0008            110*
LCT.COMN   0000 0000            110*
LCT.ENTR   0000 0001            110*
LENGTH     0000 07EC            142   1103*
LF         0000 000A            116*  786   1026  1028  1029  1030  1031  1032  1033  1034  1035
LIB        0000 0100            110*  110
LIB.CTOP   0000 0064            110*
LIB.DATE   0000 0050            110*
LIB.DUMN   0000 002C            110*
LIB.FW2    0000 0010            110*
LIB.FW3    0000 0014            110*
LIB.HIS    0000 003C            110*
LIB.IPRI   0000 0005            110*
LIB.IRN    0000 004A            110*
LIB.ITSW   0000 0018            110*
LIB.LKTA   0000 0007            110*
LIB.MPRI   0000 0004            110*
LIB.MXSG   0000 0044            110*
LIB.MXSP   0000 0014            110*
LIB.NASN   0000 0003            110*  110
LIB.NCOM   0000 0007            110*
LIB.NEPC   0000 004C            110*
LIB.NIOQ   0000 0060            110*
LIB.NLIB   0000 0001            110*  500
LIB.NLSG   0000 0008            110*
LIB.NLU    0000 0002            110*
LIB.NLVL   0000 0040            110*
LIB.NOVL   0000 0042            110*
LIB.NPRC   0000 003C            110*
LIB.NSEG   0000 0007            110*
LIB.ODTL   0000 0062            110*
LIB.OPT    0000 000A            110*
LIB.OPN    0000 0048            110*
LIB.OS     0000 0008            110*
LIB.OV     0000 0005            110*
LIB.PREC   0000 0006            110*
LIB.PRIV   0000 0003            110*
```

SYMBOL TABLE & CROSS REFERENCE LIST

```
LIB.PRN     0000 0024          110*
LIB.PSIZ    0000 0020          110*
LIB.RL      0000 0003          110*
LIB.RORT    0000 0010          110*
LIB.RREG    0000 0003          110*
LIB.RSIZ    0000 0100          110*
LIB.SEGN    0000 0020          110*   110    110
LIB.SEGS    0000 000C          110*   503
LIB.SEGT    0000 0000          110*
LIB.SPRC    0000 003E          110*
LIB.SSEG    0000 0009          110*
LIB.TA      0000 0001          110*
LIB.TATR    0000 0009          110*
LIB.TC      0000 0004          110*
LIB.TIME    0000 0058          110*
LIB.UTOP    0000 0068          110*
LIB.VARL    0000 006C          110*
LIB.XOPT    0000 0008          110*
LIBBUFF     0000 08F8:I        326    496    500    503   1114*  1115
LIBBUFFE    0000 09F7:I        327    497   1115*  1116
LODREND     0000 0A60:I        526    528    534    536   1126*
LODRSTRT    0000 0008:I        190*   197    199    212    234    257    304    415    526    534    535    536    543    734
                               752    768    774    789    819    860    894   1011   1012   1013   1014   1015   1103
LSE         0000 0014          110*   110
LSE.MNSZ    0000 000C          110*
LSE.MXSZ    0000 0010          110*
LSE.NAME    0000 0000          110*
LSE.PRIV    0000 000C          110*
LSE.SREG    0000 000B          110*
LSU         0000 0001            1*     4    137
LSUADDR     0000 1000          112*   140    141    142    775
MAG.READ    0000 0144:I        328    342*   345    358    364    373    569
MAG85       0000 069A:I       1001*
MAGC5       0000 06A2:I       1002*
MAGRD.OS    0000 0184:I        350    366*
MAGTAPE     0000 00E8:I        292*
MB256       0000 06C2:I       1006*
MB5F        0000 06B2:I       1004*
MB5R        0000 06AA:I       1003*
MB67        0000 06BA:I       1005*
MEM.ERR     0000 04E4:I        755*   918    950    979
MEM.IFST    0000 05FA:I        530    554    898*
MENU        0000 06FC:I        199   1025*
MFAD        0000 07AC:I        759    763    766   1064*
MOVE.LDP    0000 032C:I        537*   541
MSG         0000 0516:I        194    781*
MSG.PUT     0000 0528:I        788*   793
MSG1        0000 0784:I        752   1057*
MSG3        0000 0791:I        734   1059*
MSG6        0000 07A1:I        768   1063*
MTCLEAR     0000 07B5:I        297   1072*
MTREAD      0000 07B6:I        376   1073*
MTREWD      0000 07B7:I        381   1074*
```

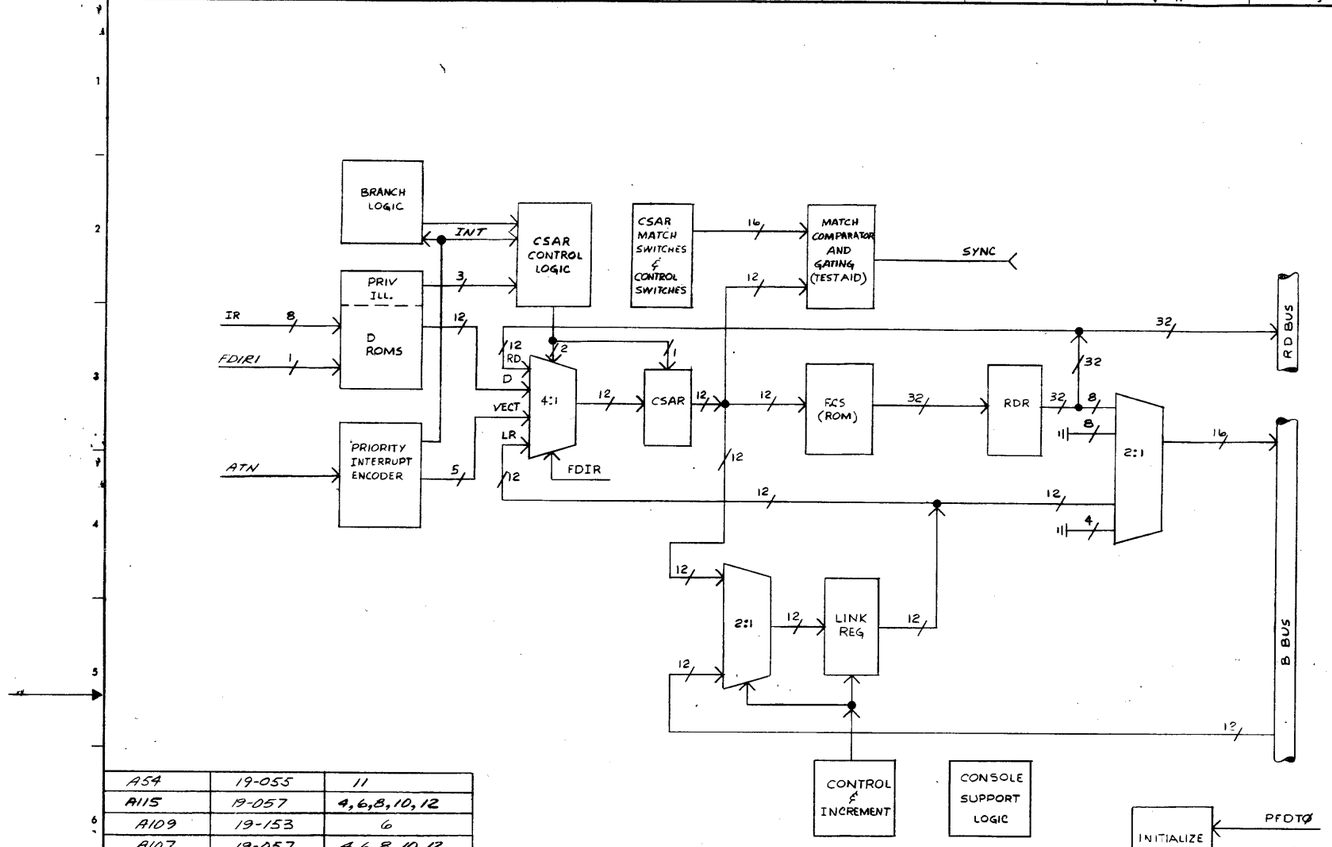
SYMBOL TABLE & CROSS REFERENCE LIST

SYMBOL TABLE & CROSS REFERENCE LIST

```
R3          0000 0003    124*  287   385   387   387   388   536   538   539   540   582   585   599   617
                         624   528   633   637   655   659   660   662   664   676   916   917   919   934
                         935   936   977   978
R4          0000 0004    125*  191   192   193   288   297   299   301   314   319   322   343   376   378
                         391   588   595   597   602   609   615   621   622   626   630   631   635   640
                         654   707   710   713   716   718   722   724   797   799   801   803   805   811
                         812   814   816   817   931   935   948   951   963   966   983   991
R5          0000 0005    126*  289   290   293   397   399   403   422   430   431   435   441   442   501
                         501   568   568   570   573   575   577   577   652   652   863   880   887   888
R6          0000 0006    127*  231   232   254   256   258   260   386   388   389   412   413   466   469
                         475   477   479   482   491   495   509   510   511   605   647   688   782   789
                         791   877   878   879   880   881   884   885   886   887   888   889
R7          0000 0007    128*  193   220   221   316   326   362   371   407   426   428   430   439   441
                         456   464   469   470   472   496   562   681   684   696   696   697   698   698
                         699   714   718   719   738   742   746   750   784   786   789   792   803   816
                         820   821   828   835   839   868   872   873   874   881   889   893
R8          0000 0008    129*  195   207   219   221   237   242   327   363   368   372   389   408   420
                         421   446   497   503   511   512   517   518   519   520   521   526   527   534
                         539   543   544   561   700   700   701   702   702   703   714   718   827   828
                         853   855   857   858   872   877   884
R9          0000 0009    130*  204   207   209   210   215   217   223   228   250   267   274   275   574
                         595   521   646   654   685   864   874   879   886
RDC.ADR     0000 0640:I  946*  958
RDC.SET     0000 063C:I  938   944*
RDKLOOP1    0000 03A0:I  594*  606
RDKLOOP2    0000 03CE:I  614*  647
RDSK2       0000 03BC:I  578   608*
READ        0000 0364:I  410   465   498   563   567*
READ.ADR    0000 060E:I  915*  926
READ.DIR    0000 0276:I  463*  486
READ.MAG    0000 01A0:I  349   354   367   375*
READ.SET    0000 060A:I  907   913*
RSAVE       0000 09FC:I  302   314   325   411   460   525   542   547   560   1117* 1118
SECCYL      0000 07C0:I  573   1090*
SECTRK      0000 07C6:I  575   1094*
SET.IO      0000 00C6:I  226   277   282*
SHCLEAR     0000 07B8:I  384   670   691   1075* 1077
SHGORD      0000 07B9:I  377   663   1076*
SKIP.FM     0000 0126:I  315*  323
SLC.WAIT    0000 0474:I  693*  695
SLCH        0000 076D:I  1014  1047*
STARTA      0000 09F8:I  903   914   932   945   965   975   1116* 1117
STR.ITEM    0000 0088:I  247   249*
SWITCH      0000 0A44:I  295   347   361   505   1120* 1121
TBNTRY      0000 0A3C:I  223   283   1118* 1119
TEST        0000 0000      2*  548   555   777   920   952   980   1066
TPOFF       0000 0A40:I  1119* 1120
UNRE        0000 04CA:I  370   394   603   611   643   678   741*
VD.ATRB     0000 07F8:I  1108* 1109
VD.FDP      0000 07FC:I  461   1109* 1110
VD.MAP      0000 0808:I  1112*
VD.OSP      0000 0800:I  1110* 1111
VD.OSS      0000 0804:I  1111* 1112
```

SYMBOL TABLE & CROSS REFERENCE LIST

VD.READ	0000 01E0:I	400	404	406*				
VD.VOL	0000 07F4:I	412	1107*	1108				
VDBUF	0000 07F4:I	407	464	466	485	1105*	1106	1107
VDBUFE	0000 08F3:I	408	1106*	1113				
VECTOR	0000 004B:I	219	222*					
VOLFIL	0000 074C:I	413	415	1042*				
WAIT.FM	0000 012A:I	318*	321					
WAIT.MAG	0000 01B2:I	381*	383					
WAIT10	0000 038C:I	584*	586					
WAIT11	0000 03AA:I	598*	600					
WAIT12	0000 03AE:I	601*	604					
WAIT15	0000 0390:I	587*	591					
WAIT21	0000 03D2:I	616*	620					
WAIT22	0000 03E4:I	623*	625					
WAIT23	0000 03EC:I	627*	629					
WAIT24	0000 03F6:I	632*	634					
WAIT25	0000 03FE:I	636*	638					
WAIT26	0000 0402:I	639*	641					
WAIT31	0000 043C:I	667*	669					
WAIT32	0000 044C:I	675*	677					
WRC.ADR	0000 062C:I	933*	940					
WRC.SET	0000 0626:I	924	930*					
WRT.ADR	0000 05FE:I	904*	909					
X.CONV	0000 05A6:I	240	852*					
X.CONV1	0000 05AE:I	854	856*					



A54	19-055	11
A115	19-057	4,6,8,10,12
A109	19-153	6
A107	19-057	4,6,8,10,12
A91	19-124	6
A90	19-055	3,11
A85	19-235	8,11
A84	19-055	8,11
A81	19-125	3,11
A80	19-236	11
A78	19-058	6,12
A77	19-058	8
A74	19-058	12
A73	19-057	8
A65	19-059	12
A61	19-057	2,4,10
A56	19-057	4
A55	19-234	1,4,10
A48	19-241	6
A46	19-063	9
A45	19-058	6,12
A35	19-236	8

A2	19-057	2,12
LOCATION	TYPE	OUTPUT

TABLE OF SPARES

REVISION	03	11	01	02	01	02								
SHEET	1	2	3	4	5	6	7	8	9	10				

* MNEMONIC IS PRESENT ON BACKPANEL BUT NOT USED ON CPU-A BOARD.

GND	5	N.C.	2
EXTRAPØ	2	N.C.	10
SYNO	1	N.C.	10
GND	4	E	7
GND	6	A	6
GND	C	G	6
GND	4	N.C.	2

MNEMONIC	FROM T.P.	TO T.P.	SHEET
TEST POINT TABLE			

USED IN MANUAL 47-022

CONN	TERM. NO.	CABLE CONNECTOR MAP ROW 2	CABLE CONNECTOR MAP ROW 1	BACK PANEL MAP ROW 1	BACK PANEL MAP ROW 2	TERM. NO.	CONN
5	16			P5	P5	41	1
	15			GND	GND	40	
	14			SR1Ø	SRØØ	39	
	13			MBYØ	SHØ	38	
	12			DIVØ	ULSRØ	37	
	11			GRD1Ø1	ENB3Ø	36	
	10			GRDØ91	GRD111	35	
	09			RD221	RD231	34	
	08			RD201	RD211	33	
	07			RD191	RD191	32	
	06			RD171	RD181	31	
	05			RD271	RD271	30	
	04			RD251	RD261	29	
	03			RD241	RD121	28	
	02			RD141	RD131	27	
	01			RD151	RD101	26	
	00			RDØØ1	RDØ11	25	
				RDØ21	RDØ31	24	
				RDØ41	RDØ51	23	
	24			RD301	RD311	22	
	23			GND	GND	21	
	22			RDØ61	RDØØ1	20	
	21			RD111	RDØ21	19	
	20			RD281	RD291	18	
	19			PSW201	PSW251	17	
	18			PSW261	PSW271	16	
	17			PSW131	PSW231	15	
	16			PSW171	PSW181	14	
	15			AENHØ	AENLØ	13	
	14			IRØ7Ø	IRØ6Ø	12	
	13			IRØ5Ø	IRØ4Ø	11	
	12			IRØ3Ø	IRØ2Ø	10	
	11			IRØ1Ø	IRØØØ	09	
	10			YDØ81	YDØ91	08	
	09			YD101	YD111	07	
	08			FLR281	FLR291	06	
	07			FLR301	FLR311	05	
	06			GFLR251	LFLRØ	04	
	05			FPPFLTØ	BSTKSØ	03	
	04			SMINTØ	JAMCIØ	02	
	03			GND	GND	01	
	02			P5	GND	00	
	01						
	00						
				P5	GND	41	
				GND	GND	40	
				CLKIA	CLKPSWØ	39	
				CLKCCØ	SCLKI	38	
				GND	GND	37	
	24	GND	GND	GDIRØ	SVØ	36	
	23	CSAR3ØØ	CSAR31Ø	DPSTOPØ *	DSTOPØ	35	
	22	CSAR28Ø	CSAR29Ø	FPPFØ	RSTOPØ	34	
	21	GND	CSAR29Ø	CLØ7Ø	UNNLDØ	33	
	20	CSAR26Ø	CSAR27Ø	FFDTØ	WAITI	32	
	19	CSAR24Ø		SFTENØ	DFTENØ	31	
	18	CSAR22Ø	CSAR25Ø	ATNØØØ	ATNØ1Ø	30	
	17	GND	CSAR23Ø	ATNØ2Ø	ATNØ3Ø	29	
	16	CSAR2ØØ	CSAR21Ø	GND	GND	28	
	15	GND	GND	BØØ1 *	BØ11 *	27	
	14			BØ21 *	BØ31 *	26	
	13			BØ41 *	BØ51 *	25	
	12			BØ61 *	BØ71 *	24	
	11			BØ81 *	BØ91 *	23	
	10			B101 *	B111 *	22	
	09			B121 *	B131 *	21	
	08			B141 *	B151 *	20	
	07			B161	B171	19	
	06			B181	B191	18	
	05			B201	B211	17	
	04			B221	B231	16	
	03		P5	B241	B251	15	
	02			B261	B271	14	
	01			B281	B291	13	
	00			B301	B311	12	
				GND	GND	11	
				HWØ	RCATNØ	10	
	16			SCATNØ	TRAPØ	09	
	15			SINGLØ	NVMØ	08	
	14			MAT Ø	ECLRØ	07	
	13			DEXTØ		06	
	12			FNCEØ	SCLROB	05	
	11			DEXBØ	ALGNØ	04	
	10			GMVFØ	DISAØ	03	
	09			PSU	DISBØ	02	
	08			GND	GND	01	
2	07			P5	GND	00	0
	06						
	05						
	04						
	03						
	02						
	01						
	00						

ON BACK PANEL MAP MNEMONICS MARKED WITH AN * WERE NOT SPEC. NVMØ AT PDS 20B-D WAS NOT SPEC. IN TABLE OF SPARES A115, WAS NOT SPEC. SHEET 6 & 9 WERE SPEC AS RDØ. IN "BOARDS AGREEING" BLOCK REV LEVEL WAS RDØ.

VR	BNL	2CB 4844	M	9-11-81	R01	

RELEASED FOR PRODUCTION
DEV. ENG. _____ DATE 6-81

REVISED SHTS. 1 & 9

VT	WI	4973	M	3-22-82	R02	X

SPARE GATE LIST, ADDED A54-11 & DELETED A74-06 & A35-03. REVISED SHTS. 1, 3, 5, 6 & 8.

KR	WI	5114	MS	7-23-82	E03	

35-816	R04
BOARD	REV. LEVEL

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

NAME	TITLE	DATE
V. PERRI	DRAFT	11-6-81
E. GREENSTEIN	SYS. TEST	11-6-81
R. ZERO	"	11-6-81
M. MANSIONE	ENGR	11-6-81
R. A. BARKER	QC	11-6-81
D. COOKDA	MGR	11-6-81

SCALE: NONE

TITLE: FUNCTIONAL SCHEMATIC CPU-A

SIZE: D | 35-816 | R03

REVISIONS

B A
0 0 LINK
0 1 RD
1 0 INT
1 1 DD

A22 19-116 4 TO 1 MUX — INPUT 2 / INPUT 1 / STB 2 / STB 1 / SEL A / SEL B / 2Y / 1Y
A23 19-116
A13 19-116
A14 19-116
A4 19-116
A5 19-116

LR21! RD16! DD20! GOTO1A VSELA0 VSELB0 LR22! RD17! DD21!
LR22! RD18! DD22! LR23! RD19! DD23!
LR24! RD20! DD24 GOTO1 LR25! RD21! DD25!
LR26! RD22! DD26!
LR27! RD23! RPPLT! DD27!
LR28! RD24! VECT0! DD28!
LR29! RD25! VECT1! DD29!
LR30! RD26!A VECT2! DD30!
LR31! RD27!A VECT3! DD31!

9M3 SCLR0D
7D2 RCLK1
3E4 LDCSAR0
TP3 ENCSAR!
TP5
R5
R8 1K

A21 A12 A3 — 19-135 4 BIT CNTR — INPUTS D C B A — OUTPUTS D C B A — LD ENP ENT CLK CLR CL
N.C.

R54 1K R5

C1-C9 15uF, 25V
C10-C58, C63-C66, C68, C70-C83, C88 .1uf

A125 19-240 LINE DVR/RCVR — N.C. N.C. N.C. N.C.
A124 19-240 LINE DVR/RCVR
A124 19-240 LINE DVR/RCVR

A20 19-057 SG
A11 19-057 SG
A54 19-055 SG
A2 19-057 SG

CSAR20! CSAR21! CSAR22! CSAR23! CSAR24! CSAR25! CSAR26! CSAR27! CSAR28! CSAR29! CSAR30! CSAR31!

482,3L3 216-3 1007 481,3L3 116-3 1006 482,3K3 278-3 1006 482,3K3 117-3 1005
482,3L3 279-3 1005 482,3L3 118-3 1004 483,3K3 220-3 1004 483,3K3 120-3 1004
483,3N3 222-3 1003 483,3N3 121-3 1002 483,3N3 223-3 1002 483,3N3 122-3 1002

SCLR0D 9M3
RDCLE0 5A1

NOTES
1. X'007' - ILLEGAL
X'0004' - POWER UP

DRAFTER	V. PERRI
DATE	4-27-81
TITLE	CPU-A CONTROL STORE ADDRESS REGISTER (CSAR)
TASK	03173
DWG	35-816 008
SHT	2 - 10

IBRUNING 44-131-4079-2

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
AREA E4, DELETED 6M4 FROM BRANCH1.				
KR 141	S114	MS	7-23-82	R01

5F4 RD@6@
6R3 TBRCH1
5N4 RD15@
A35 19-236 SA
6R2 TBRCH@
5G5 RD@61
5F4,B4 RD@5@
5E4 RD@41
B9 MAT MPE@
E8 FDIR1
A44 19-062 SG
08 VSELA@ 2BE
7G9 FLTILL1
11S-1 PSW13I
A20 19-057 SG
A36 19-055 SG
6N5 FPP1
E8 FDIR1
7F9 PRIV1
21S-1 PSW B3I
7F9 COMILL1
D1 FLT
D1 PRIV
D1 ILL
EXPANSION
A37 19-062 SG
5M4 RD131
INT1
A36 19-055 SG
GBRCH1
A45 19-058 SG
08 VSELB@ 2B1
5F4 RD@51
A11 19-057 SG
BRANCH1 7K6, 8B2, 7K6
BRANCH@ 6M2 7F2
5F4 RD@5@
6R3 FBRCH1
6R4 TBRCH1
A27 19-241 SN
06 LDCSAR@ 2A5
8M8 INT1
6D5 DIR@
A27 19-241 SN
05 GDIR1 2F1
5B4 RD@@1
5C4 RD@11
5C4 RD@E@
5E4 RD@31
A26 19-060 SG
A28 19-241 SN
05 GDIR1A 2B1
A88 19-057 SG
04 GDIR@ 13G-@
R9 1K P5
A46 19-063
FDIR1 F1, 7A8, 8E9, A3
7D3 RCLK@A
9M3 SCLR@D
FDIR@ 6B4, 8H7
7J4 LDLR@
A88 19-057 SG
LDLR1
A84 19-055 SG
A93 19-236 SA
5M5 RD141
7D3 RCLK@A
7D5 SCLK@A
NC
LINK
LINK INC
LOAD LINK
A92 19-062 SG
7D5 SCLK1A
7D2 SCLK1
LRCLK@
9M3 SCLR@D
CSAR2@1 2C9 B2@1 7R3
CSAR211 2D9 B211 7R4
CSAR221 2D9 B221 7R4
CSAR231 2E9 B231 7R4
CSAR241 2H9 B241 7R5
CSAR251 2H9 B251 7R5
CSAR261 2H9 B261 7R5
CSAR271 2J9 B271 7R6
CSAR281 2L9 B281 7R6
CSAR291 2M9 B291 7R7
CSAR3@1 2M9 B3@1 7R7
CSAR311 2N9 B311 7R7
A102 2TO1MUX
A110 2TO1MUX
A111 2TO1MUX
SEL 19-065 ENB
A101 4 BIT CNTR
A99 4 BIT CNTR
A100 4 BIT CNTR
19-135
INPUTS
OUTPUTS
LD CL CAR
R30 1K P5
LR2@1 LR211 LR221 LR231
LR241 LR251 LR261 LR271
LR281 LR291 LR3@1 LR311
7K3,2B1 7K4,2C1 7K4,2D1 7K4,2E1
7K5,2F1 7K5,2G1 7K5,2H1 7K5,2J1
7K6,2K1 7K7,2L1 7K7,2M1 7K7,2N1

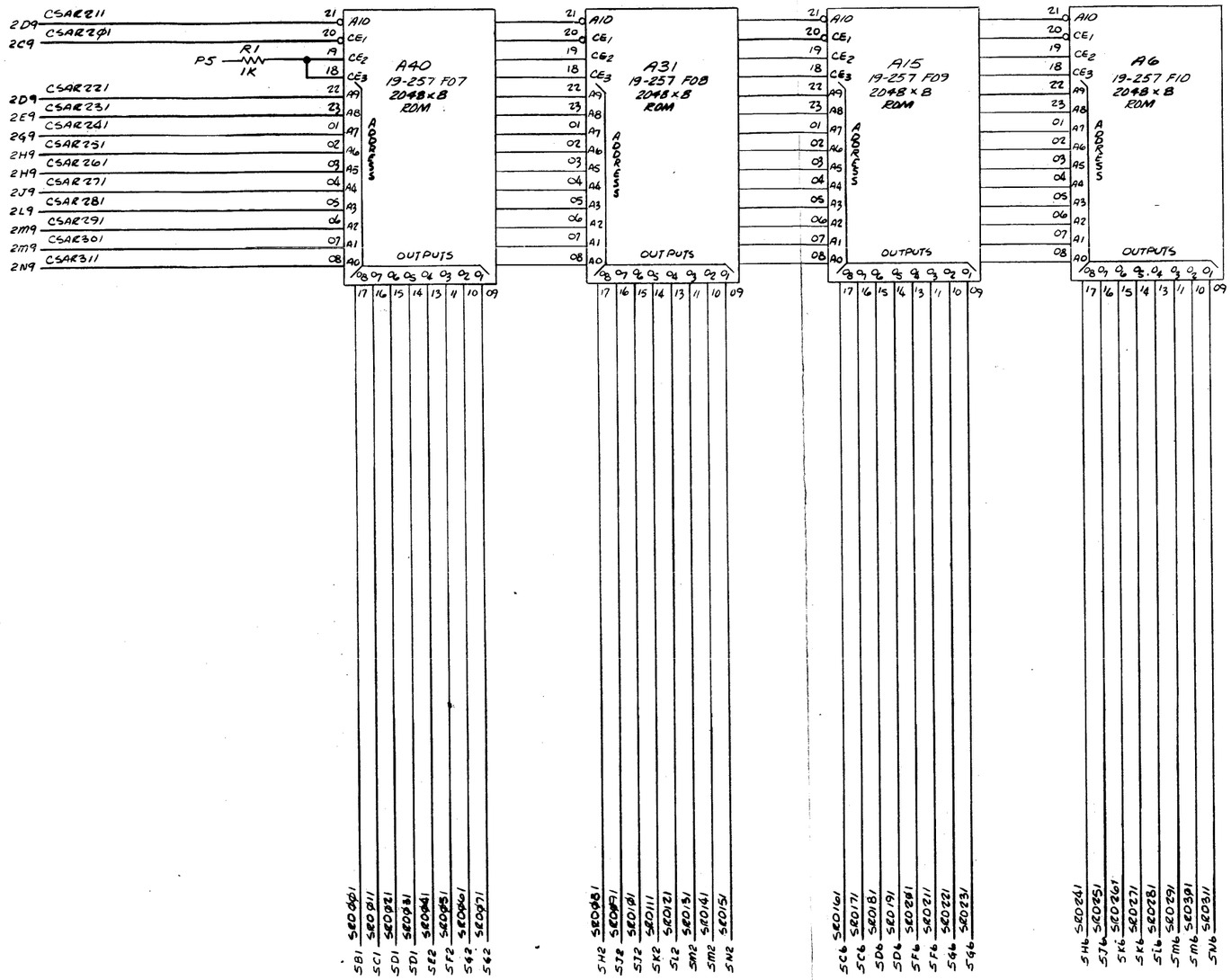
SCALE –	NAME	TITLE	DATE
TOLERANCE .XXX ± .@@@ .XX ± .@3 .X ± .@5 ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	BLUSK	DRAFT	9-29-80
		CHK	
		ENGR	

TITLE CPU-A
LINK REGISTER

DWG NO. 03179
TYPE NO. 35-816 R01 D00
SHEET 9 – 10

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



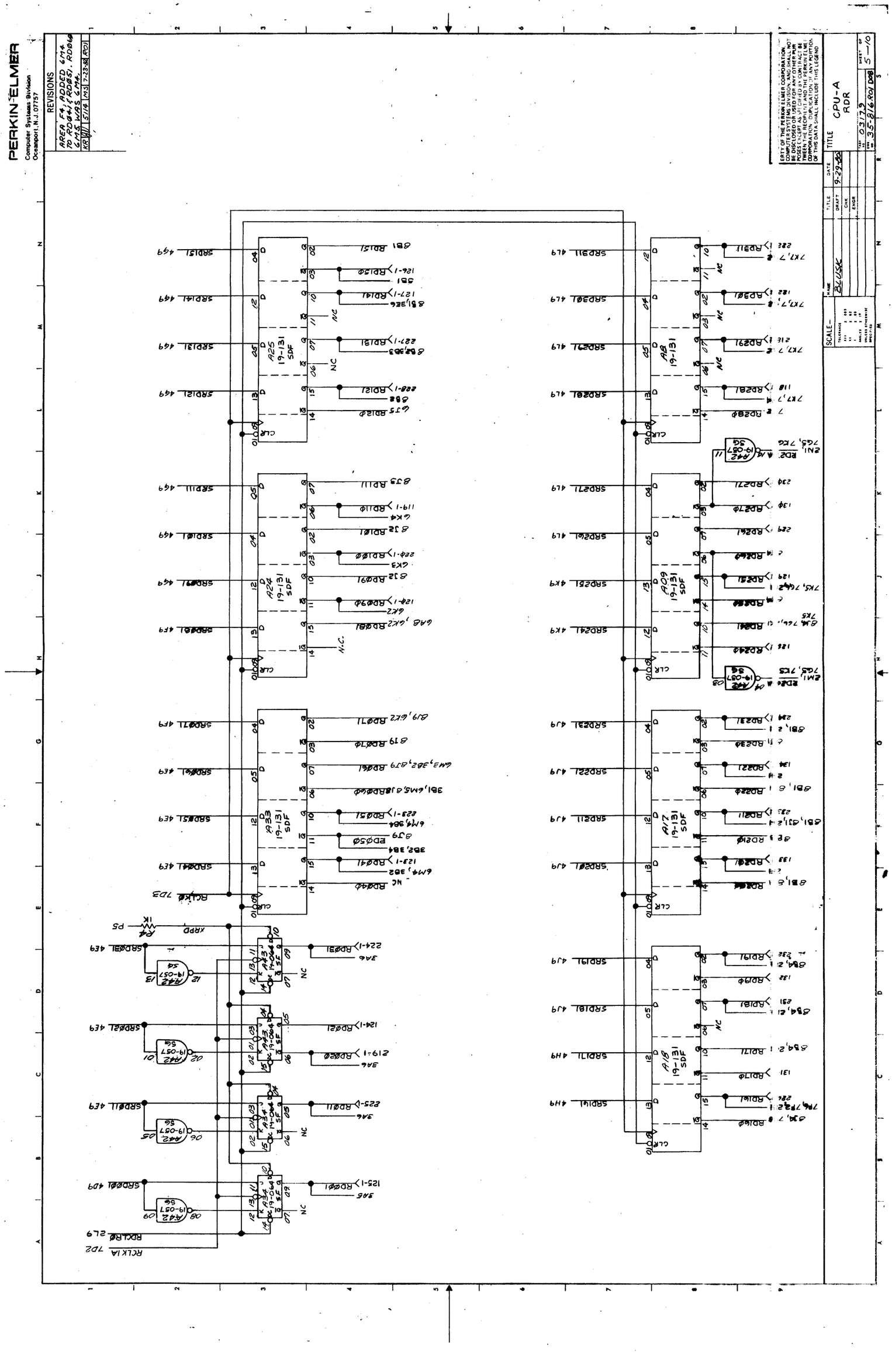
FCS
'000'X-'7FFF'X

SCALE–
TOLERANCE
XXX ± .005
.XX ± .02
.X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
BLUSK	DRAFT	9-29-80
	CHK	
	ENGR	

TITLE
CPU-A
FIXED CONTROL STORE

TASK NO. 03179
DWG NO. 35-816 DOB
SHEET OF 4–10


PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757
REVISIONS
AREA F4, ADDED 6714
TO RDA14 & RDA61, RDA66
AT LEVEL 4 ONLY
TITLE
CPU-A
RDR
DRAFT
CHK
ENGR
DATE
9-29-80
SCALE-
SHEET 5-10
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PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS					
IN AREA D6, A57 PIN 15 WAS SPEC AS MNEMONIC MVFI.					
NSR	BWL	ECO 7844	M	9-11-81	R01
AREA N4, ADDED A74-06 & A35-03. DELETED A56-11 A56-11 WAS TO A55-12					
KRAV		5114	MS	7-23-82	R02

214-1 PSWI81
8N4 FSMINTØ
9H1 FEPPØ
9H2 FPPFI
8D9
1Ø5-Ø FNCØØ
7J3 CCATNØ
7D3 BCLKØA
9M3 SCLRØD
3E8 FDIRØ
1Ø9-Ø SCATNØ
21Ø-Ø RCATNØ
1Ø3-Ø GNVFØ
11Ø-Ø HWØØ
3B5 DIRØ
GFSEPFØ 8E8
FSPPFØ 8D8
FSMPEØ N.C.
FSCATNØ 8D6
1Ø7-Ø MATØ
8D9, 8F9
E8 1Ø6-1 FLR281
8J8 INTI
SJ5 RDØ7Ø
5G5 RDØ71
5H5 RDØ61
5J5 RDIØØ
8J2 2Ø6-1 FLR291
MATI
9H1 FEPFI
E7 1Ø5-1 FLR3Ø1
SEE NOTE 2
FPPI
5K5 RDIIØ
3F1
E7 2Ø5-1 FLR311
FCATNI
5L5 RDI2Ø
1Ø8-1 YDØØ1
2Ø8-1 YDØ91
1Ø7-1 YDI01
2Ø7-1 YDIII
HWI
8J6 YDØØ1
8J6 YDØ91
8J6 YDI01
8J6 YDIII
BRANCHØ 3E4
TBRCHØ 3B2
TBRCHI 3B1
FBRCHI 3B4
GBRCHI 3C3
TRBRCHI 3B4
3B2 RDØ61
5F4 RDØ41
5F4 RDØ51
RDØ6ØA
5F4 RDØ6Ø
MSKI
9L2 XRPT
5H5 RDØ81
7D4 DCLKØ
9M3 SCLRØD
7E5 SCLKØA
138-Ø CLKCCØ
H5 FLR311
H4 FLR3Ø1
8N1 GFLR291
H1
APSW311
APSW3Ø1
APSW291
APSW281
AUX PSW

NOTES,
1. STRAP A TO G FOR COMM OPTION NOT PRESENT LEAVE OPEN FOR COMM OPTION PRESENT.
2. STRAP C TO G, FOR FLOATING POINT PROCESSOR NOT PRESENT, LEAVE OPEN FOR FPP PRESENT.

SCALE—
TOLERANCE: XXX ± .000, XX ± .02, X ± .05, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

TITLE: CPU-A CONSOLE SYNC & BRANCH CONDITIONING
TASK NO. 03179
DWG NO. 35-B16 R02D08
SHEET OF 6—10

PERKIN-ELMER
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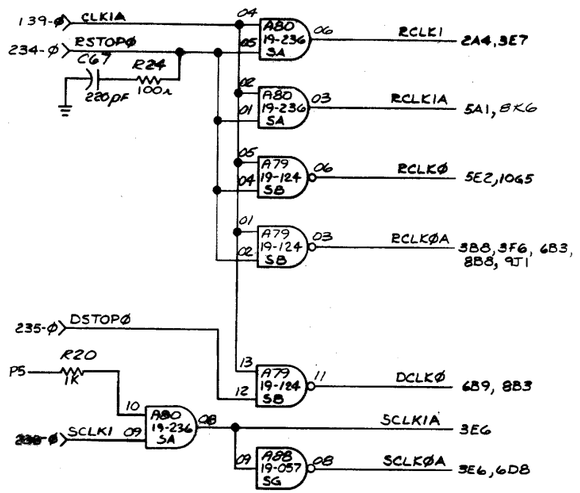
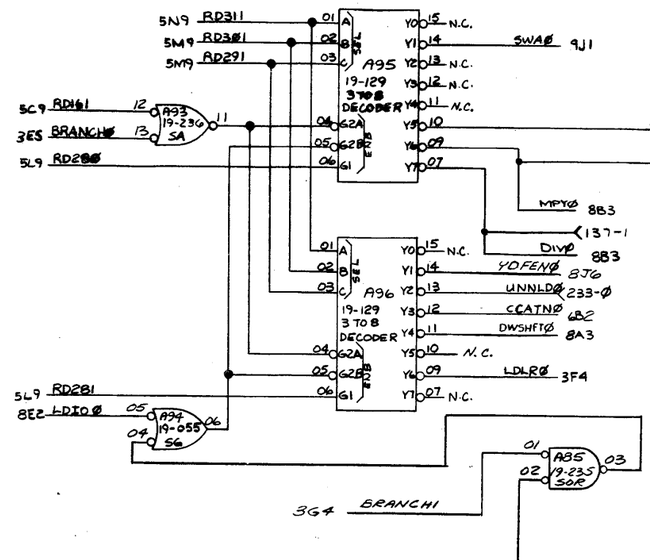
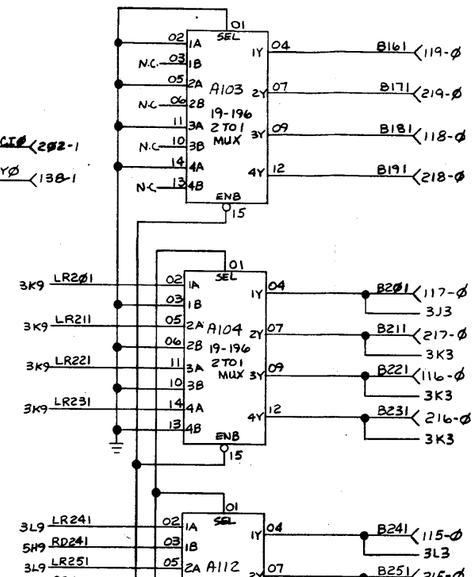
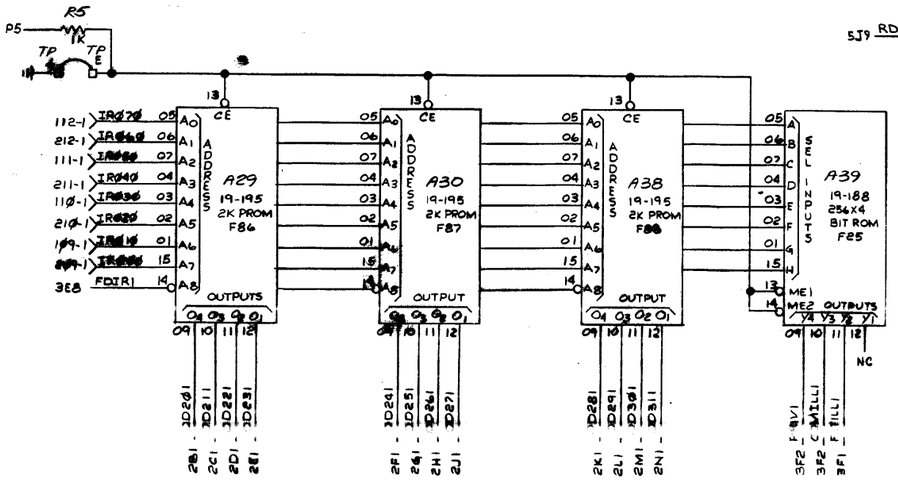
Oceanport, N.J. 07757

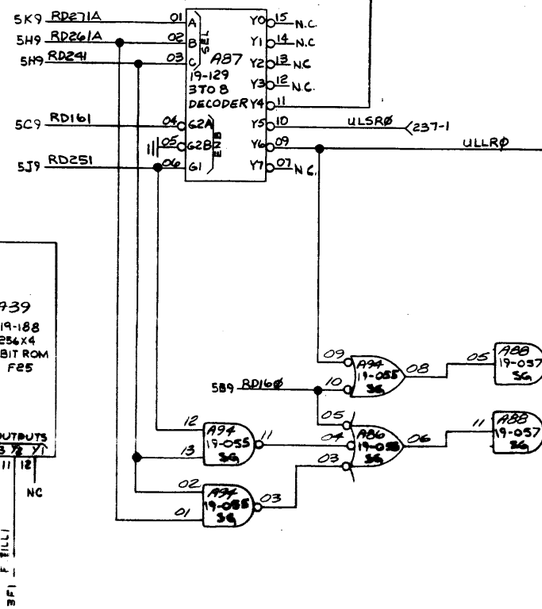
REVISIONS











SCALE –

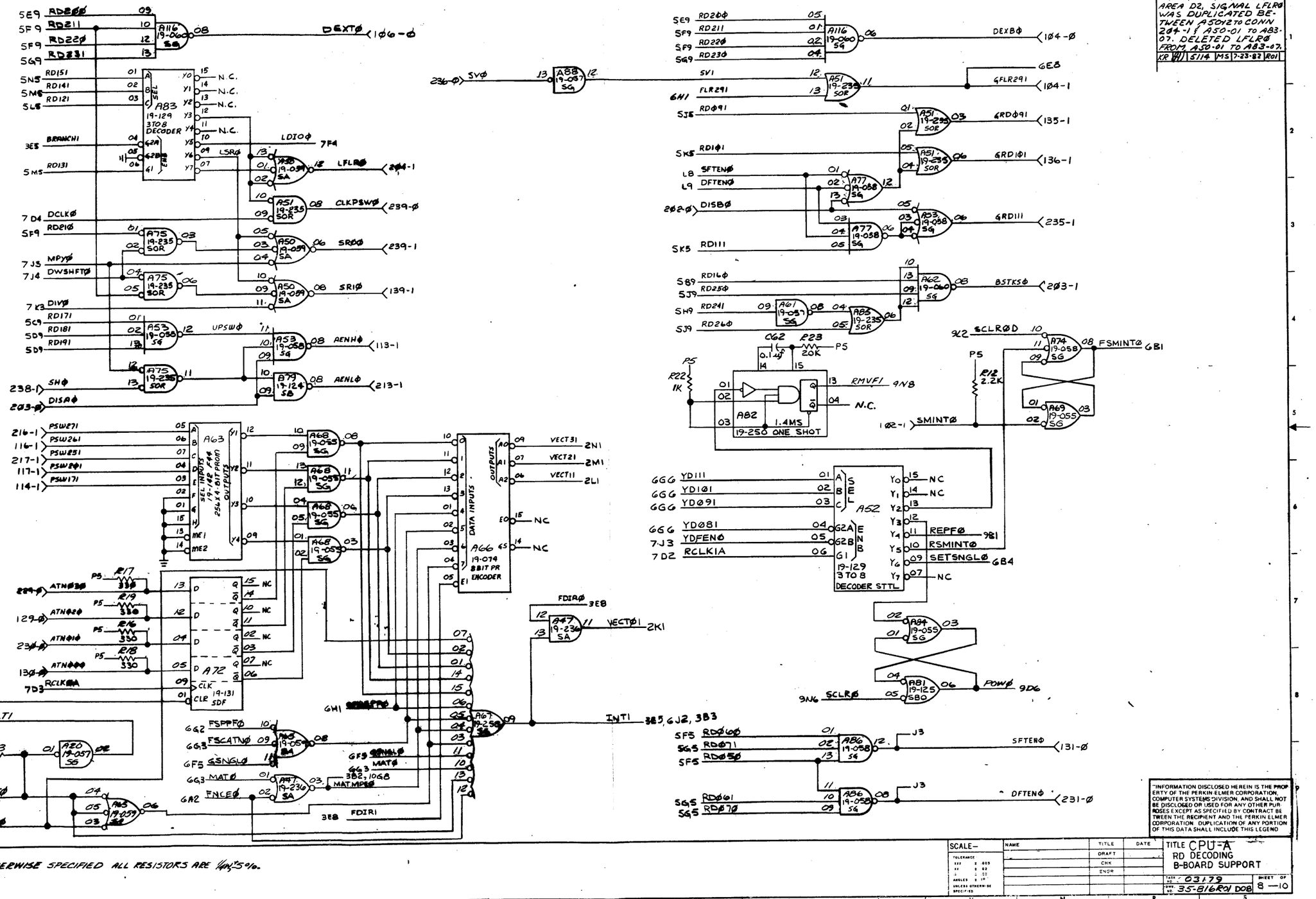
	NAME	TITLE	DATE
		DRAFT	
		CHK	
		ENGR	

TITLE
CPU-A
E-FIELD DECODE & B-BUS DRIVERS

SIZE D | DWG NO 33179 | REV
SHEET 7 OF 10
DWG NO 35-816 D08

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
AREA D2, SIGNAL LFLRØ WAS DUPLICATED BETWEEN A50-02 TO CONN 204-1 & A50-01 TO A83-07. DELETED LFLRØ FROM A50-01 TO A83-07.				
XR 181	S114	MS	7-23-82	R01

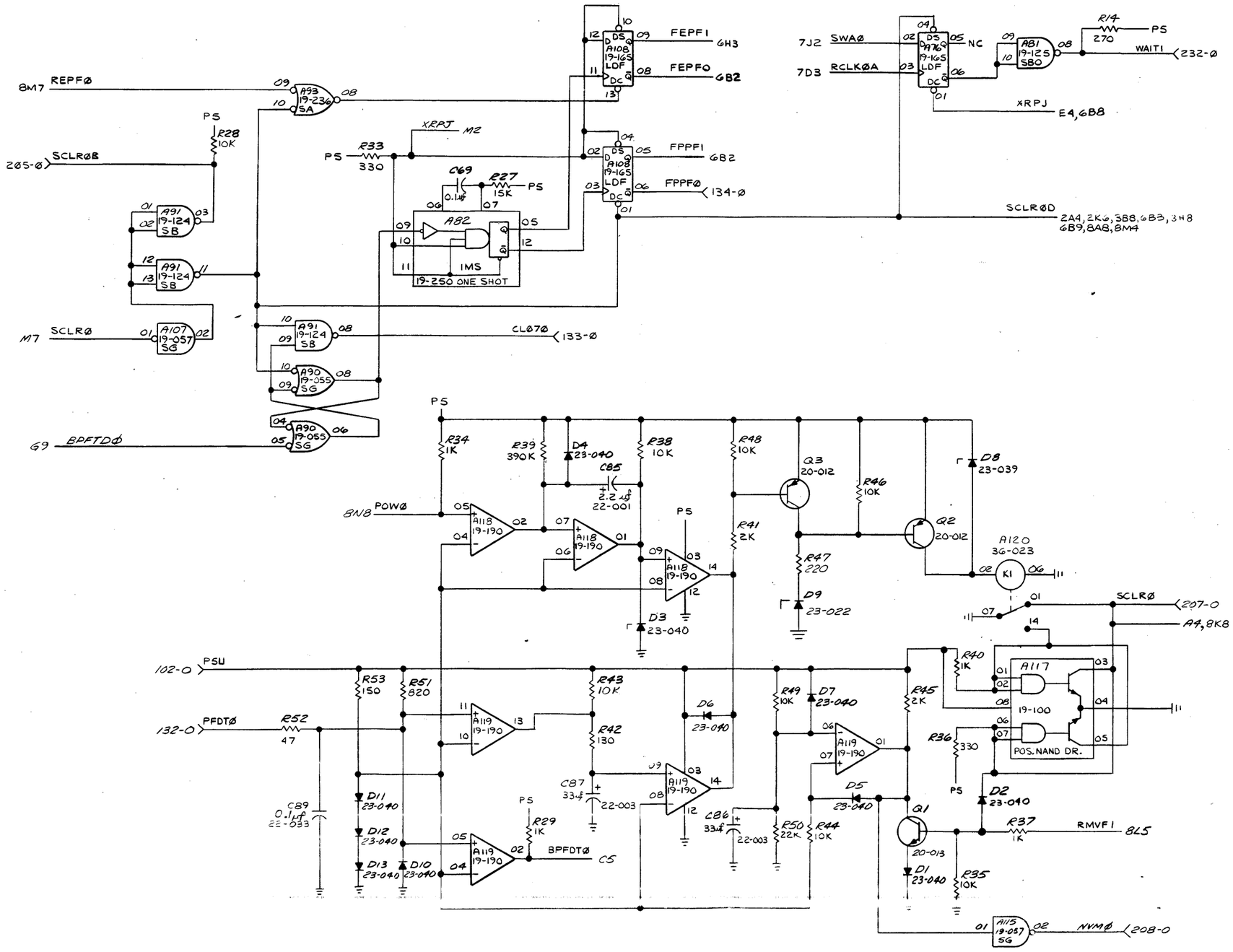


NOTE:
UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE 1/4W ±5%.

SCALE—	NAME	TITLE	DATE
TOLERANCE .XXX ± .005, .XX ± .02, .X ± .1, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE CPU-A
RD DECODING
B-BOARD SUPPORT

TASK NO. 03179
DWG NO. 35-816RØ1 D08
SHEET 8 OF 10



REVISIONS					
IN AREA L9 19-057 GATE (A115) PINS 01 & 02 WERE NOT SPEC.					
U.J.P.	BNL	ECR 4844	M	9-11-81	R01
ADDED C89 TO AREA D8					
VT	GV	4973	M	3-22-82	R02

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	E. JOHNSON	DES/DFT	
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

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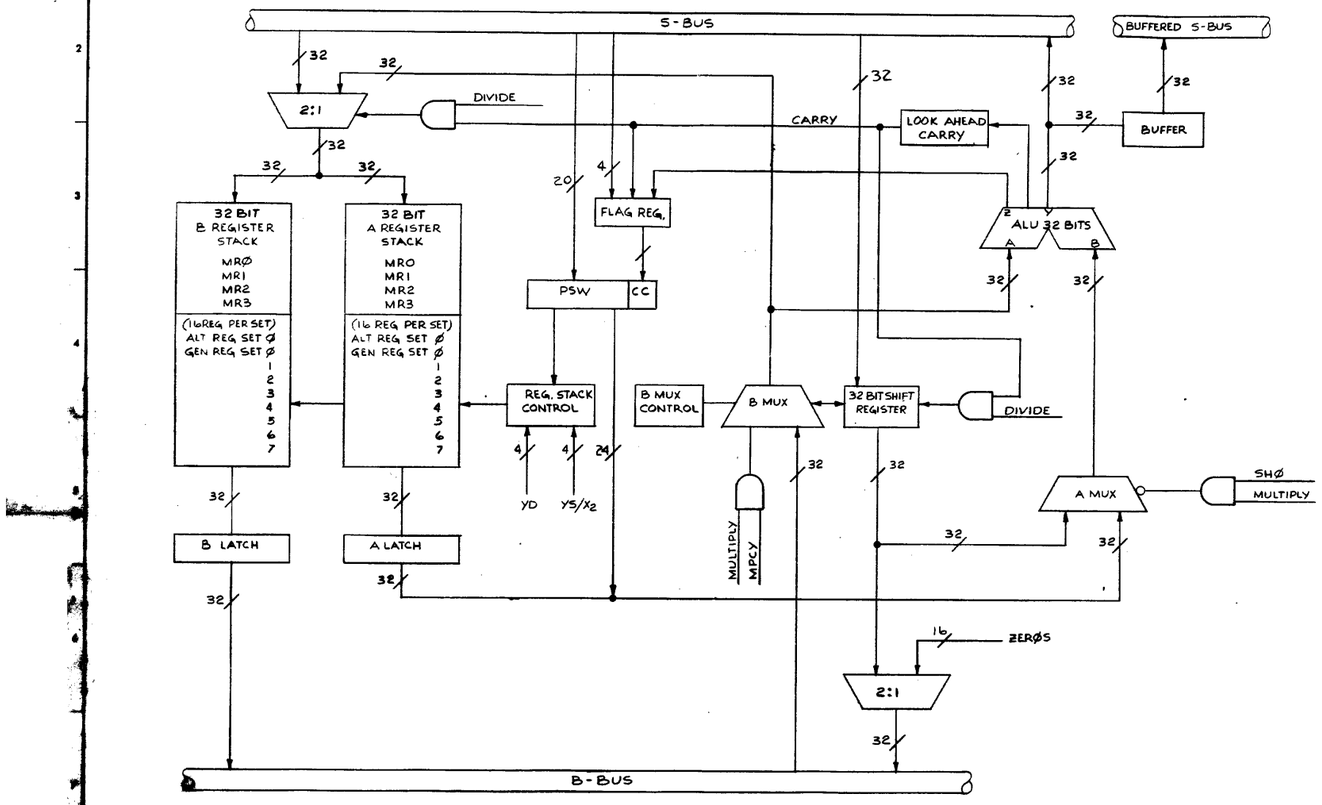
Oceanport, N.J. 07757

TITLE

TASK 03179	SHT
DWG 85-816 R02 D08	9 - 10

NOTES



NOTE:
FOR NET # MNEMONIC & LOCATION TO SCHEMATIC SEE SHT. 16.

16M	19-126	08
14M	19-235	11
13H	19-057	12,
13B	19-057	06,08
12S	19-057	04,10,12
03E	19-057	04
REF. DESIGN.	PART NUMBER	SPARE OUTPUT

TABLE OF SPARES

CONN	TERM. NO.	CABLE CONNECTOR MAP ROW 2	CABLE CONNECTOR MAP ROW 1	BACK PANEL MAP ROW 1	BACK PANEL MAP ROW 2	TERM. NO.	CONN
5	16			P5	P5	41	1
	15			GND	GND	40	
	14			SR10	SR00	39	
	13			MPY0	SH1	38	
	12			DIV0	ULSR0	37	
	11			GRD101	ENBS0	36	
	10			GRD091	GRD111	35	
	09			RD221	RD231	34	
	08			RD201	RD211	33	
	07			RD190	RD191	32	
	06			RD170	RD181	31	
	05			RD250	RD271	30	
	04			RD251	RD261	29	
	03			RD240	RD121	28	
	02			RD141	RD131	27	
	01			RD150	RD161	26	
	00					25	
						24	
					RD0S1	23	
4	24	S301	S311			22	
	23	S281	S291	GND	GND	21	
	22	GND	S271	YS01	YS11	20	
	21	S261	S251	YS21	YS31	19	
	20	S241		PSW101	PSW111	18	
	19	S221	S231	PSW201	PSW251	17	
	18	GND	S211	PSW261	PSW271	16	
	17	S201	S191	PSW131	PSW231	15	
	16	S181		PSW171	PSW181	14	
	15	S161	S171	AENH0	AENL0	13	
	14	GND	S151	PSW121	PSW211	12	
	13	S141	S131	PSW191	PSW151	11	
	12	S121		CLFR0	PSW141	10	
	11	S101	S111	GND	GND	09	
	10	GND	S091	YD081	YD091	08	
	09	S081	S071	YD101	YD111	07	
	08	S061		FLR281	FLR291	06	
	07	S041	S051	FLR301	FLR311	05	
	06	GND	S021	GFLR291	LFLR1	04	
	05	S021	S011		BSTKS0	03	
	04	S001			JAMC10	02	
	03	GND		GND	GND	01	
	02	GND		P5	GND	00	
	01	GND					
	00	GND	GND	P5	GND	41	
				GND	GND	40	
				CLKCC0	CLKPSW0	39	
				CLK1B	SCLK1	38	
				GND	GND	37	
	24	GND	GND			36	
	23	S011	S001		DSTOP0	35	
	22	S031	S021			34	
	21	GND	GND	GND	GND	33	
	20	S051	S041	S160	S170	32	
	19	S071	S061	S180	S190	31	
	18	GND	GND	S200	S210	30	
	17	S091	S081	S220	S230	29	
	16	S111	S101	GND	GND	28	
	15	GND	GND	B001	B011	27	
	14	S131	S121	B021	B031	26	
3	13	S151	S141	B041	B051	25	
	12	GND	GND	B061	B071	24	
	11	S171	S161	B081	B091	23	
	10	S191	S181	B101	B311	22	0
	09	GND	GND	B121	B131	21	
	08	S211	S201	B141	B151	20	
	07	S231	S221	B161	B171	19	
	06	GND	GND	B181	B191	18	
	05	S251	S241	B201	B211	17	
	04	S271	S261	B221	B231	16	
	03	GND	GND	B241	B251	15	
	02	S291	S281	B261	B271	14	
	01	S311	S301	B281	B291	13	
	00	GND	GND	B301	B311	12	
				GND	GND	11	
				S240	S250	10	
	16			S260	S270	09	
	15			S280	S290	08	
	14			S300	S310	07	
	13			GND	GND	06	
	12				SCLR0B	05	
	11				EXB0	04	
	10					03	
	09					02	
2	08			GND	GND	01	
	07			P5	GND	00	
	06						
	05						
	04						
	03						
	02						
	01						
	00						

CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

PERKIN ELMER

REVISIONS

PRE PRODUCTION APPROVAL	DEV PROD	INIT	DATE

RELEASED FOR PRODUCTION
DEV MFG. ENG: Bailey DATE 7/2/80

AREA 5B: BOARD REV WAS R00. REVISED SHTS 1 & 7

ECO	SO94	R	7-19-82	R01	X

USED IN MANUAL 47-011

35-768	R02
BOARD	REV. LEVEL

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REV. LEV.

REVISION	1															
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

SCALE —

NAME	TITLE	DATE
R STINE	DRAFT	
E GREENSTEIN	SYS TEST	
R. CERO	CHK	
R. BALAS	ENGR	
R.A BARKER	QC	
D. FRANKENBERGER	MGR	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE CPU-B CONNECTOR MAP

TASK NO.
DWG NO. 35-768 R01 D08
SHEET OF 1 — 16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

065 19-082 SG0

06T 19-132 2TO1 MUX

06W 19-132 2TO1 MUX

03C 19-066 2TO1 MUX

07T 19-132 2TO1 MUX

07W 19-132 2TO1 MUX

03D 19-066 2TO1 MUX

04B 19-068 LOOK AHEAD CAR. GEN

02B 19-067 4-BIT ALU

02F 19-067 4-BIT ALU

04C 19-068 LOOK AHEAD CAR. GEN.

02C 470 1K 1K 1K

05H 1K 1K 1K 1K

05C 330

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SCALE—	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	DESTINE	DRAFT	8-13-78
		CHK	
		ENGR	

TITLE CPU-B BITS 0-7

TASK NO

DWG NO 35-768 DAB SHEET OF 2—16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

08W 19-132 2TO1 MUX
09W 19-132 2TO1 MUX
04D 19-066 2TO1 MUX
10W 19-132 2TO1 MUX
12W 19-132 2TO1 MUX
04E 19-066 2TO1 MUX

05C 1K 1K 1K 1K P5
05H 1K 1K 1K 1K P5

05B 19-067 4-BIT ALU
05F 19-067 4-BIT ALU

ZEROL 1524

SCALE—	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .09, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	BSTINE	DRAFT	4-13-78
		CHK	
		ENGR	

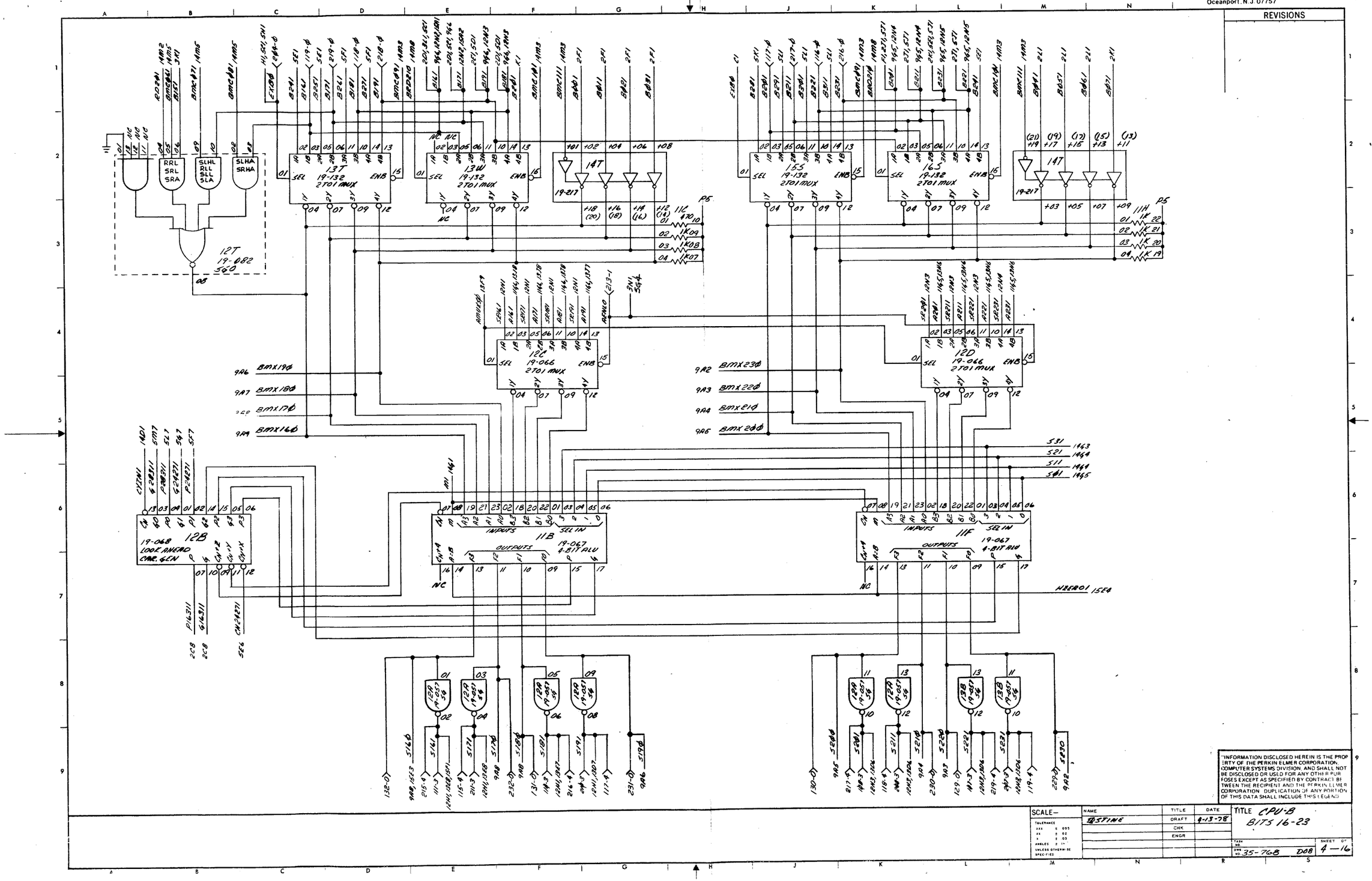
TITLE CPU-B BITS 8-15

TASK NO.
DWG NO. 35-768 D08
SHEET 3 OF 16

PERKIN ELMER

Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



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SCALE—	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	RESTINE	DRAFT	4-13-78
		CHK	
		ENGR	

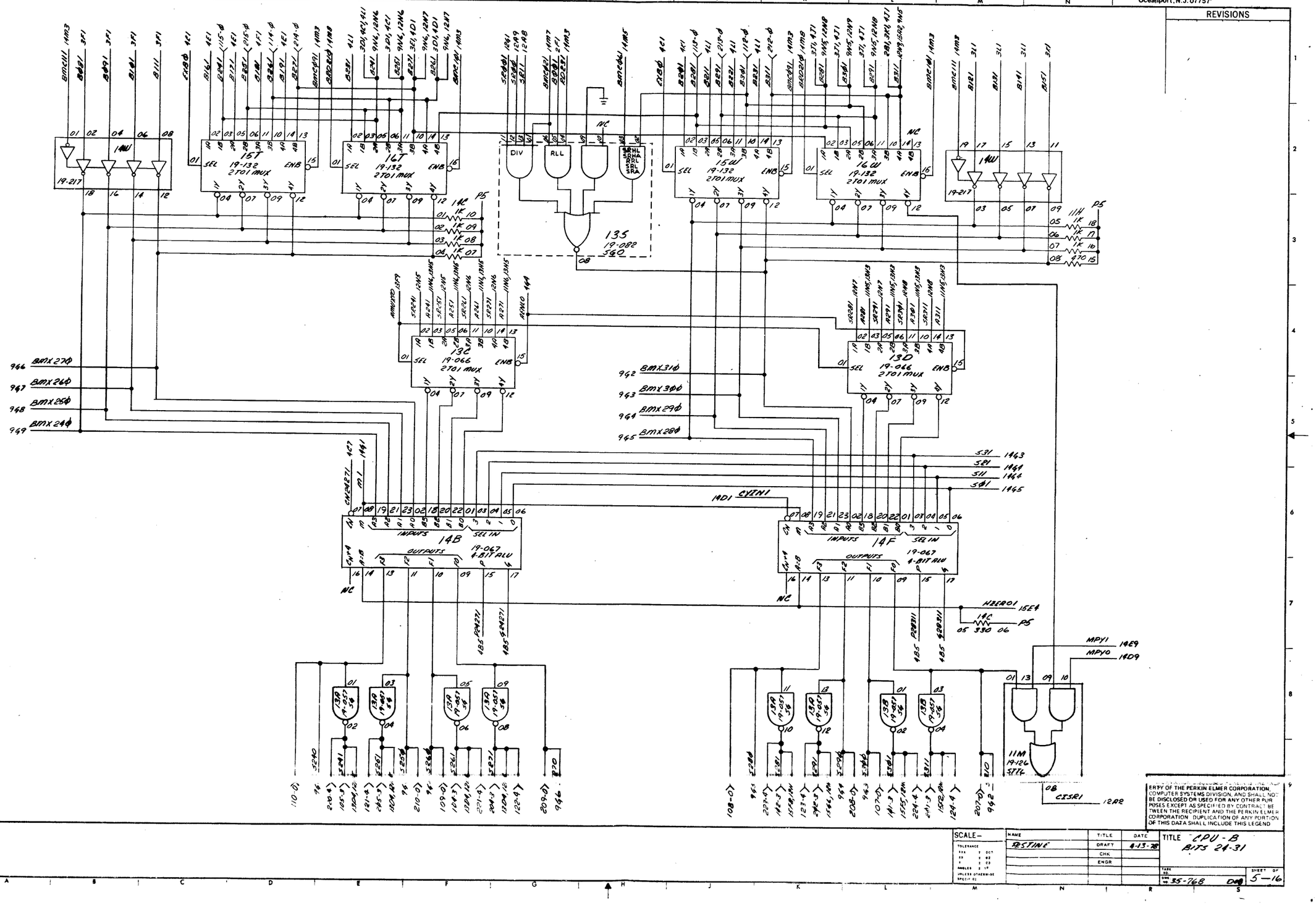
TITLE CPU-B BITS 16-23

TASK NO. SYS NO. 35-768 D08

SHEET 4 OF 16

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

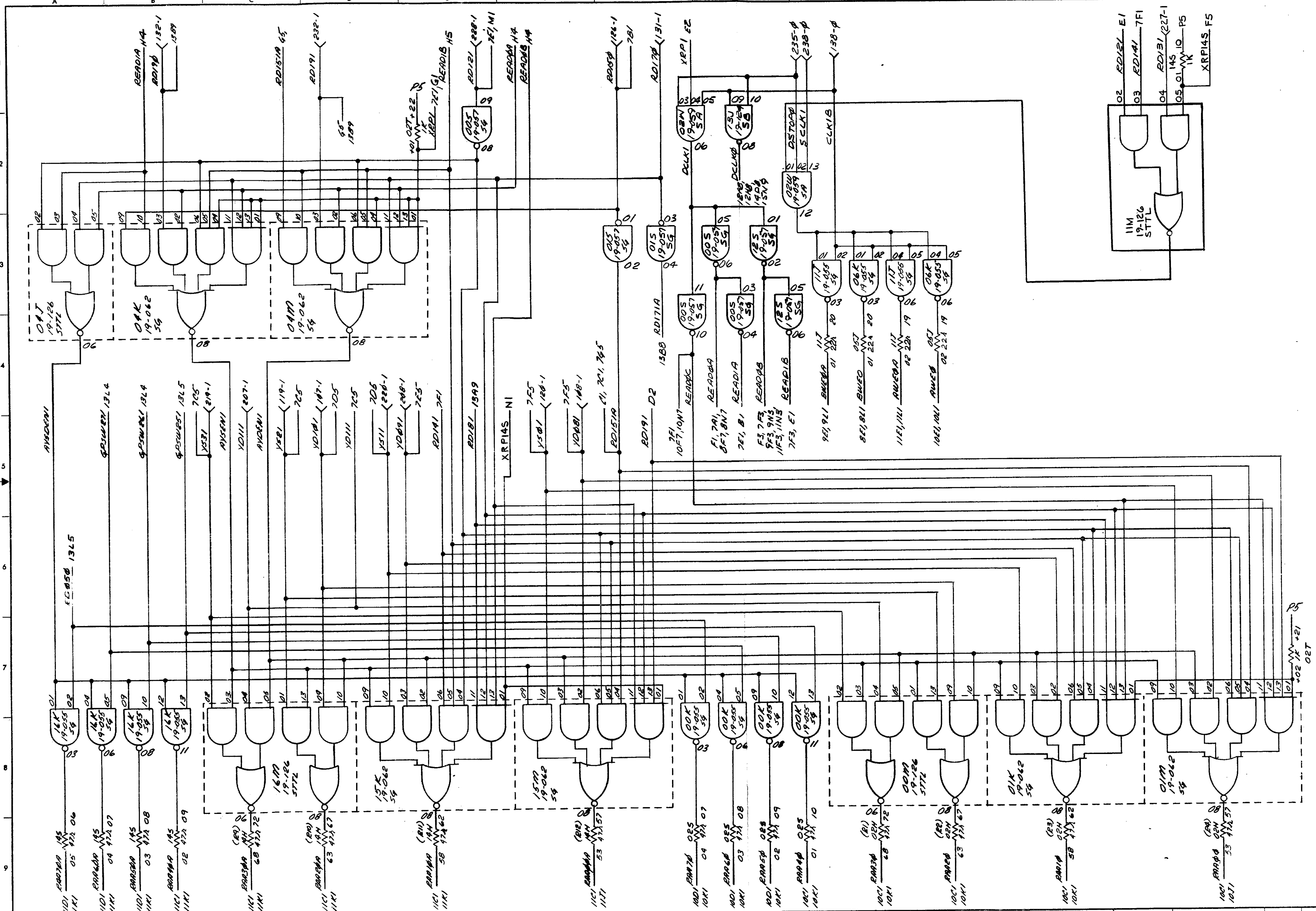


SCALE –	NAME	TITLE	DATE
TOLERANCE	RESTINE	DRAFT	4-13-78
		CHK	
		ENGR	

TITLE CPU-B BITS 24-31

SIZE B | SHEET 5 OF 16 | DWG NO. 55-768 | REV

REVISIONS



INFORMATION DISCLOSED HEREIN IS THE PROPERTY OF THE PERKIN ELMER CORPORATION, COMPUTER SYSTEMS DIVISION, AND SHALL NOT BE DISCLOSED OR USED FOR ANY OTHER PURPOSES EXCEPT AS SPECIFIED BY CONTRACT BETWEEN THE RECIPIENT AND THE PERKIN ELMER CORPORATION. DUPLICATION OF ANY PORTION OF THIS DATA SHALL INCLUDE THIS LEGEND

SCALE–	NAME	TITLE	DATE	TITLE CPU-B A-FIELD RD DECODE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± , UNLESS OTHERWISE SPECIFIED	JD STINE	DRAFT	4-13-78	
		CHK		
		ENGR		
				TASK NO.
				DWG NO. 35-768 D08 — SHEET 6 OF 16

PERKIN-ELMER

REVISIONS
AREA L1-L5 REVISED REG TABLE INFO. SEE R00 MICROFILM FOR PREVIOUS REV LEVEL
REV | LTR | 5094 | R | 7-19-82 | R01

A2D	A1D	A0D	A3D	A2D	A1D	A0D	
1	1	1	1	1	1	1	MRØ
1	1	1	1	1	1	0	MR1
1	1	1	1	1	0	1	MR2
1	1	1	1	1	0	0	MR3
1	0	0	0				ALT REG SET
0	1	1	1				REG SET Ø
0	0	1	1				REG SET 1
0	1	0	1				REG SET 2
0	0	0	1				REG SET 3
0	1	1	0				REG SET 4
0	0	1	0				REG SET 5
0	1	0	0				REG SET 6
0	0	0	0				REG SET F
				1	1	1	1 GEN REG Ø
				0	1	1	1 GEN REG 1
				1	0	1	1 GEN REG 2
				0	0	1	1 GEN REG 3
				1	1	0	1 GEN REG 4
				0	1	0	1 GEN REG 5
				1	0	0	1 GEN REG 6
				0	0	0	1 GEN REG 7
				1	1	1	0 GEN REG 8
				0	1	1	0 GEN REG 9
				1	0	1	0 GEN REG A
				0	0	1	0 GEN REG B
				1	1	0	0 GEN REG C
				0	1	0	0 GEN REG D
				1	0	0	0 GEN REG E
				0	0	0	0 GEN REG F

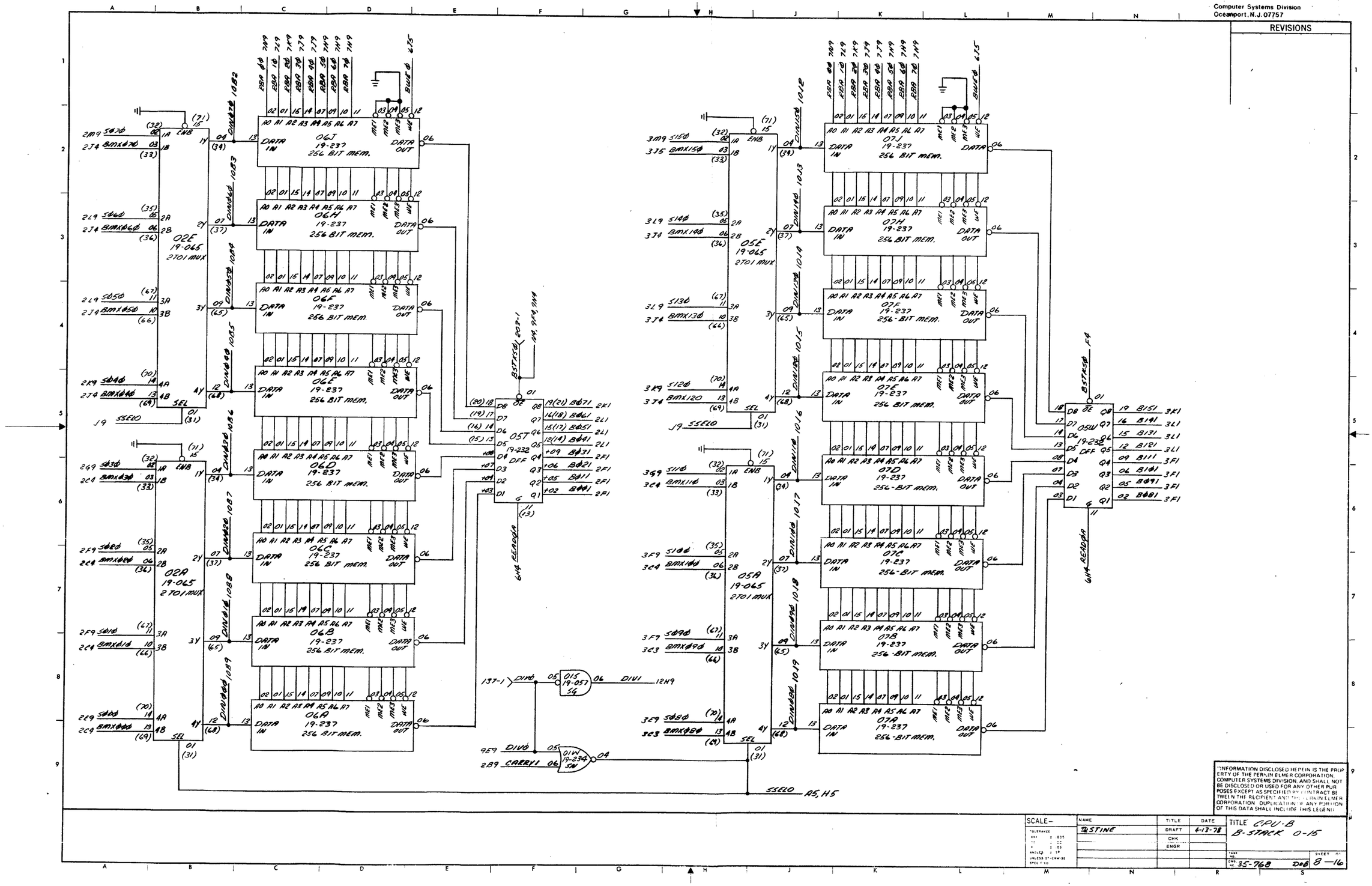
SCALE –	NAME	TITLE	DATE
TOLERANCES: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 0°, UNLESS OTHERWISE SPECIFIED	IRSTINE	DRAFT	4-13-78
		CHK	
		ENGR	

TITLE CPU-B B-FIELD RD DECODE

SIZE — DWG NO. 35-768 R01 D08 — SHEET OF 7-16

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



SCALE—
TOLERANCE
XXX ± .005
XX ± .02
X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

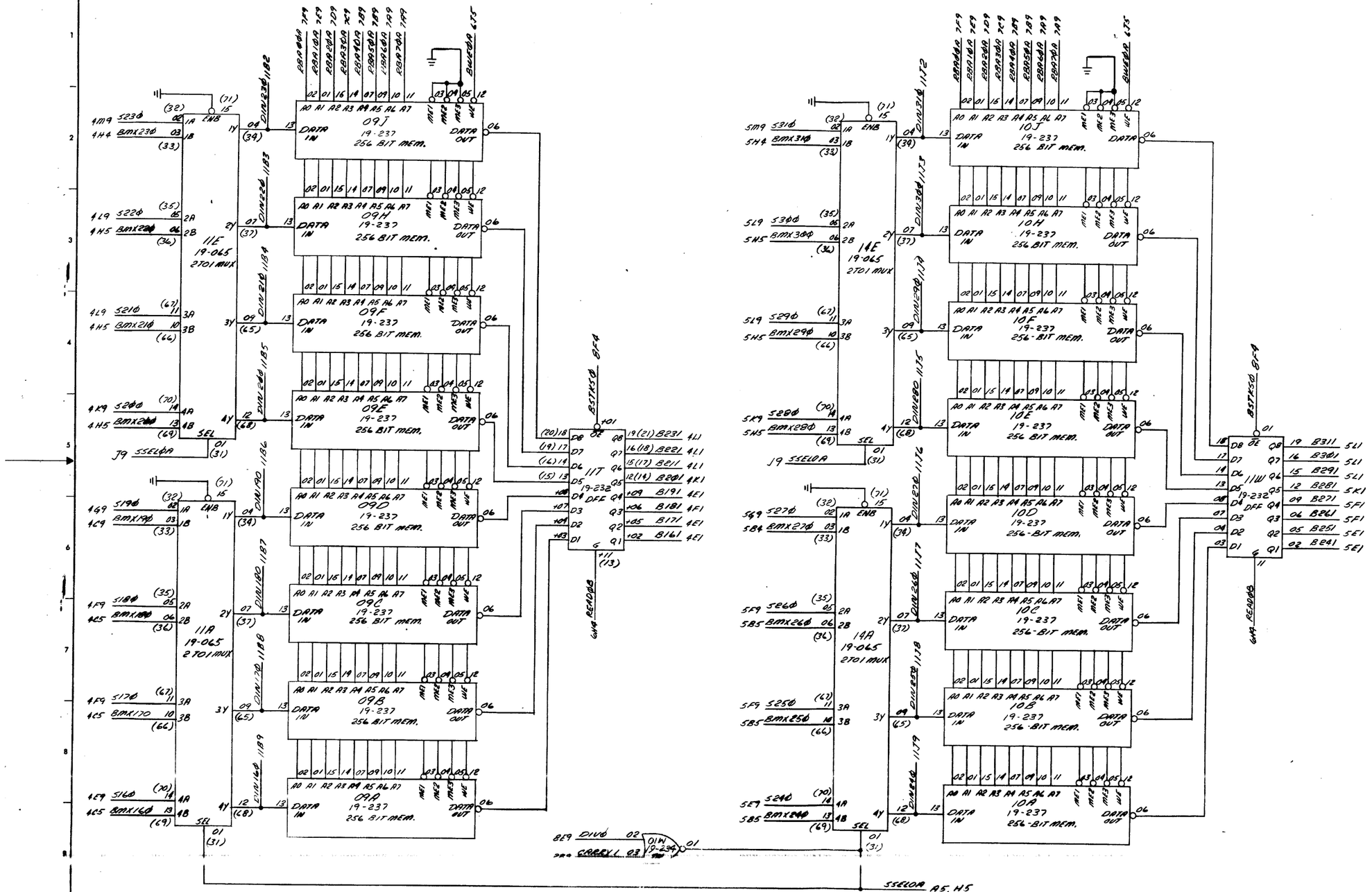
NAME	TITLE	DATE
DESTINE	DRAFT	4-13-78
	CHK	
	ENGR	

TITLE CPU-B
B-STACK 0-15

TASK NO.
DWG NO. 35-768 D08
SHEET 01
8—16

PERKIN-ELMER

REVISIONS



SCALE —	NAME	TITLE	DATE
TOLERANCE	DESTINE	DRAFT	4-13-78
		CHK	
		ENGR	

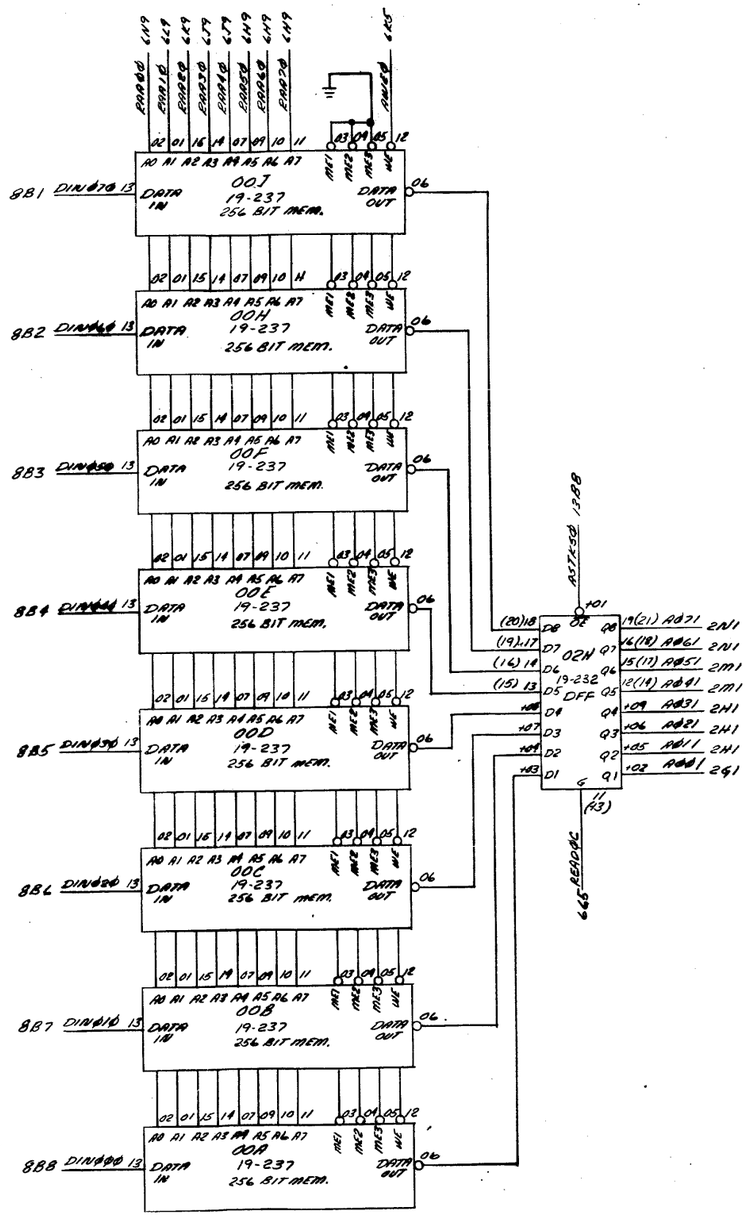
TITLE CPU-B B-STACK 16-31

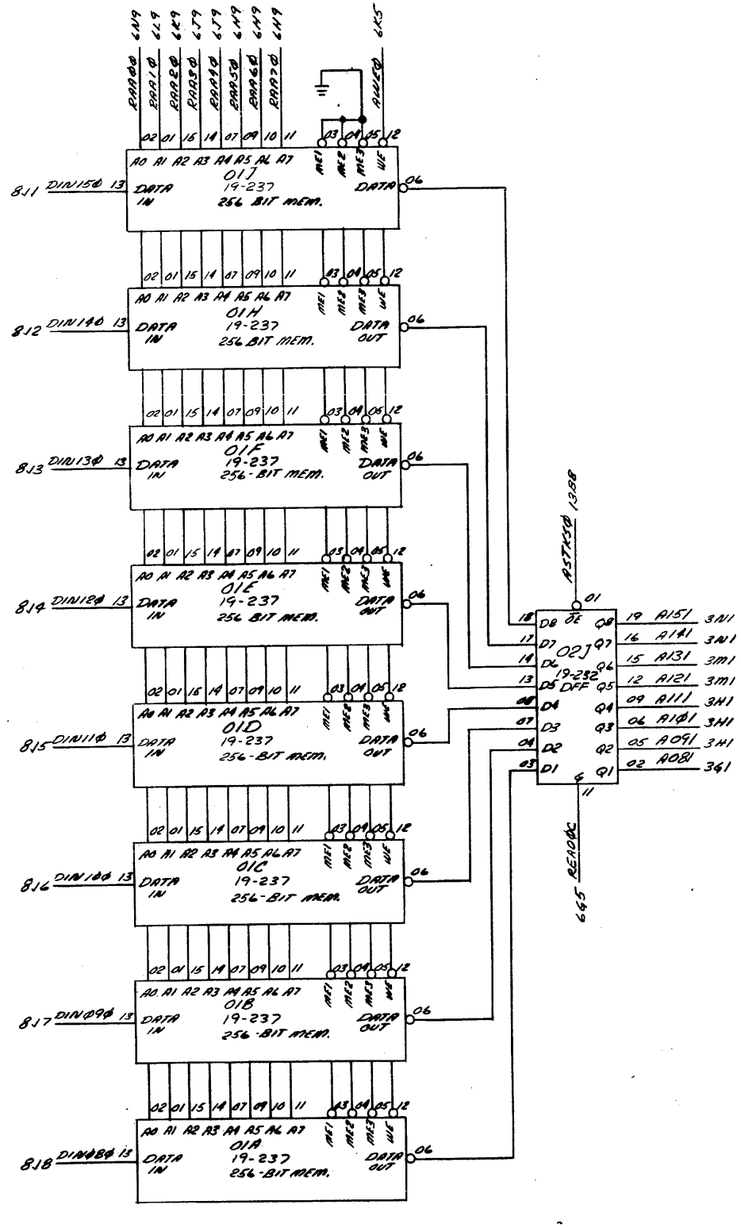
SIZE A 35-7628 DWG

SHEET 9 OF 16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS





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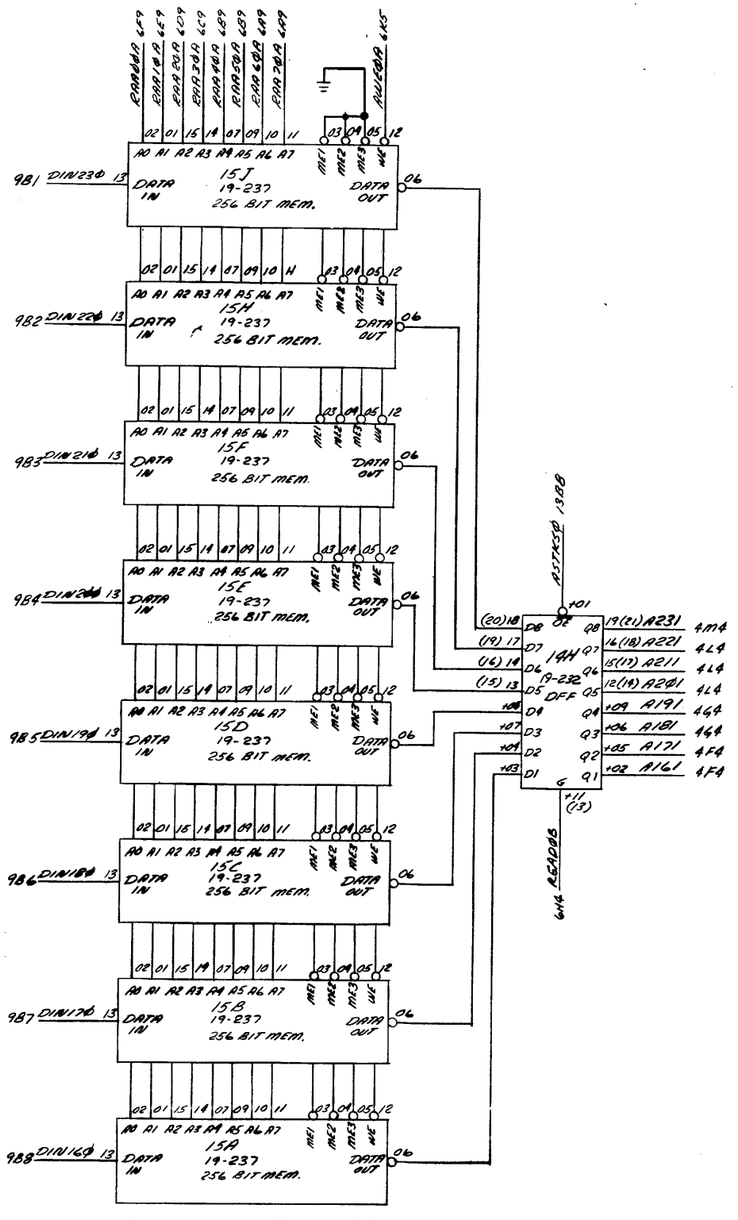
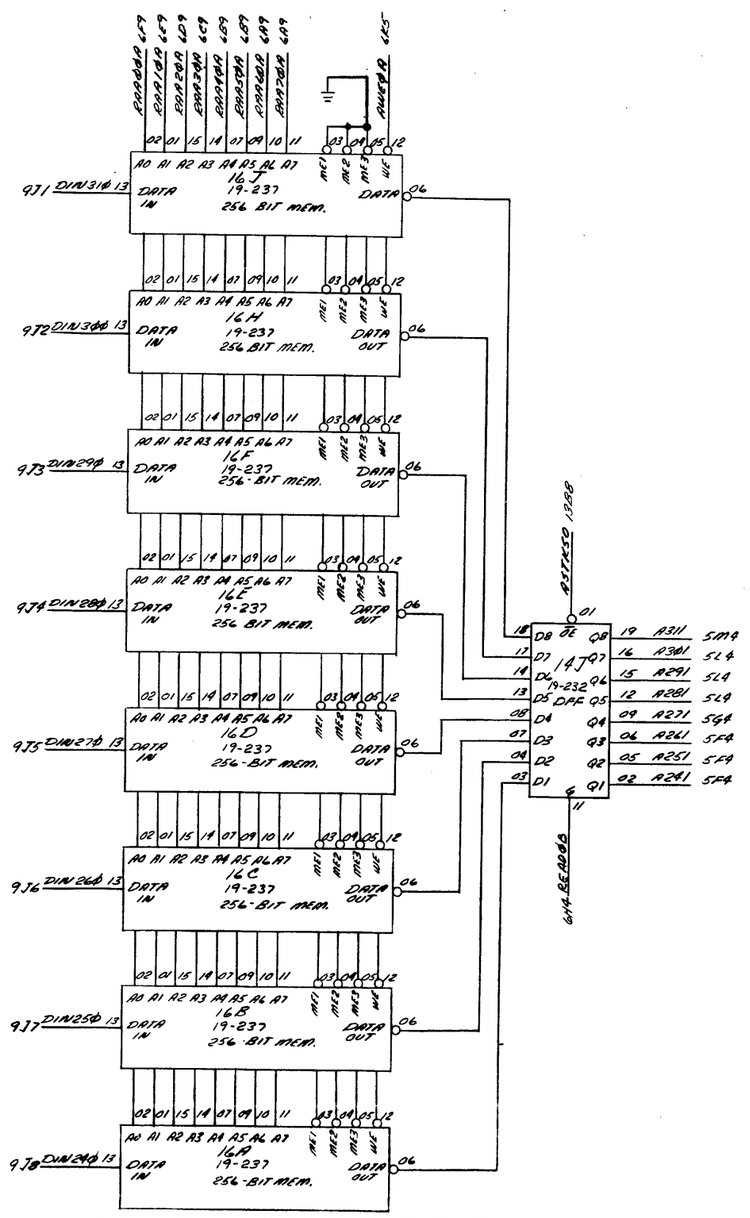
SCALE—	NAME	TITLE	DATE	TITLE CPU-B A-STACK 0-15
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	D.STONE	DRAFT	4-13-78	
		CHK.		
		ENGR		
				FSN0. — DWG. NO. 35-7GB D08 SHEET 10 OF 16

PERKIN ELMER

REVISIONS





SCALE—	NAME	DATE	TITLE CPU-B
TOLERANCE	DSTINE	DRAFT 4-13-78	A-STACK 16-31
XXX ± .005		CHK	
XX ± .02		ENGR	
X ± .03			
ANGLES ± 1°			
UNLESS OTHERWISE SPECIFIED			TASK NO.
			DWG NO. 35-7688 DOB SHEET 11 OF 16

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

237-1 ULSRϕ
205-ϕ SCLRϕB

2E9 S$\phi$$\phi$1
2F9 Sϕ11
2G9 Sϕ21
2H9 Sϕ31
EN9 CISR1

OBA 19-182 4 BIT L/R SHIFT REG

SR$\phi$$\phi$1 2G1, 5G1
SRϕ11 2G1
SRϕ21 2N1
SRϕ31 2N1

075 19-196 2 TO 1 MUX (STTL)

B$\phi$$\phi$1 2F1
Bϕ11 2F1
Bϕ21 2F1
Bϕ31 2F1

2K9 Sϕ41
2L9 Sϕ51
2L9 Sϕ61
2M9 Sϕ71

OBB 19-182 4 BIT L/R SHIFT REG

SRϕ41 2M1
SRϕ51 2M1
SRϕ61 2N1
SRϕ71 2N1

085 19-196 2 TO 1 MUX (STTL)

Bϕ41 2L1
Bϕ51 2L1
Bϕ61 2L1
Bϕ71 2K1

3E9 Sϕ81
3F9 Sϕ91
3G9 S1ϕ1
3H9 S111

OBC 19-182 4 BIT L/R SHIFT REG

SRϕ81 3G1
SRϕ91 3G1
SR1ϕ1 3N1
SR111 3H1

OBT 19-196 2 TO 1 MUX (STTL)

Bϕ81 3F1
Bϕ91 3F1
B1ϕ1 3F1
B111 3F1

14G8 $CLR0B

3K9 S121
3L9 S131
3L9 S141
3M9 S151

OBD 19-182 4 BIT L/R SHIFT REG

SR121 3M1
SR131 3M1
SR141 3N1
SR151 H2, 3N1

N1 SR161
6H3 DCLKϕ
5G1, H8 $R11
H8 SRϕ1

095 19-196 2 TO 1 MUX (STTL)

B121 3L1
B131 3L1
B141 3L1
B151 3K1

139-1) SR1ϕ 09 — 13H 19-057 5G — 08
239-1) SR$\phi\phi$ — 11 — 13H 19-057 5G — 10
236-1) ENBS0

4E9 S161
4F9 S171
4G9 S181
4H9 S191
G8 SR15'1

OBE 19-182 4 BIT L/R SHIFT REG

SR161 AB, 4F4
SR171 4F4
SR181 4F4
SR191 4G4

09T 19-229

B161 4E1
B171 4E1
B181 4F1
B191 4E1

4K9 S201
4K9 S211
4L9 S221
4M9 S231

OBF 19-182 4 BIT L/R SHIFT REG

SR201 4L4
SR211 4L4
SR221 4L4
SR231 4M4

09T 19-229

B2ϕ1 4K1
B211 4L1

105 19-229

B221 4L1
B231 4L1

5E9 S241
5F9 S251
5F9 S261
5G9 S271

OBA 19-182 4 BIT L/R SHIFT REG

SR241 5F4
SR251 5F4
SR261 5F4
SR271 5G4

105 19-229

B241 5E1
B251 5E1
B261 5F1
B271 5F1

5K9 S281
5K9 S291
5L9 S301
5M9 S311

OBJ 19-182 4 BIT L/R SHIFT REG

SR281 5L4
SR291 5L4
SR301 5L4
SR311 5M4, 14D8

6H3 DCLKϕ
A8 $R11
A9 SRϕ1

2B9 CARRY1 — 09 — 02W 19-059 5A — 08
8G8 DIV1 — 10 — 11

10T 19-229

B281 5K1
B291 5L1
B301 5L1
B311 5L1

SI	SO
0	0 - HOLD DATA
0	1 - SHIFT RIGHT
1	0 - SHIFT LEFT
1	1 - LOAD

SCALE—
TOLERANCE
XXX ± .005
XX ± .02
X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

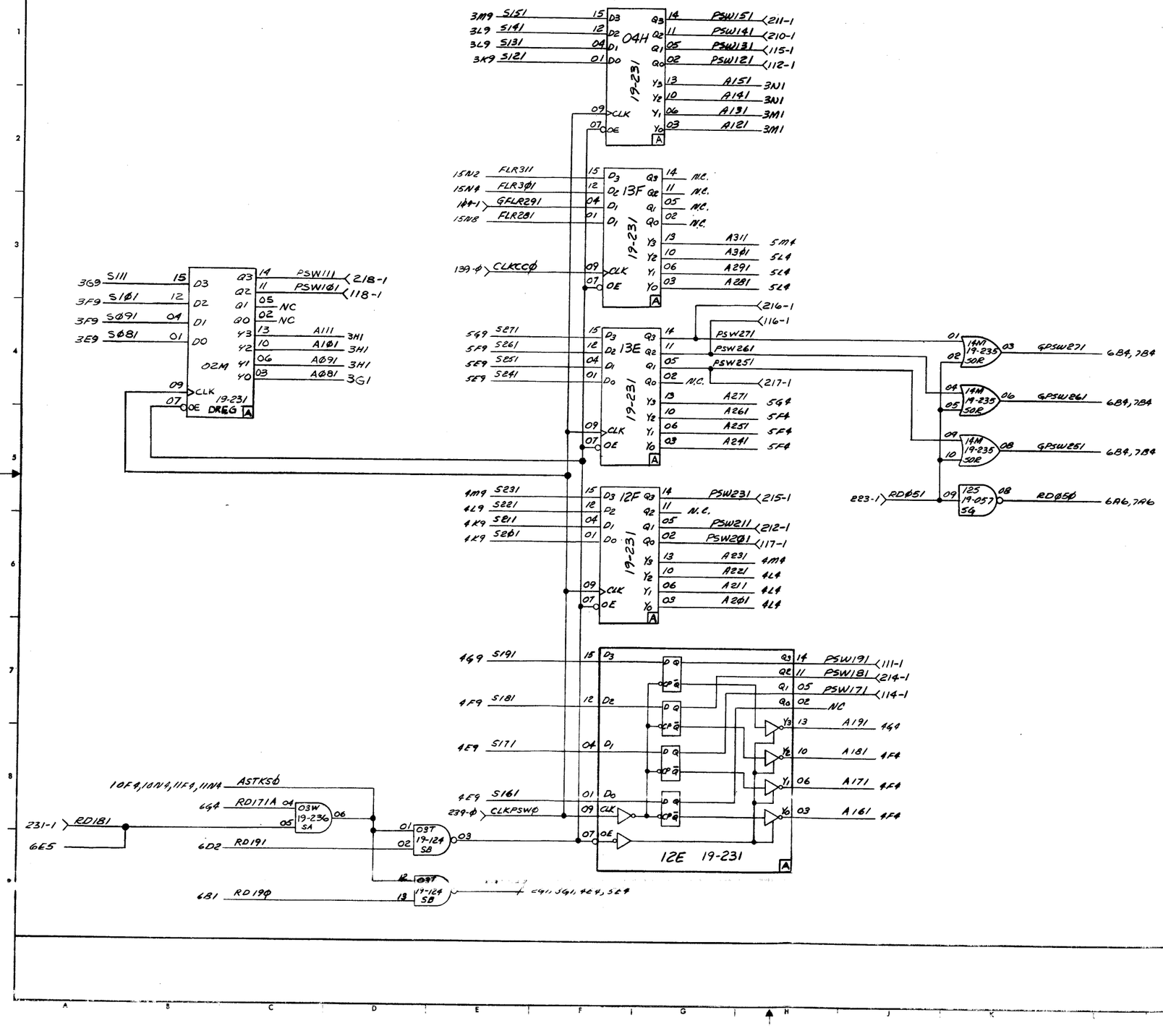
NAME	TITLE	DATE
R. STINE	DRFT	4-13-78
W. LIMPERT	CHK	
	ENGR	

TITLE CPU-B
SHIFT REGISTER

DWG NO. 35-763 DOB
SHEET 12 OF 16

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS



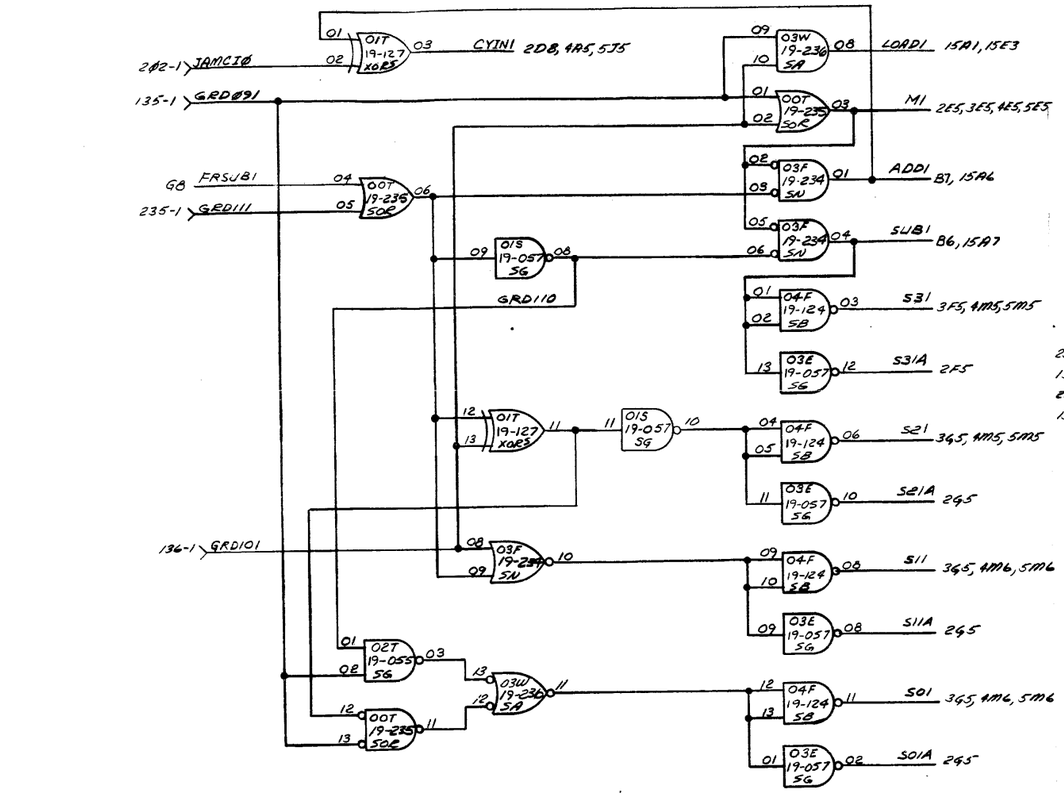
SCALE	NAME	TITLE	DATE
	R STINE	DRAFT	4-13-78
		CHK	
		ENGR	

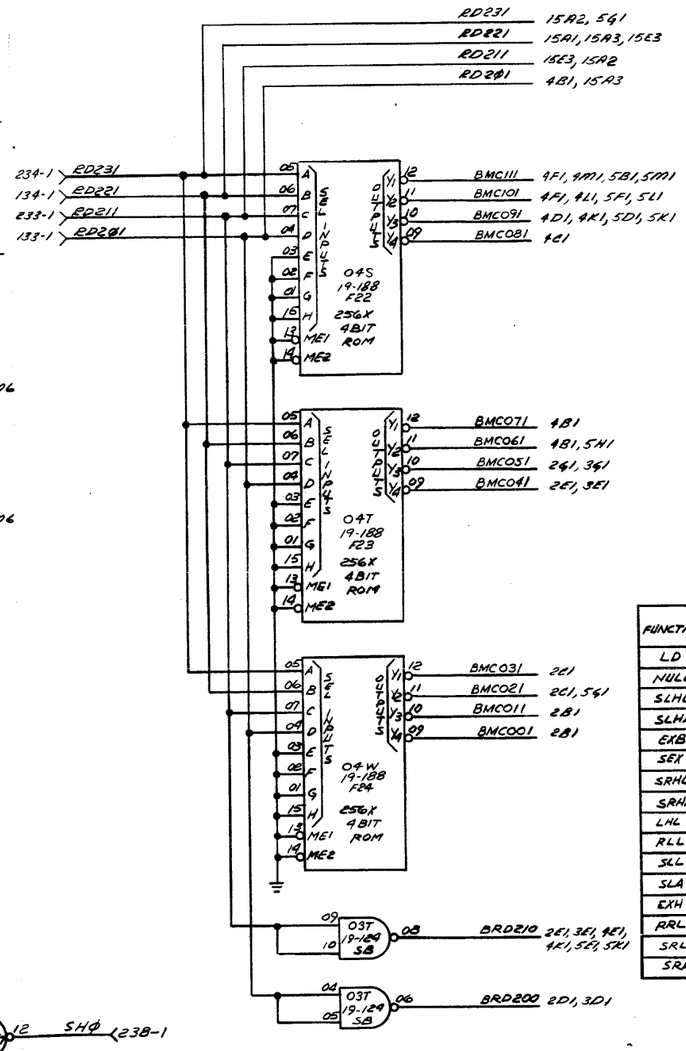
TITLE CPU B PROGRAM STATUS REGISTER, CONDITION CODE REGISTER

TASK NO. | PRM NO. 35-768 DOB | SHEET OF 13-16

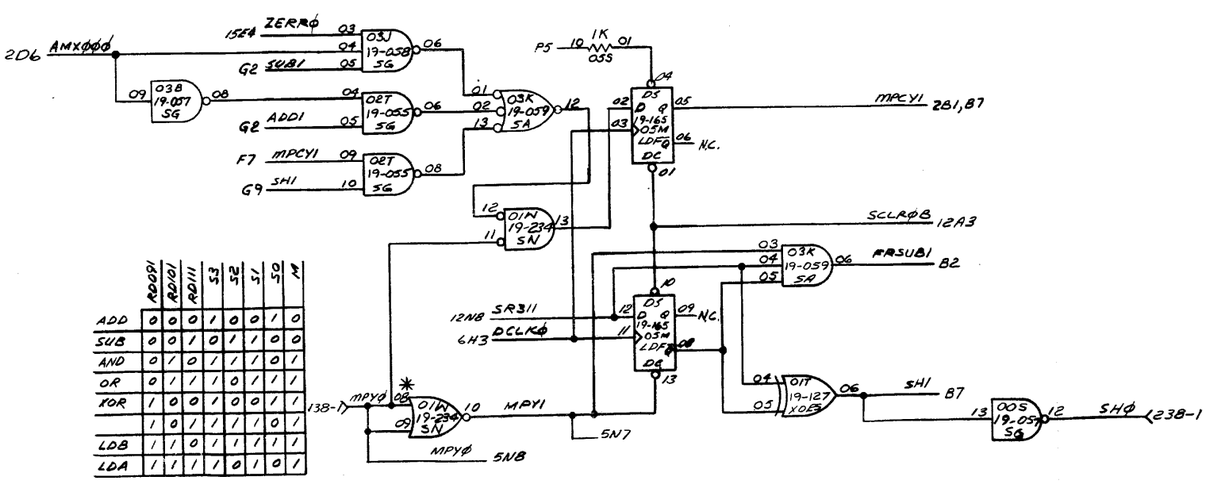
PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS





FUNCTION	RDBIT 2 2 2 2 0 1 2 3	BMC 0 0 0 0 0 1 2 3	BMC 0 0 0 0 4 5 6 7	BMC 0 0 1 1 8 9 0 1
LD	0 0 0 0	0 0 0 0	0 1 0 0	0 0 1 1
NULL	0 0 0 1	0 0 0 0	1 1 0 0	0 1 1 1
SLHL	0 0 1 0	0 0 0 0	0 1 0 1	0 1 0 1
SLHA	0 0 1 1	0 0 0 0	0 1 0 0	1 1 0 1
EXB	0 1 0 0	0 0 0 0	0 1 0 0	0 0 1 1
SEX	0 1 0 1	0 0 0 0	0 1 0 0	0 0 1 1
SRHL	0 1 1 0	0 0 0 0	0 1 1 0	0 1 0 1
SRHA	0 1 1 1	0 0 0 0	0 1 1 0	1 1 0 1
LHL	1 0 0 0	0 0 0 0	1 1 0 0	0 0 1 1
RLL	1 0 0 1	0 0 1 0	1 0 0 1	0 1 0 1
SLL	1 0 1 0	0 0 1 0	1 0 0 1	0 1 0 1
SLA	1 0 1 1	0 0 0 1	1 0 0 1	0 1 0 1
EXH	1 1 0 0	0 0 0 0	0 1 0 0	0 1 1 0
RRL	1 1 0 1	0 1 0 0	1 0 1 0	0 1 0 1
SRL	1 1 1 0	1 0 0 0	1 0 1 0	0 1 0 1
SRA	1 1 1 1	0 0 0 1	1 0 1 0	0 1 0 1



	RDØ9/	RDIØI/	RDIII/	S3	S2	S1	S0	M
ADD	0	0	0	1	0	0	1	0
SUB	0	0	1	0	1	1	0	0
AND	0	1	0	1	1	1	0	1
OR	0	1	1	1	0	1	1	1
XOR	1	0	0	1	0	0	1	1
	1	0	1	1	1	1	0	1
LDB	1	1	0	1	1	1	1	1
LDA	1	1	1	1	0	1	0	1

* SEE CPU-A SCHEMATICS SHEET 3B13 FOR ADDITIONAL INFORMATION.

SCALE—	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	TOSTINE	DRAFT	4-13-78
		CHK.	
		ENGR	

TITLE CPU-B

TASK NO.

DWG NO. 35-768 DOB

SHEET 14 OF 16

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

14M2 RD221 12 — 02T 19-055 SG — 11
1461 LOAD1 13

2F1 B00I
2F1 B01I
4E1 B16I
4E1 B17I
5L1 B31I
ENB 07
DATA IN 06M 19-173 8TO1 MUX
Y 05 SHCRY1 FB
W 06 N.C.
14M2 RD231 — A 11
14M2 RD211 01 — 03W 19-236 5A — 03
14M2 RD221 02 — B 10
C 09
SEL DATA

14M2 RD261 — 015 19-057 SG — 12

4E9 S161
2E9 S001
5M9 S311
4E9 S160
12H 19-062 SG
HW LOAD
FW LOAD
LOAD FLR
NC 02

14M2 RD221 09 — 00T 19-236 SOR — 08
14M2 RD211 10
09 — 03K 19-059 5A — 08
10
11
1461 LOAD1

4M7, 5M7 HZERO1 — 13J 19-124 SG — 11
2N7, 3N7 ZERO1 12
1486 ZERRO
01 — 13H 19-057 SG — 02
12 — 03F 19-234 SN — 13
11
S301
5L9
2E9 S000
12J 19-062 SG
12K 19-062 SG
12M 19-062 SG
SUB
ADD
LOAD SHIFT

1462 ADD1 — 03H 19-058 SG — 06 — 13J 19-124 SG — 03
2D6 AMX000 09 — 01T 19-127 XORS — 08 — 03E 19-057 SG — 06
10
1462 SUB1 — 03J 19-058 SG — 12 — 13J 19-124 SG — 06
2C4 BMX000 05 — 03B 19-057 SG — 06
2E9 S001
5K9 S291
2B9 CARRY 1
E1 SHCRY 1
5K9 S281
13H 19-057 SG — 04
2D4-1 LFLR0 — 13H 19-057 SG — 06

CLFLR0 110-1
LESS THAN
FLR311 (205-1
13E2
GREATER THAN
FLR301 105-1
13E2
OVERFLOW
FLR291 206-1
CARRY
FLR281 (106-1
13E3
05 1114 10 — P5
1K-DCLK0 6H3

DS D Q 19-063 SDF 13M DC

SCALE—
TOLERANCE
XXX ± .005
XX ± .02
X ± .1
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
DESTINE	DRAFT	4-13-78
	CHK	
	ENGR	

TITLE CPU-B
TABS XC
DWG NO 35-768 D08
SHEET 15—16

CROSS REFERENCE NET#, MNEMONIC, SHEET#

NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.
001	CLK1B	06	063	YD081	06	125	09M08	07	187	16H06	11	249	B081	03	311	BMX240	09	373	00B06	10	435	GND09F	09	497	P502C		559	03D07	02	621	S001	02	683	S281	05	745	03T03	13	807		
002	D1TOP0	06	064	YD091	06	126	10A06	09	188	16J06	11	250	B091	03	312	BMX250	09	374	01H06	10	436	GND09H	09	498	P502T	06	560	03D09	02	622	S01	14	684	S190	05	746	03W03	15	808		
003	SCLK1	06	065	YD101	06	127	10B06	09	189	14S01	06	251	B101	03	313	BMX260	05	375	01J06	10	437	GND09J	09	499	P503A		561	03D12	02	623	S010	02	685	S191	05	747	04B10	02	809		
004	RDI21	06	066	YD111	06	128	10C06	09	190	16K03	06	252	B111	03	314	BMX270	09	376	01K08	06	438	GND09S	12	500	P503B		562	03E06	15	624	S011	02	686	S300	05	748	ZERRO	14	810		
005	RDI41	07	067	HZERO1	15	129	10D06	09	191	16K06	06	253	B121	03	315	BMX280	09	377	01M08	06	439	GND10A	09	501	P503E		563	03F10	14	625	S01A	02	687	S301	05	749	12C04	04	811		
006	RDI50	06	068	ZERO1	02	130	10E06	09	192	16K08	06	254	B131	03	316	BMX290	09	378	01S10	14	440	GND10B	09	502	P503F		564	03F13	15	626	S020	02	688	S31	14	750	02W08	12	812		
007	RDI70	06	069	READOA	06	131	10F06	09	193	16K11	06	255	B141	03	317	BMX300	09	379	01S12	15	441	GND10C	09	503	P503H		565	03H06	15	627	S021	02	689	S310	05	751	16W12	05	813		
008	RDI81	06	070	READOB	06	132	10H06	09	194	16M06	06	256	B151	03	318	BMX310	09	380	FRSUB1	14	442	GND10D	09	504	P503J		566	RAA00	10	628	S030	08	690	S311	05	752	CISR1	06	814		
009	RDI90	06	071	READOC	06	133	10J06	09	195	16M08	06	257	B161	04	319	BRD200	14	381	G08111	02	443	GND10E	09	505	P503K		567	ARR00A	11	629	S031	02	691	S31A	02	753	RD050	13	815		
010	RDI91	06	072	READIA	06	134	10K08	07	196	A001	10	258	B171	04	320	BRD210	14	382	G12151	02	444	GND10F	09	506	P503M		568	RAA10	10	630	S040	02	692	00C06	10	754	PSW251	13	816		
011	RD201	04	073	READIB	06	135	10M08	07	197	A011	10	259	B181	04	321	01A06	10	383	G16311	02	445	GND10H	09	507	P503S		569	RAA10A	11	631	S041	02	693	SCLROB	12	755	PSW261	13	817		
012	RD211	14	074	DCLKO	12	136	11J03	06	198	A021	10	260	B191	04	322	01B06	10	384	G24271	04	446	GND10J	09	508	P503T		570	RAA20	10	632	S050	02	694	03H08	15	756	PSW271	13	818		
013	RD221	14	075	04DI2	03	137	11J06	06	199	A031	10	261	B201	04	323	BWEO	08	385	G28311	04	447	GND11A	09	509	P503W		571	RAA20A	11	633	S051	02	695	SH1	14	757	RD051	13	819		
014	RD231	14	076	04E04	03	138			200	A041	10	262	B211	04	324	BWEØA	09	386	01T08	15	448	GND11E	09	510	P504A		572	RAA30	10	634	S060	02	696	SHCRY1	15	758			820		
015	RD240	07	077	04E07	03	139			201	A051	10	263	B221	04	325	BYDEN1	07	387	GND00A	10	449	GND12H	14	511	P504F		573	RAA30A	11	635	S061	02	697	03H12	06	759			821		
016	RD261	07	078	04E09	03	140	12B05	04	202	A061	10	264	B231	04	326	BYSDEN1	07	388	GND00B	10	450	GND12J	14	512	P504J		574	RAA40	10	636	S070	02	698	SR001	02	760			822		
017	RD270	07	079	04E12	03	141	12B06	04	203	A071	10	265	B241	05	327	BYSEN1	07	389	GND00C	10	451	GND12K	14	513	P504K		575	RAA40A	11	637	S071	02	699	SR01	12	761			823		
018	RD271	07	080	05M08	14	142	12B09	04	204	A081	10	266	B251	05	328	CARRY	08	390	GND00D	10	452	GND12T	05	514	P504M		576	RAA50	10	638	S080	03	700	SR011	02	762			824		
019	AENHO	02	081	05S01	14	143	12B11	04	205	A091	10	267	B261	05	329	01C06	10	391	GND00C	10	453	GND13S	05	515	P505C	03	577	RAA50A	11	639	S081	03	701	SR021	02	763			825		
020	AENLO	03	082	06A06	08	144	12B14	04	206	A101	10	268	B271	05	330	00A06	10	392	GND00F	10	454	GND14A	09	516	P505H	03	578	RAA60	10	640	S090	03	702	SR031	02	764			826		
021	RD131	06	083	06B06	08	145	12B15	04	207	A111	10	269	B281	05	331	01D06	10	393	GND00H	10	455	GND14E	09	517	P505M		579	RAA60A	11	641	S091	03	703	SR041	02	765			827		
022	BSTKEO	08	084	06C06	08	146	12C07	04	208	A121	10	270	B291	05	333	01E06	10	394	GND00J	10	456	GND15A	11	518	P505S	07	580	RAA70	10	642	S100	03	704	SR051	02	766			828		
023	CLFLRO	15	085	06D06	08	147	12C09	04	209	A131	10	271	B301	05	333	CN0811	02	395	GND01A	10	457	GND15B	11	519	P506K		581	RAA70A	11	643	S101	03	705	SR061	02	767			829		
024	CLKCCO	13	086	06E06	08	148	12C12	04	210	A141	10	272	B311	05	334	CN12151	02	396	GND01B	10	458	GND15C	11	520	P506S		582	RBA00	08	644	S11	14	706	SR071	02	768			830		
025	CLKPSWO	13	087	06F06	08	149	12D04	04	211	A151	10	273	BC50	08	335	CN2471	04	397	GND01C	10	459	GND15D	11	521	P507K		583	RBA00A	09	645	S110	03	707	SR081	03	769			831		
026	DIVO	08	088	06N06	08	150	12D07	04	212	A161	04	274	BC50A	09	336	CYIN1	05	398	GND01D	10	460	GND15E	11	522	P507M		584	RBA10	08	646	S111	03	708	SR091	03	770			832		
027	ENBS0	12	089	06J06	08	151	12D09	04	213	A171	04	275	BMC001	14	337	04D09	03	399	GND01E	10	461	GND15F	11	523	P508K		585	RBA10A	09	647	S11A	02	709	03J06	14	771			833		
028	EXBO	04	090	06K03	06	152	12D12	04	214	A181	04	276	BMC011	14	338	DCLK1	06	400	GND01F	10	462	GND15H	11	524	P508M		586	RBA20	08	648	S120	03	710	SR101	03	772			834		
029	FLR281	15	091	06K06	06	153	12H08	15	215	A191	04	277	BMC021	14	339	DIN000	10	401	GND01H	10	463	GND15J	11	525	P509K		587	RBA20A	09	649	S121	03	711	SR11	12	773			835		
030	FLR291	15	092	PSW101	13	154	12J08	15	216	A201	04	278	BMC031	14	340	DIN010	10	402	GND01J	10	464	GND16A	11	526	P509M		588	RBA30	08	650	S130	03	712	SR111	03	774			836		
031	FLR301	15	093	PSW11!	13	155	12K08	15	217	A211	04	279	BMC041	14	341	DIN020	10	403	GND02A	08	465	GND16B	11	527	P510K		589	RBA30A	09	651	S131	03	713	SR121	03	775			837		
032	FLR311	15	094	07A06	08	156	12M08	15	218	A221	04	280	BMC051	14	342	DIN030	08	404	GND02E	08	466	GND16C	11	528	P510M		590	RBA40	08	652	S140	03	714	SR131	03	776			838		
033	GFLR291	13	095	07B06	08	157	13C04	05	219	A231	04	281	BMC061	14	343	DIN040	10	405	GND04C	02	467	GND16D	11	529	P511C	04	591	RBA40A	09	653	S141	03	715	SR141	03	777			839		
034	GRD091	14	096	07C06	08	158	13C07	05	220	A241	05	282	BMC071	14	344	DIN050	10	406	GND04S	14	468	GND16E	11	530	P511H	05	592	RBA50	08	654	S150	03	716	SR151	03	778			840		
035	GRD101	14	097	07D06	08	159	13C09	05	221	A251	05	283	BMC081	14	345	DIN060	08	407	GND04T	14	469	GND16F	11	531	P511M	15	593	RBA50A	09	655	S151	13	717	SR161	12	779			841		
036	GRD110	14	098	07E06	08	160	13C12	05	222	A261	05	284	BMC091	14	346	DIN070	08	408	GND04W	14	470	GND16H	11	532	P511S	07	594	RBA60	08	656	S160	15	718	SR171	12	780			842		
037	GRD111	14	099	07F06	08	161	13D04	05	223	A271	05	285	BMC101	14	347	DIN080	10	409	GND05A	08	471	GND16J	11	533	P512A		595	RBA60A	09	657	S161	04	719	SR181	12	781			843		
038	JAMC10	14	100	07H06	08	162	13D07	05	224	A281	05	286	BMC111	14	348	DIN090	10	410	GND05E	08	472	01T11	14	534	P512H		596	RBA70	08	658	S170	04	720	SR191	12	782			844		
039	LFLRO	15	101	07J06	08	163	13D09	05	225	A291	05	287	BMX000	08	349	DIN100	10	411	GND06A	08	473	01W13	14	535	P512J		597	RBA70A	09	659	S171	04	721	SR201	12	783			845		
040	MPYO	14	102	07K08	07	164	13D12	05	226	A301	05	288	BMX010	08	350	DIN110	10	412	GND06B	08	474	02T03	14	536	P512K		598	00D06	10	660	S180	04	722	SR211	12	784			846		
041	PSWI21	13	103	07M08	07	165	13H02	15	227	A311	05	289	BMX020	02	351	DIN120	10	413	GND06C	08	475	02T06	14	537	P512M		599	00E06	10	661	S181	04	723	SR221	12	785			847		
042	PSWI31	13	104	08K02	07	166	13H04	15	228	AC50	10	290	BMX030	08	352	DIN130	10	414	GND06D	08	476	04B09	02	538	P512S		600	00F06	10	662	S190	04	724	SR231	12	786			848		
043	PSWI41	13	105	08K03	07	167	13H06	15	229	AC50A	11	291	BMX040	08	353	DIN140	10	415	GND06E	08	477			539	P512T		601	RD151A	06	663	S191	04	725	SR241	12	787			849		
044	PSWI51	13	106	08K06	07	168	13J03	15	230	ADD1	14	292	BMX050	08	354	DIN150	10	416	GND06F	08	478	02T0E	14	540	P513A		602	00H06	10	664	S200	04	726	SR251	12	788			850		
045	PSWI71	13	107	08K08	07	169	13J06	15	231	00T08	15	293	BMX060	02	355	DIN160	09	417	GND06H	08	479	02T11	15	541	P513B		603	RD171A	06	665	S201	04	727	SR261	12	789			851		
046	PSWI81	13	108	08K11	07	170	13M13	15	232	00T11	14	294	BMX070	08	356	DIN170	09	418	GND06J	08	480	LOAD1	15	542	P5131H		604	00J06	10	666	S21	14	728	SR271	12	790			852		
047	PSWI91	13	109	08M06	07	171	15A06	11	233	AMUXS0	13	295	BMX080	08	357	DIN180	09	419	GND07A	08	481	M1	14	543	P513J		605	00K02	06	667	S210	04	729	SR281	12	791			853		
048	PSW201	13	110	08M08	07	172	15B06	11	234	AMX000	15	296	BMX090	08	358	DIN190	09	420	GND07B	08	482	MPCY1	14	544	P513K		606	00K03	06	668	S211	04	730	SR291	12	792			854		
049	PSW211	13	111	09A06	09	173	15C06	11	235	ASTKS0	13	297	BMX100	03	359	DIN200	09	421	GND07C	08	483	02WI?	06	545	P513M		607	00K06	06	669	S21A	02	731	SR301	12	793			855		
050	PSW231	13	112	09B06	09	174	15D06	11	236	AWE0	10	298	BMX110	08	360	DIN210	09	422	GND07D	08	484	MPY1	14	546	P513S		608	00K08	06	670	S220	04	732	SR311	12	794			856		
051	GPSW251	13	113	09C06	09	175	15E06	11	237	AWEDA	11	299	BMX120	08	361	DIN220	09	423	GND07E	08	485	P08111	02	547	P514C	05	609	00K11	06	671	S221	04	733	S5ELO	08	795			857		
052	GPSW261	13	114	09D06	09	176	15F06	11	238	AYDEN1	06	300	BMX130	08	362	DIN230	09	424	GND07F	08	486	P12151	02	548	P514S	06	610	00M06	06	672	S230	04	734	S5ELOA	09	796			858		
053	GPSW271	13	115	09E06	09	177	15H06	11	239	AYSDEN1	06	301	BMX140	03	363	DIN240	09	425	GND07H	08	487	P16311	02	549	P515K		611	00M08	06	673	S231	04	735	03J08	15	797			859		
054	SH0	14	116	09F06	09	178	15J06	11	240	AYSEN1	06	302	BMX150	08	364	DIN250	09	426	GND07J	08	488	P24271	04	550	P515M		612	00S12	07	674	S240	05	736	6UB1	15	798			860		
055	SR00	12	117	09H06	09	179	15K08	06	241	B001	14	303	BMX160	09	365	DIN260	09	427	GND07S	12	489	P28311	04	551	P516K		613	00S08	06	675	S241	05	737	03J12	15	799			861		
056	SR10	12	118	09J06	09	180	15M08	06	242	B011	08	304	BMX170	09	366	DIN270	09	428	GND08S	12	490	P500K		552	P516M		614	00T06	14	676	S250	05	738	XRP1	06	800			862		
057	STKEN1	06	119	09K02	07	181	16A06	11	243	B021	08	305	BMX180	04	367	DIN280	09	429	GND08T	12	491	P500S		553	03B06	15	615	04B11	02	677	S251	05	739	03W11	14	801			863		
058	ULSRO	12	120	09K03	07	182	16B06	11	244	B031	08	306	BMX190	09	368	DIN290	09	430	GND09A	09	492	P500T		554	03B08	14	616	04B14	02	678	S260	05	740	04B05	02	802			864		
059	YS01	06	121	09K06	07	183	16C06	11	245	B041	02	307	BMX200	09	369	DIN300	09	431	GND09B	09	493	P501K		555	03C07	02	617	04B15	02	679	S261	05	741	04B06	02	803			865		
060	YS11	06	122	09K08	07	184	16D06	11	246	B051	08	308	BMX210	09	370	DIN310	09	432	GND09C	09	494	P501M		556	03C09	02	618	04D04	03	680	S270	05	742	04B07	02	804			866		
061	YS21	06	123	09K11	07	185	16E06	11	247	B061	02	309	BMX220	04	371	01F06	10	433	GND09D	09	495	P501T		557	03C12	02	619	04D07	03	681	S271	05	743	03K08	15	805			867		
062	YS31	06	124	09M06	07	186	16F06	11	248	B071	02	310	BMX230	09	372	DIV1	08	434	GND09E	09	496	P501W		558	03D04	02	620	5000	08	682	S280	05	744	03K12	02	806			868		

NOTES
1 CROSS REF. LIST OF MNEMONICS REFLECTS THE SCHEMATIC
NOT THE MULTIWIRE LISTING

REVISIONS

SCALE—

TOLERANCE
XXX ± .005
XX ± .02
X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
B STINE	DRAFT	10-30-78
RCERO	CHK	
GJOYCE	ENGR	
PAINERCE		
N. LEMONDE		

TITLE MULTIWIRE CPU-13
CROSS REF.

DWG NO. 35-768 D08

SHEET OF 16—16

CABLE CONNECTOR MAP

CONN	TERM. NO.	ROW 2	ROW 1
6	16		
	15		
	14		
	13		
	12		
	11		
	10		
	09		
	08		
	07		
	06		
	05		
	04		
	03		
	02		
	01		
	00		
5	24	GND	GND
	23		
	22		
	21		
	20		
	19		
	18		
	17		CWRØ
	16	MDHSAI	ENMAAØ
	15	CAMAØ	PA30I
	14	MDR$Ø	DISEXTØ
	13	LHWRTØ	LWRTØ
	12	PSBCØ	MSBCØ
	11	PMEMI	MFAULTØ
	10	MDLCKØ	MDHCKØ
	09	MDSBØ	MDLSAI
	08		HALTØ
	07	GND	GND
	06	FSCLKI	FSCLKØ
	05	GND	GND
	04	LPSTDØ	LSSTDØ
	03	CLSTAØ	MATSTOPØ
	02	RFAULTØ	MARSTPØ
	01	ILOCØ	IMARØ
	00	GND	GND
4	24	GND	GND
	23	S011	S001
	22	S031	S021
	21	GND	GND
	20	S051	S041
	19	S071	S061
	18	GND	GND
	17	S091	S081
	16	S111	S101
	15	GND	GND
	14	S131	S121
	13	S151	S141
	12	GND	GND
	11	S171	S161
	10	S191	S181
	09	GND	GND
	08	S211	S201
	07	S231	S221
	06	GND	GND
	05	S251	S241
	04	S271	S261
	03	GND	GND
	02	S291	S281
	01	S311	S301
	00	GND	GND
3	16		
	15		
	14		
	13		
	12		
	11		
	10	GND	GND
	09	GND	GND
	08		
	07		
	06		
	05		
	04		
	03		
	02		
	01		
	00		

FROM	TO	SHT
16A12	16A44	13
16A10	16A12	13
16A09	16A10	13
16A08	16A09	13
16A05	16A08	13
16A03	16A05	13
16A02	16A03	13

STRAPPING INFORMATION

PART NO.	REF DESIGNATION	SPARE OUTPUT NO.
19-055	01B	11
19-055	19B	03,06
19-236	20J	11
19-236	15R	06
19-236	10K	11
19-236	05H	11
19-235	00A	08,11
19-234	19F	01
19-127	19H	08,11
19-126	14C	08
19-126	09E	08
19-124	23K	08,11
19-124	12H	11
19-064	10C	07
19-063	04D	08
19-060	11C	08
19-059	03B	06,08
19-059	01C	08
19-059	00R	08
19-058	20H	08
19-058	10R	08,12
19-058	06B	06
19-058	04C	12
19-057	22D	02,10,12
19-057	18A	02,04,06
19-057	11R	12
19-057	04H	02,04,06,08
19-057	02H	02
19-057	02B	02,04,08
19-057	01D	04,06
19-124	22K	06
19-055	18B	11
19-055	16H	08
19-055	13R	11
19-055	11H	11
19-055	06C	03,06,08
19-055	01R	03,06,08
19-055	00B	03,11

BACK PANEL MAP

CONN	TERM. NO.	ROW 1	ROW 2
2	43	GND	GND
	42		
	41		
	40		
	39		
	38		
	37		
	36		
	35		
	34	GND	GND
	33	GND	GND
	32		
	31		
	30		
	29		
	28		
	27		
	26		
	25		
	24	GND	GND
	23	GND	GND
	22		MATRSDØ
	21		MATRSRØ
	20	GND	GND
	19	GND	GND
	18	MDS30Ø	MDS31Ø
	17	MDS28Ø	MDS29Ø
	16	MDS26Ø	MDS27Ø
	15	MDS24Ø	MDS25Ø
	14	MDS22Ø	MDS23Ø
	13	MDS20Ø	MDS21Ø
	12	MDS18Ø	MDS19Ø
	11	MDS16Ø	MDS17Ø
	10	GND	GND
	09	GND	GND
	08	MDS14Ø	MDS15Ø
	07	MDS12Ø	MDS13Ø
	06	MDS10Ø	MDS11Ø
	05	MDS08Ø	MDS09Ø
	04	MDS06Ø	MDS07Ø
	03	MDS04Ø	MDS05Ø
	02	MDS02Ø	MDS03Ø
	01	MDS00Ø	MDS01Ø
	00	GND	GND

BACK PANEL MAP

CONN	ROW 1	ROW 2	TERM. NO.
1	GND	GND	43
			42
			41
			40
			39
			38
			37
			36
			35
	GND	GND	34
	GND	GND	33
			32
			31
			30
		RD27I	29
	RD25I	RD26I	28
	RD24Ø	RD12I	27
	RD14I	RD13I	26
	RD15Ø	RD16I	25
	GND	GND	24
	GND	GND	23
	RD00I	RD01I	22
	RD02I	RD03I	21
	GND	GND	20
	GND	GND	19
		RD02Ø	18
			17
		PSW2II	16
	PSWI0I	PSWIII	15
			14
		MSTOPØ	13
		DSTOPØ	12
			11
	GND	GND	10
	GND	GND	09
			08
	SCLRØ		07
			06
		MCLKI	05
			04
		DEXTØ	03
	EXBØ	DEXBØ	02
	ALGNØ	MATØ	01
	GND	GND	00
0	GND	GND	43
	B00I	B01I	42
	B02I	B03I	41
	B04I	B05I	40
	B06I	B07I	39
	B08I	B09I	38
	B10I	B11I	37
	B12I	B13I	36
	B14I	B15I	35
	GND	GND	34
	GND	GND	33
	B16I	B17I	32
	B18I	B19I	31
	B20I	B21I	30
	B22I	B23I	29
	B24I	B25I	28
	B26I	B27I	27
	B28I	B29I	26
	B30I	B31I	25
	GND	GND	24
	GND	GND	23
			22
	CLKIC	SCLKI	21
	GND	GND	20
	GND	GND	19
		FNCEØ	18
	DUAØ	PSELI	17
			16
			15
	LMA30Ø	LMA31Ø	14
	LMA28Ø	LMA29Ø	13
	LMA26Ø	LMA27Ø	12
	LMA24Ø	LMA25Ø	11
	GND	GND	10
	GND	GND	09
	LMA22Ø	LMA23Ø	08
	LMA20Ø	LMA21Ø	07
	LMA18Ø	LMA19Ø	06
	LMA16Ø	LMA17Ø	05
	LMA14Ø	LMA15Ø	04
	LMA12Ø	LMA13Ø	03
	LMA10Ø	LMA11Ø	02
	LMA08Ø	LMA09Ø	01
	GND	GND	00

35-769 R05
BOARD REV LEVEL

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL.

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

REVISION	3			3		2	2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25

USED IN MANUAL;

IBRUNING 44-131 40579

REVISIONS

PRE PRODUCTION APPROVAL — INIT DEV Gml — DATE 9/16/80

SPARE OUTPUT PIN 01 ON 14H WAS REMOVED.
REVISED AREA N9 & R9
REVISED REV. BLOCK IN AREA A9.
REVISED SHTS. 1,5,8,9,11,15,19, & 25.

E.C.J.		4494	M	10-23-80	R01

RELEASED FOR PRODUCTION
ENG. _____ DATE 11/17/80

REVISED SHTS 1,5,8,9,10

JAT		4623	D	2-27-81	R02

DELETED: "19-234 14H 10,13" FROM SPARE GATE TABLE, AREA M9: BOARD REV LEVEL WAS R01. REVISED "STRAPPING INFORMATION" TO ADD 16AD9. REVISED SHT 1, 5 & 13

JV		4907	MS	12-28-81	R03	X

UNLESS OTHERWISE SPECIFIED

SCALE: — TOLERANCE:
DIMENSIONS ARE IN INCHES — .XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME	TITLE	DATE
E. JOHNSON	DES/DFT	11-19-80
R. CERO	SUPV	11-19-80
	CHK	11-19-80
E. MARCH	ENG	11-19-80
D. FRANKENBERGER	MGR	11-19-80
R. BARKER	QC	11-19-80

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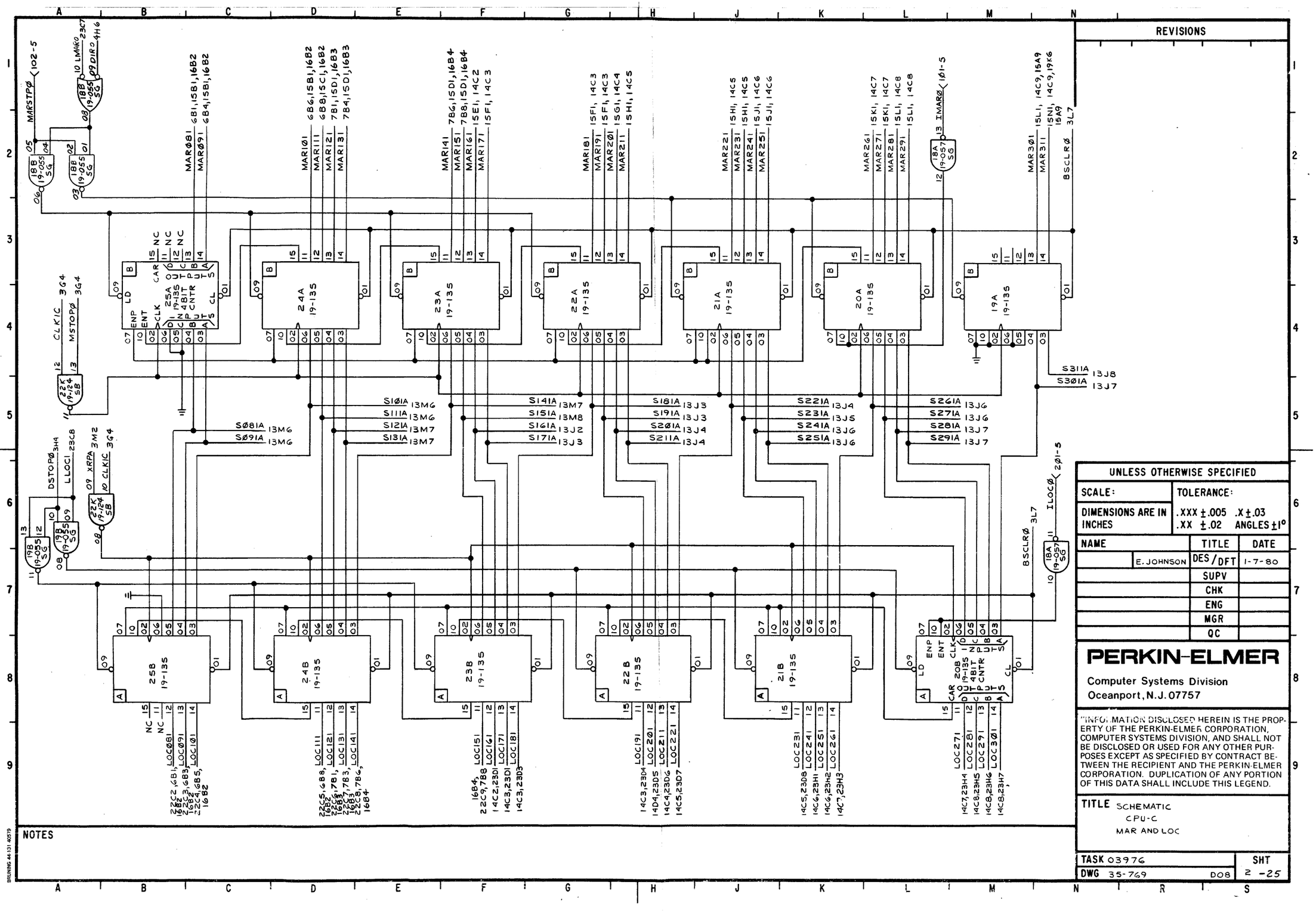
Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C

TASK 03976	SHT
DWG 35-769 R03 D08	1 - 25



REVISIONS

NOTES

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	E. JOHNSON	DES/DFT	1-7-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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TITLE SCHEMATIC
CPU-C
MAR AND LOC

TASK 03976 | SHT 2-25
DWG 35-769 D08

REVISIONS

14M 19-233 A
13M 19-233 A
12M 19-233 A
09H 19-231 DREG
11J 19-117 4-BIT MAG COMP
10J 19-117 4BIT MAG COMP.
DATA IN
DATA OUT
A<B A=B A>B
XRPA M2
MCLK1 2B5-1
MSTOP0 2A4
CLK1C 2A4
SCLK1 9A6
DSTOP0 2A6
LPSTD0 2B15
LPSTDI 5G9
LPSTDCK0 9A3
DCLK1 H7
SCLR0C 10F7-1
GETSSTEI 9NG
EPSTDI A2
TYPICAL 'A' BOX CONFIGURATION 3 PLACES

UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ±.005 .XX ±.02	.X ±.03 ANGLES ±1°
NAME	TITLE	DATE
A.WILLIAMS	DES/DFT	2-11-80
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

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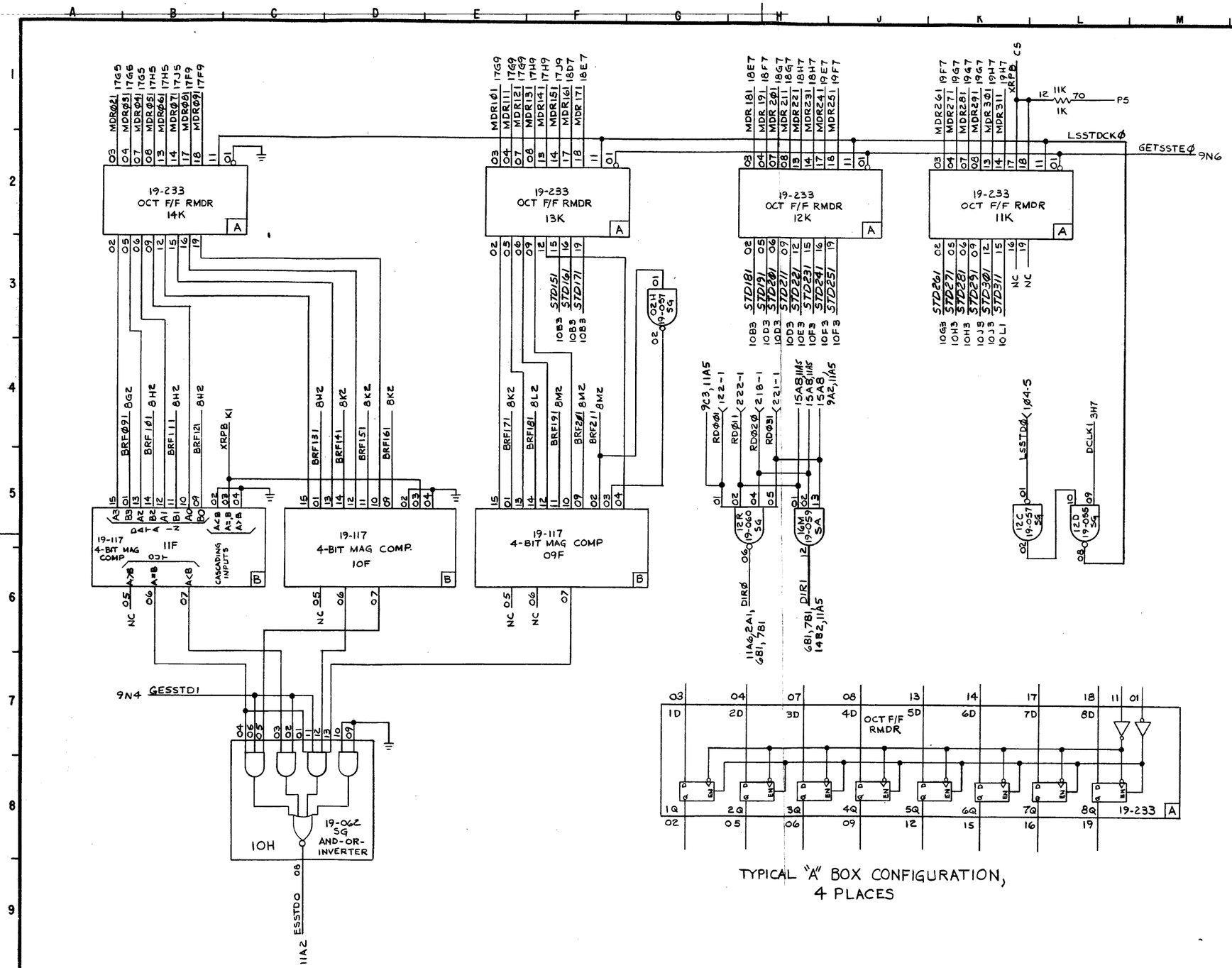
TITLE SCHEMATIC
CPU-C
PROCESS SEGMENT TABLE DESCRIPTOR AND SEGMENT SIZE COMPARITOR

TASK 03976 | SHT
DWG 35-729 D08 | 3 -25

NOTES



REVISIONS

UNLESS OTHERWISE SPECIFIED			
SCALE:		TOLERANCE:	
DIMENSIONS ARE IN INCHES		.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME		TITLE	DATE
	A. WILLIAMS	DES / DFT	2-11-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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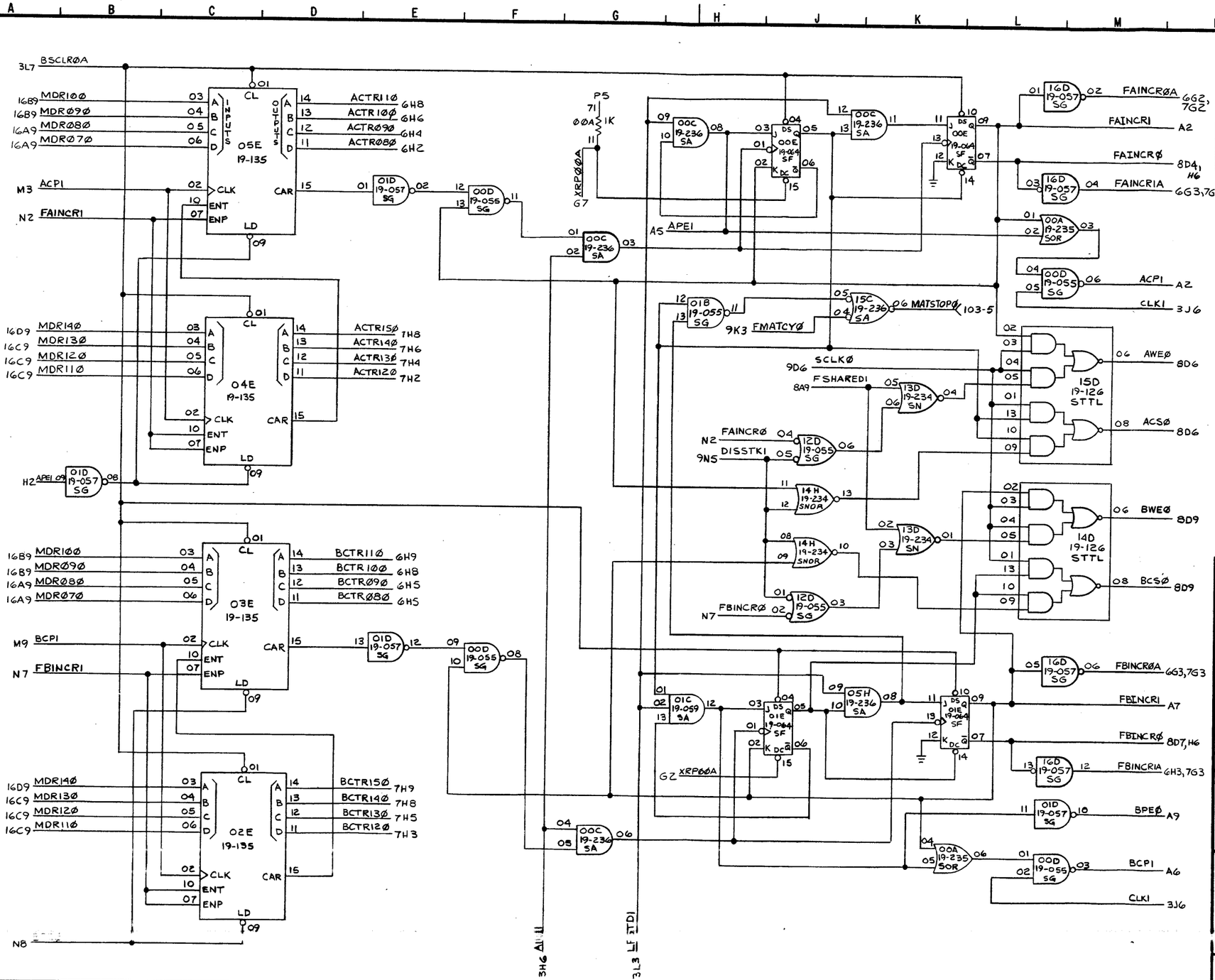
TITLE SCHEMATIC
CPU-C
SHARED SEGMENT TABLE DESCRIPTOR AND SHARED SEGMENT SIZE COMPARITOR

TASK 03976
DWG 35-769 D08
SHT 4 -25

NOTES



REVISIONS					
REV. 15C TO ALT. LOGIC SYMBOL IN AREA J3					
E.C. J	[illegible]	9494	M	10-23-80	R01
AREA N8; REF 6H3 WAS 6C3					
JAT	[illegible]	9623	D	2-27-81	R02
EXTENSIVE CHANGES: FOR PREVIOUS REVISION SEE R02 MICROFILM. ADDED 2 SPARE GATES (14H 13 & 14H10) AREA J5.					
JLV	[illegible]	4907	MS	12-28-81	R03 X

UNLESS OTHERWISE SPECIFIED			
SCALE:		TOLERANCE:	
DIMENSIONS ARE IN INCHES		.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME		TITLE	DATE
	A. WILLIAMS	DES/DFT	2-7-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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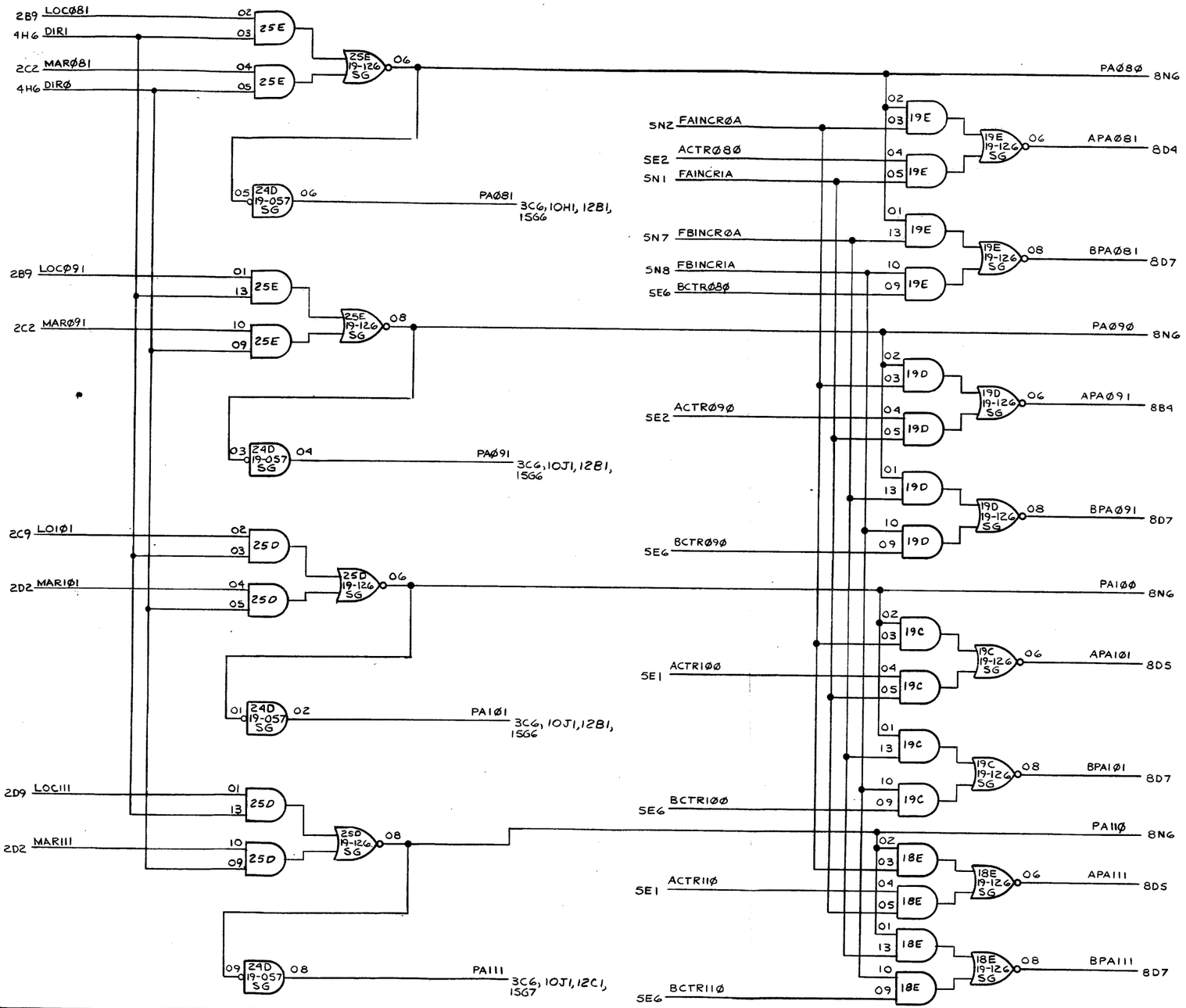
TITLE
SCHEMATIC
CPU-C
PRESENCE BIT INITIALIZATION

TASK 03976	SHT
DWG 35-769 RC3 D08	5 -25

NOTES



REVISIONS

NOTES

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	A.WILLIAMS	DES/DFT	2-7-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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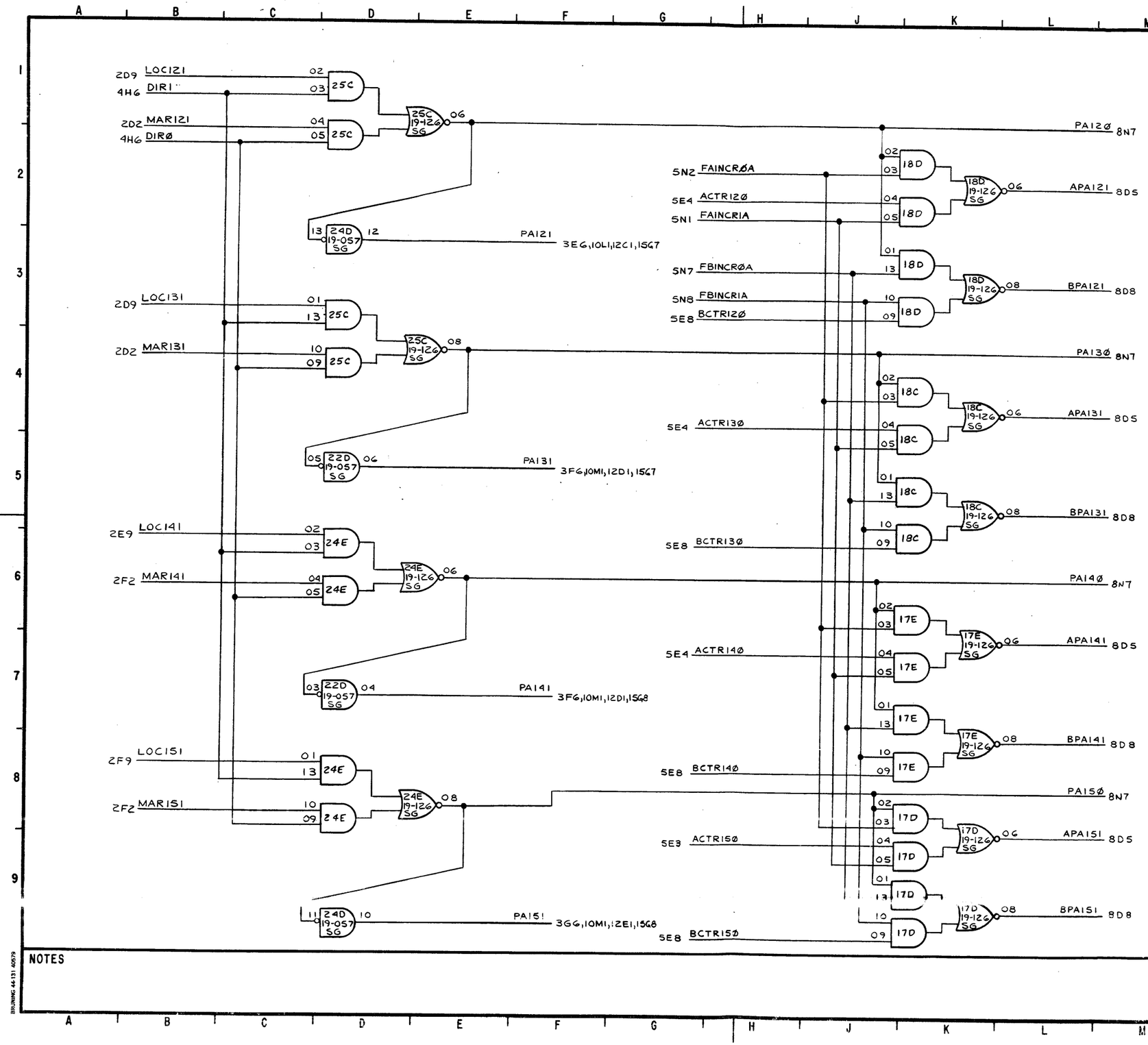
TITLE SCHEMATIC
CPU-C
PA LATCH 8-11

TASK 03976 SHT 6-25
DWG 35-769 D08



REVISIONS

NOTES

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	E.JOHNSON	DES/DFT	1-24-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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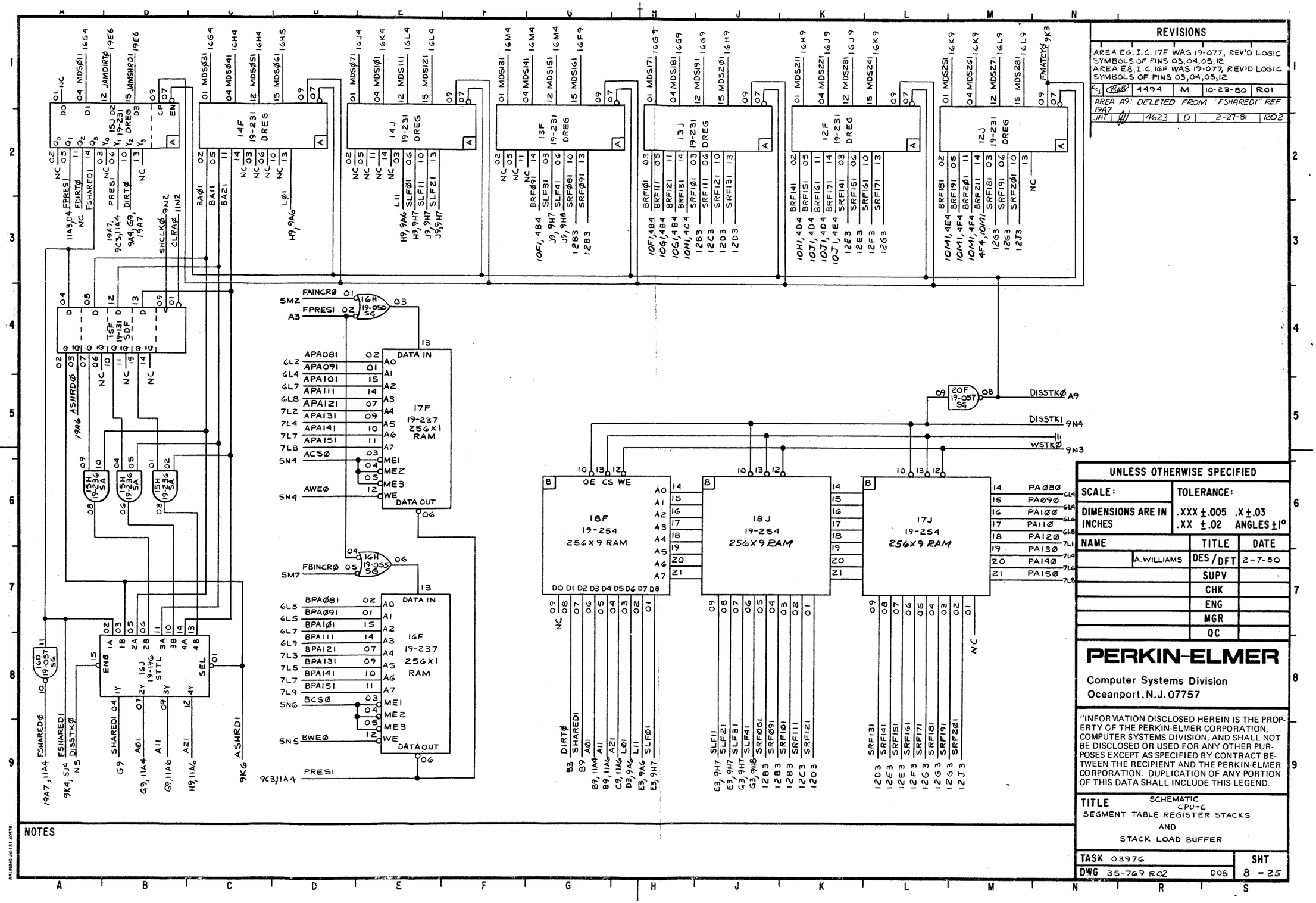
TITLE
SCHEMATIC
CPU-C
PA LATCH 12-15

TASK 03976
DWG 35-769 D08
SHT 7 -25


REVISIONS
AREA E6, I.C. 17F WAS 19-077, REV'D LOGIC SYMBOLS OF PINS 03,04,05,12
AREA E8, I.C. 16F WAS 19-077, REV'D LOGIC SYMBOLS OF PINS 03,04,05,12
EJ | 4494 | M | 10-23-80 | R01
AREA A9: DELETED FROM "FSHAREDI" REF 19A7
JAT | 4623 | D | 2-27-81 | R02
14F 19-231 DREG
14J 19-231 DREG
13F 19-231 DREG
13J 19-231 DREG
12F 19-231 DREG
12J 19-231 DREG
15F 19-131 SDF
16J 19-196 STTL
17F 19-237 256X1 RAM
16F 19-237 256X1 RAM
18F 19-254 256X9 RAM
18J 19-254 256X9 RAM
17J 19-254 256X9 RAM
DISSTKØ A9
DISSTKI 9N4
WSTKØ 9N3
UNLESS OTHERWISE SPECIFIED
SCALE:
TOLERANCE:
DIMENSIONS ARE IN INCHES
.XXX ±.005 .X ±.03
.XX ±.02 ANGLES ±1°
NAME | TITLE | DATE
A. WILLIAMS | DES/DFT | 2-7-80
SUPV
CHK
ENG
MGR
QC
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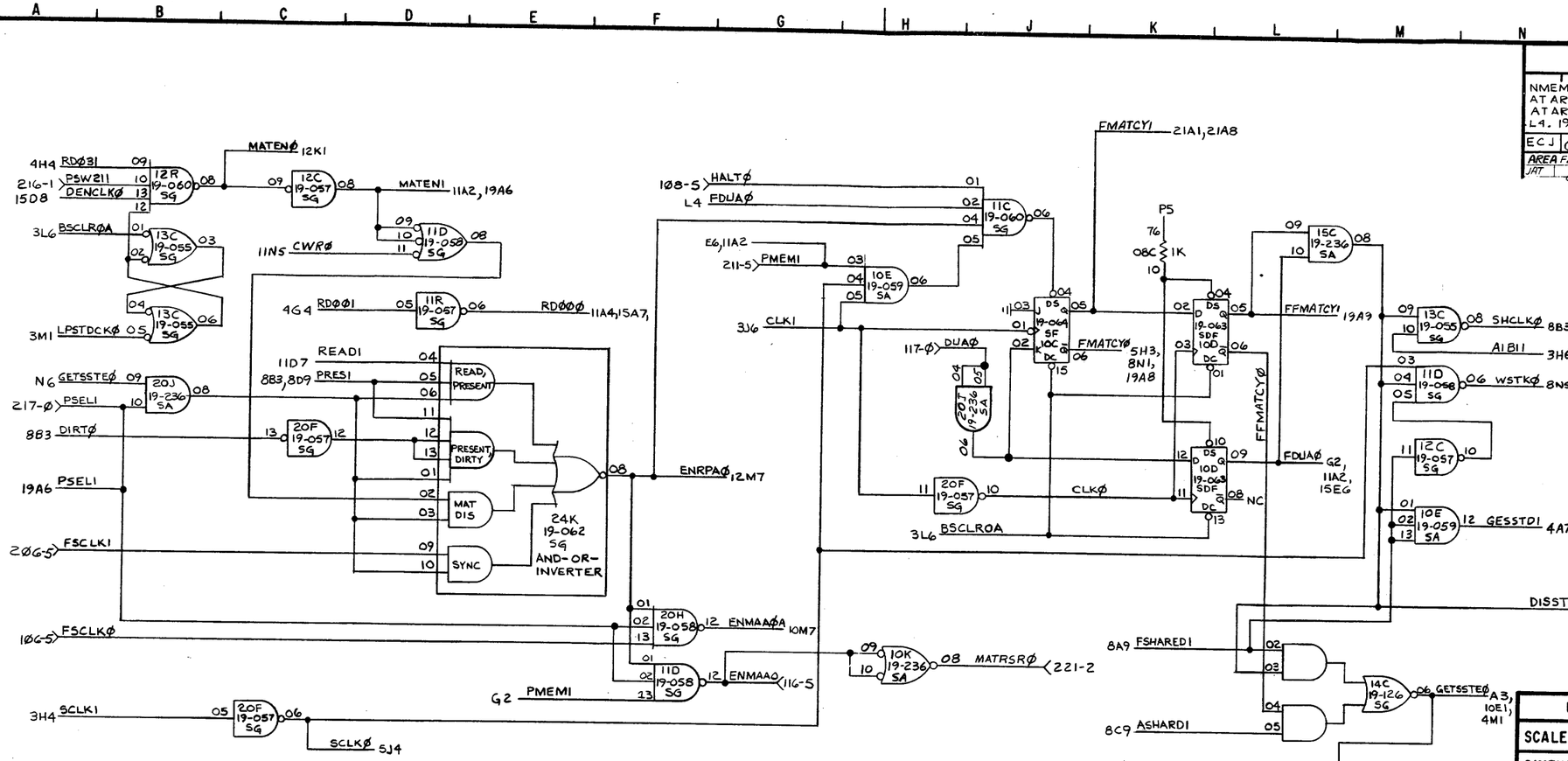
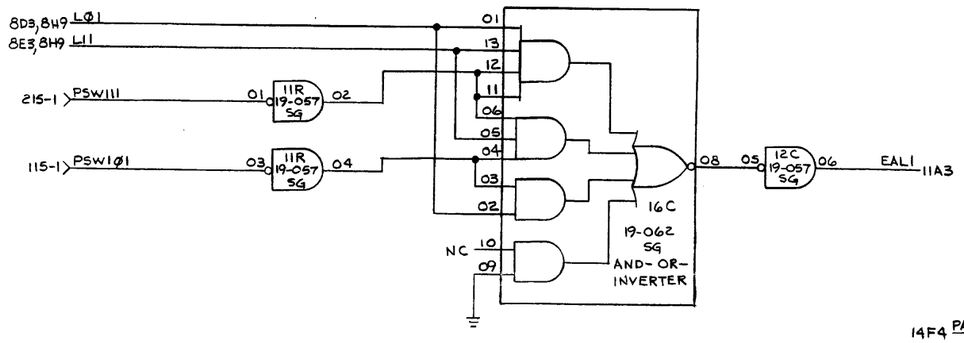
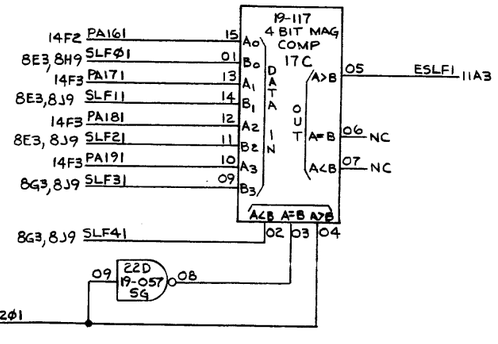
Oceanport, N.J. 07757
"INFORMATION DISCLOSED HEREIN IS THE PROPERTY OF THE PERKIN-ELMER CORPORATION, COMPUTER SYSTEMS DIVISION, AND SHALL NOT BE DISCLOSED OR USED FOR ANY OTHER PURPOSES EXCEPT AS SPECIFIED BY CONTRACT BETWEEN THE RECIPIENT AND THE PERKIN-ELMER CORPORATION. DUPLICATION OF ANY PORTION OF THIS DATA SHALL INCLUDE THIS LEGEND.
TITLE SCHEMATIC CPU-C
SEGMENT TABLE REGISTER STACKS
AND
STACK LOAD BUFFER
TASK 03976
SHT 8 - 25
DWG 35-769 R02 D08
NOTES
BRUNING 44-131 40579

REVISIONS				
NMEMONIC "READI" WAS ADDED TO PIN 24K09 AT AREA D3. PIN 24K09 WAS CONN. TO 11R05 AT AREA D3. 15E6 WAS ADDED TO "FDUAØ" AT L4. 19A6 WAS REMOVED FROM "RDØØØ" AT E3.				
ECJ	[signature]	4494	M	10-23-80 R01
AREA F2: DELETED FROM PMEMI REF 15E6.				
JAT	JV	4623	D	2-27-81 R02





ACCESS LEVEL DETECTION



SEGMENT LIMIT DETECTION

UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ±.005	.X ±.03
	.XX ±.02	ANGLES ±1°

NAME	TITLE	DATE
A. WILLIAMS	DES/DFT	2-11-80
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

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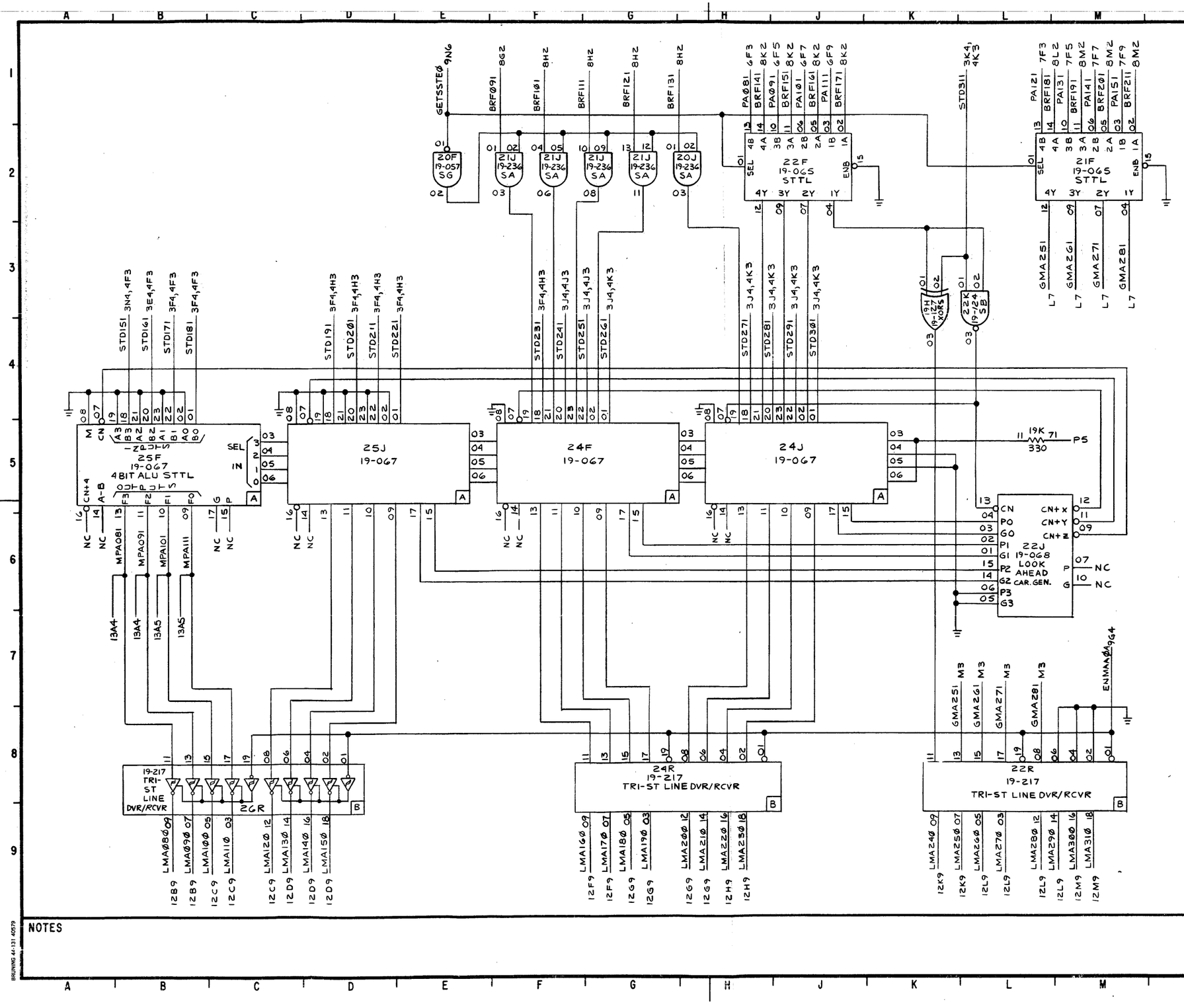
TITLE SCHEMATIC
CPU-C
MAT CONTROL

TASK 03976 | SHT 9 -25

DWG 35-769 R02 D08

NOTES



REVISIONS				
AREA F6: IC 24F PIN 14 WAS PIN 04.				
JAT	4623	D	2-27-81	R01

NOTES

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	A. WILLIAMS	DES / DFT	2-7-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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TITLE SCHEMATIC
CPU-C
MAT RELOCATION SUMMER AND LMA DRIVERS

TASK 03976	SHT
DWG 35-769 R01 D08	10 -25

REVISIONS				
I.C. 14H 19-234 SN AT D7 WAS ADDED.				
ECJ	[illegible]	4494	M	10-23-80	R01

MAT FAULT CODES			
EMAT29Ø	EMAT3Ø1	EMAT311	
0	0	0	ACCESS MODE FAULT – EXECUTE PROTECTED
0	0	1	ACCESS MODE FAULT – WRITE PROTECTED
0	1	0	ACCESS MODE FAULT – READ PROTECTED
0	1	1	ACCESS LEVEL FAULT
1	0	0	SEGMENT LIMIT FAULT
1	0	1	NON-PRESENT SEGMENT FAULT
1	1	0	SST – SIZE EXCEEDED
1	1	1	PST – SIZE EXCEEDED

NOTE: THE MICRO-PROCESSOR ADDS X'1' TO THE MAT FAULT CODE IN REGISTER 13.

MAT FAULT

UNLESS OTHERWISE SPECIFIED			
SCALE:		TOLERANCE:	
DIMENSIONS ARE IN INCHES		.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME		TITLE	DATE
	A.WILLIAMS	DES/DFT	2-7-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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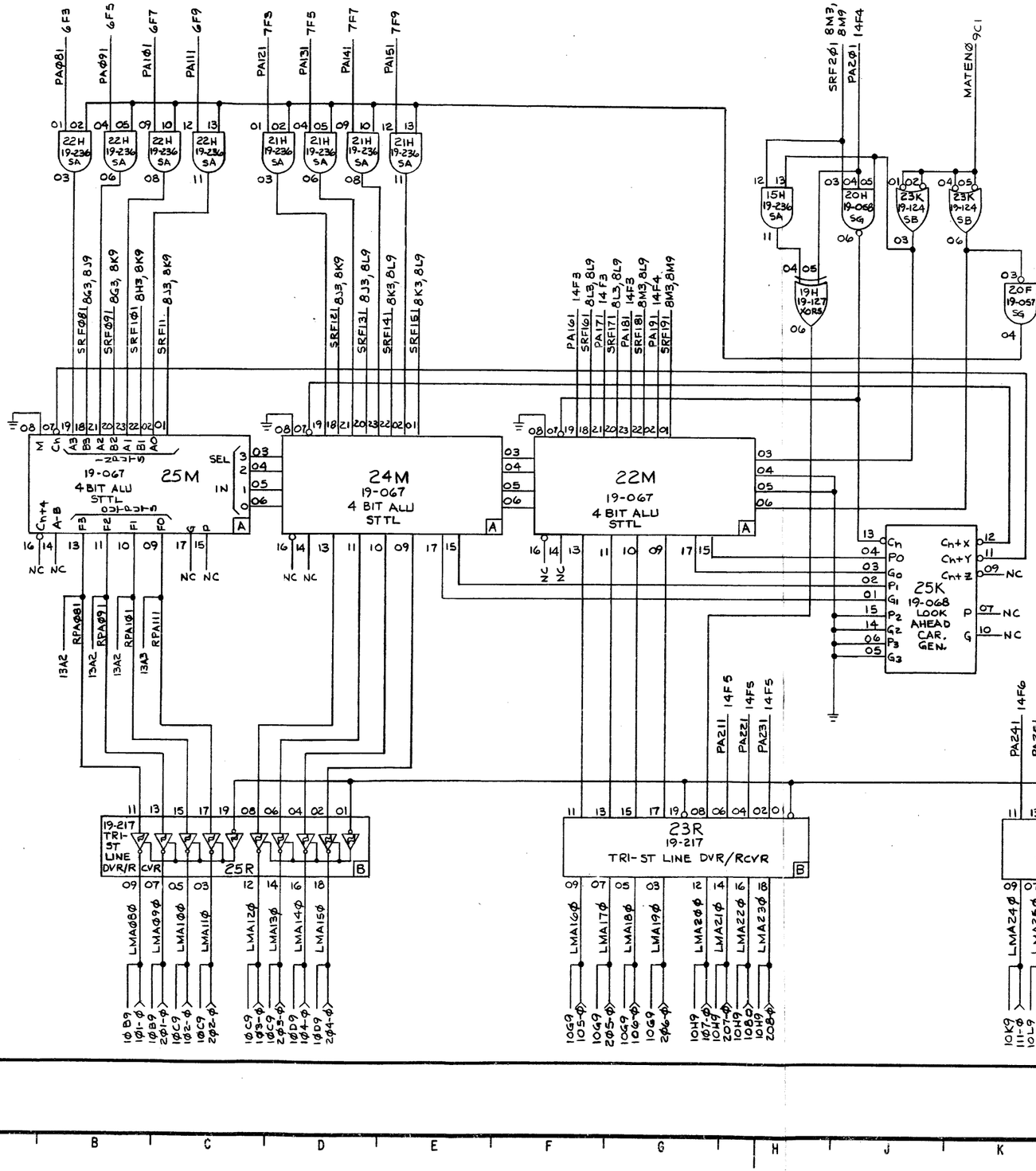
TITLE SCHEMATIC
CPU-C
MAT FAULT DECODE

TASK 03976 SHT 11 – 25
DWG 35-769 R01 D08

NOTES



NOTES

BRUNING 44-131 40579

REVISIONS

UNLESS OTHERWISE SPECIFIED,	
SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
	A.WILLIAMS	DES/DFT	1-30-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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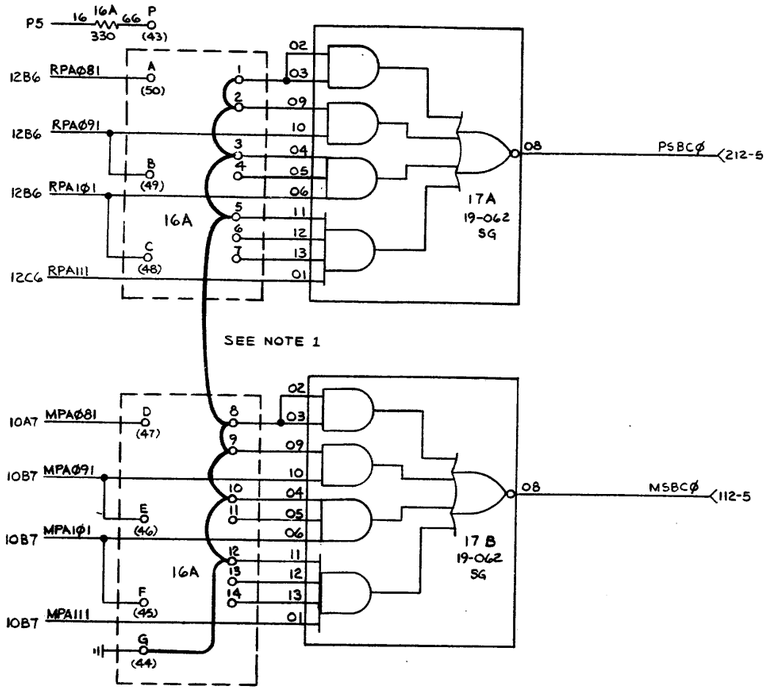
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
PROGRAM ADDRESS RELOCATION
SUMMER LMA DRIVERS

TASK 03976
DWG 35-769 D08
SHT 12 - 25



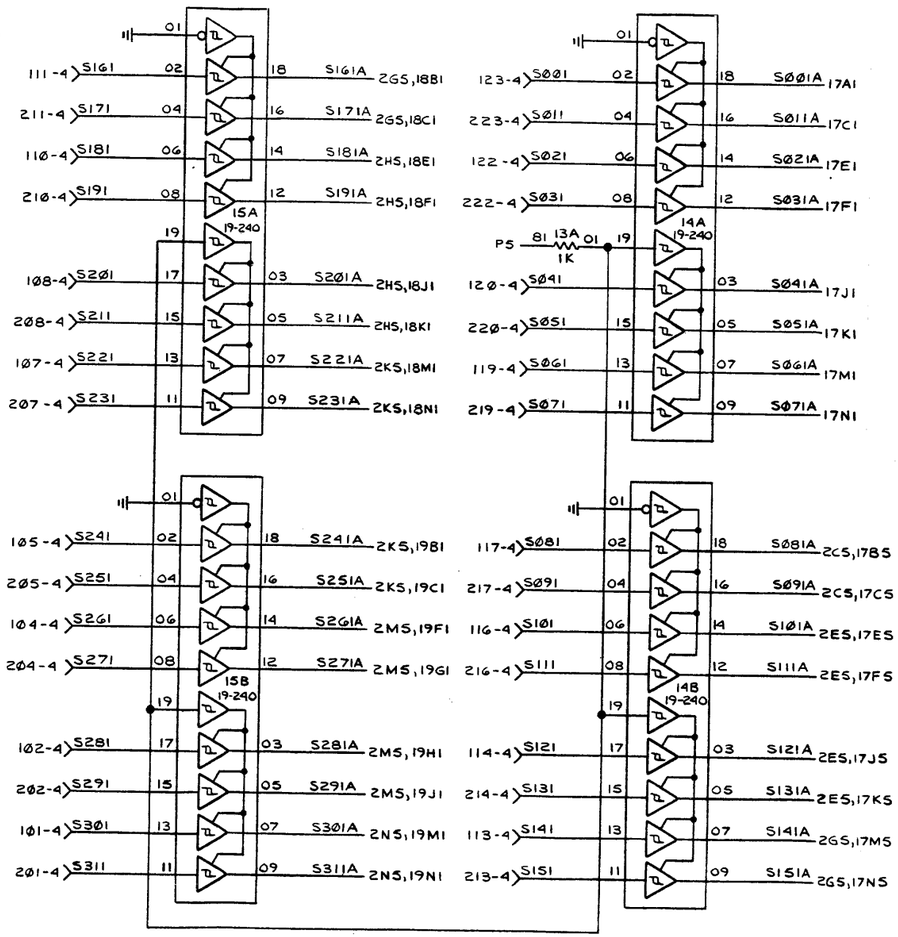


TABLE 1 SHARED/MEMORY STRAPPING

TEST POINTS	MEGA BYTES OF SHARED MEMORY															
	Ø	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	G	G	G	G	G	G	G	G	A	A	A	A	A	A	A	A	P
2	G	G	G	G	A	A	A	A	G	G	G	G	P	P	P	P	G
3	G	G	A	A	G	G	A	A	G	G	P	P	G	G	P	P	G
4	NC	NC	B	B	NC	NC	P	P	NC	NC	B	B	NC	NC	P	P	NC
5	G	A	G	A	G	A	G	A	G	P	G	P	G	P	G	P	G
6	NC	B	NC	B	NC	P	NC	P	NC	B	NC	B	NC	P	NC	P	NC
7	NC	C	NC	P	NC	C	NC	P	NC	C	NC	P	NC	C	NC	P	NC
8	G	G	G	G	G	G	G	G	D	D	D	D	D	D	D	D	P
9	G	G	G	G	D	D	D	D	G	G	G	G	P	P	P	P	G
10	G	G	D	D	G	G	D	D	G	G	P	P	G	G	P	P	G
11	NC	NC	E	E	NC	NC	P	P	NC	NC	E	E	NC	NC	P	P	NC
12	G	D	G	D	G	D	G	D	G	P	G	P	G	P	G	P	G
13	NC	E	NC	E	NC	P	NC	P	NC	E	NC	E	NC	P	NC	P	NC
14	NC	E	NC	E	NC	E	NC	E	NC	E	NC	E	NC	E	NC	E	NC

NOTE: NC = NO CONNECTION

NOTES 1. STRAPPING IS SHOWN FOR AN ALL LOCAL MEMORY SYSTEM, NO SHARED MEMORY. SEE TABLE 1 FOR LOCAL/SHARED MEMORY STRAPPING.

REVISIONS					
ADDED STRAP FROM PIN 9 (16A) TO 16A08 & 16A10 (GND)					
JLV	JV	4907	MS	12-28-81	A01

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	E. JOHNSON	DES/DFT	
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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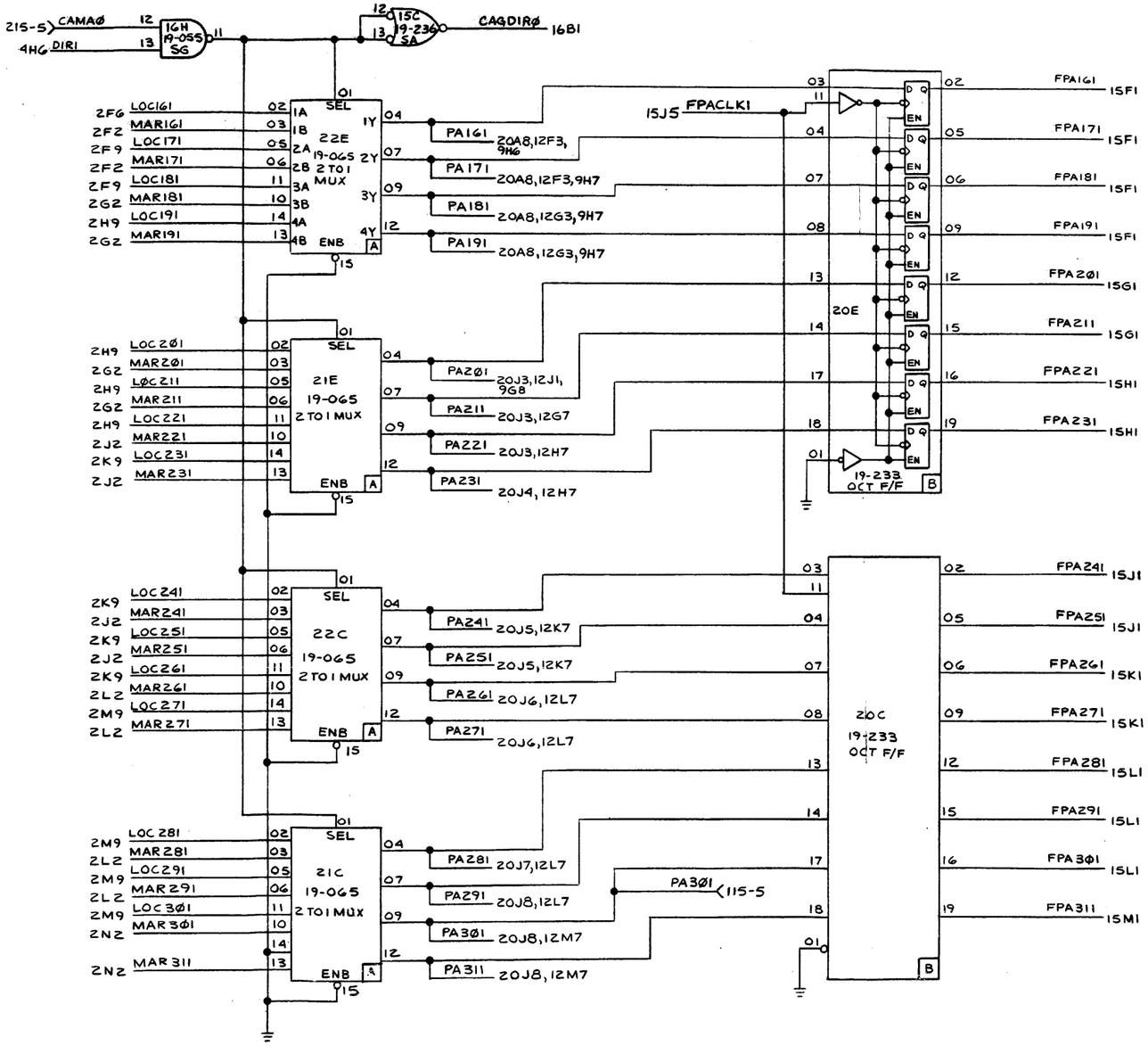
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
LOCAL/SHARED MEMORY DETECTION

TASK 03976
DWG 35-769 R01 DOB
SHT 13 -25



NOTES

REVISIONS

UNLESS OTHERWISE SPECIFIED	
SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME	TITLE	DATE
E. JOHNSON	DES / DFT	1-28-80
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
PROGRAM ADDRESS MULTIPLEXOR AND LATCH

TASK 03976	SHT
DWG 35-769 D08	14 - 25

REVISIONS					
PIN 10E10 AT F6 WAS PMEM1, 9G2					
ECJ	[illegible]	4494	M	10-23-80	R01

EIMARI
EIMARØ

FPACLKI 14G2

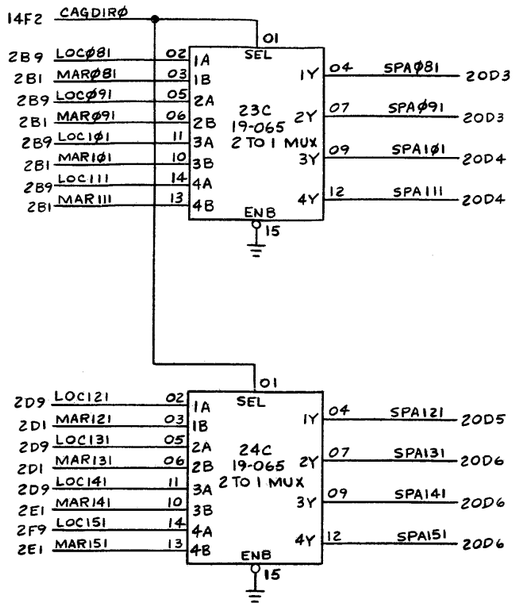
NOTES

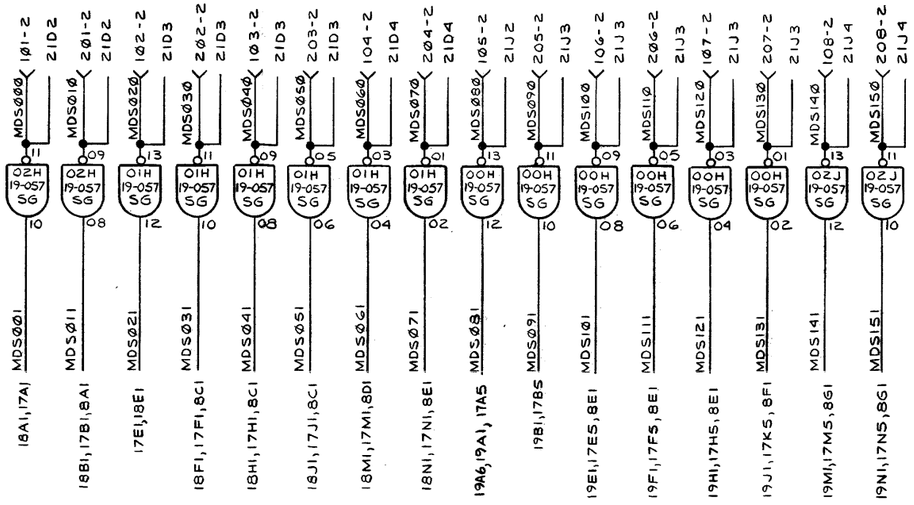
UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	E. JOHNSON	DES / DFT	1-28-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

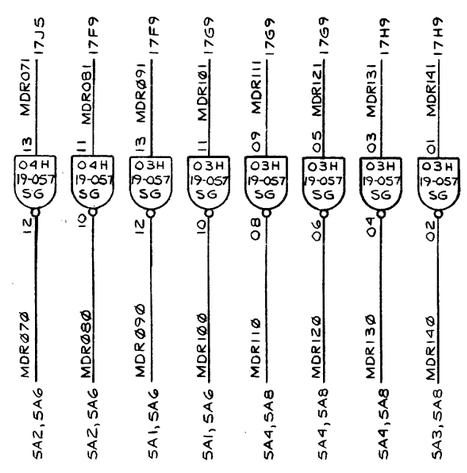
PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

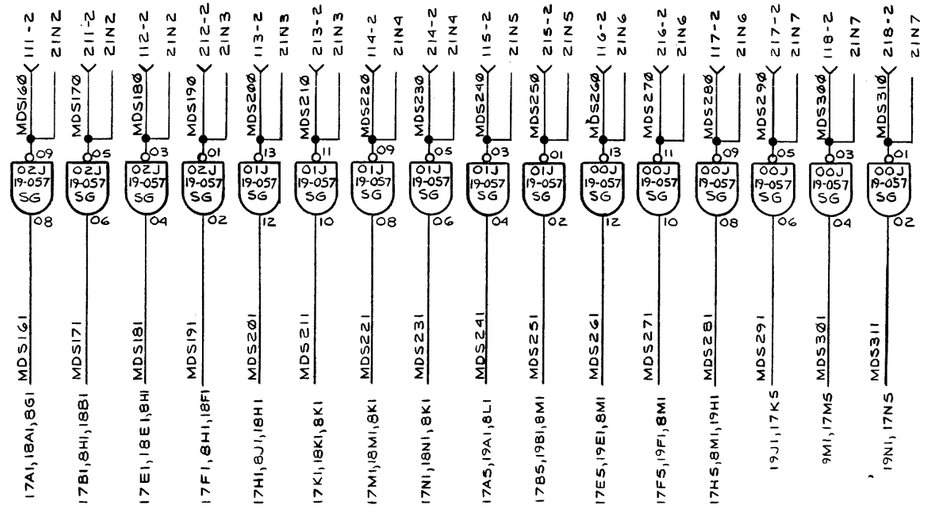
TITLE SCHEMATIC
CPU-C ZMAR

TASK 03976	SHT
DWG 35-769 R01 D08	15 - 25









NOTES

REVISIONS

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
		DES/DFT	
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
MDS BUFFERS

TASK 03976
DWG 35-769 D08
SHT 16-25

PERKIN ELMER
Computer Systems Division
Oceanport N.J. 07757

REVISIONS

09K 19-116 STTL
08K 19-116 STTL
07K 19-116 STTL
06K 19-116 STTL
09M 19-116 STTL
08M 19-116 STTL
07M 19-116 STTL
06M 19-116 STTL
05K 19-233 OCT F/F RMD3
05M 19-233 OCT F/F RMD3

B	A	MDR 0/15 MUX
0	0	EMD
0	1	OMS
1	0	MAT FAULT

SCALE-	NAME	TITLE	DATE
TOLERANCE XXX ± .005 XX ± .02 X ± .03 ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	A. WILLIAMS	DRAFT	2-11-80
		CHK	
		ENGR	

TITLE SCHEMATIC CPU-C PROCESSOR MDR BITS 0-15

CODE NO. 03976 SIZE D DWG NO. 35-769 D08 SHEET OF 17-25

PERKIN ELMER

Computer Systems Division
Teterboro, N.J. 07757

REVISIONS

B	A	MDR 16-23 DATA MUX
0	0	EMD
0	1	OMS
1	0	MAT FAULT
1	1	SBUS

SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	A. WILLIAMS	DRAFT	2-11-80
		CHK	
		ENGR	

TITLE CPU-C
PROCESSOR MDR BITS 16-23

TASK NO. 03976
DWG. NO. 35-769 D08
SHEET 18 OF 25

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
PIN 11M03 AT A6 WAS RD000, 11E6.				
LTR	ECO	4494	M	10-23-80	R01

MD5081 16K4
MD5241 16K9
S241A 13J6
MDLCA1 18B1
MD5818 18B1
MD5091 16K4
MD5251 16K9
S251A 13J6
19-116 STTL 04M
1Y 2Y

MD5101 16K4
MD5261 16K9
S261A 13J6
MD5111 16L4
MD5271 16L9
S271A 13J6
19-116 STTL 03M
1Y 2Y

MD5121 16L4
MD5281 16L9
S281A 13J7
19-116 STTL 02M
1Y 2Y

MD5131 16M4
MD5291 16M9
EMAT291 11M7
S291A 13J7
MD5141 16M4
MD5301 16M9
EMAT301 11M8
S321A 13J7
19-116 STTL 01M
1Y 2Y

MD5151 16M4
MD5311 16M9
EMAT311 11M9
S311A 13J8

18R1 MDLCKØ 09
R6 DISB1 10
09J 19-235 SOR 08

8A5 ASHRDØ
16K4 MDS Ø81
9A4 PSELI
9D2 MATENI
11E6 READØ
11M 19-059 SA 12
8B3 DIRTØ
8A9 FSHAREDØ
8B3 PRESI
15B6 XRPD
9K3 FMATCYØ
9M3 FFMATCYI
09D 19-063 SDF
10M 19-062 SG
10K 19-236 SA 03
JAMSHRDI 8B1
09J 19-235 SOR 03
JAMDIRTØ 8B1
MATRSDØ 222-2

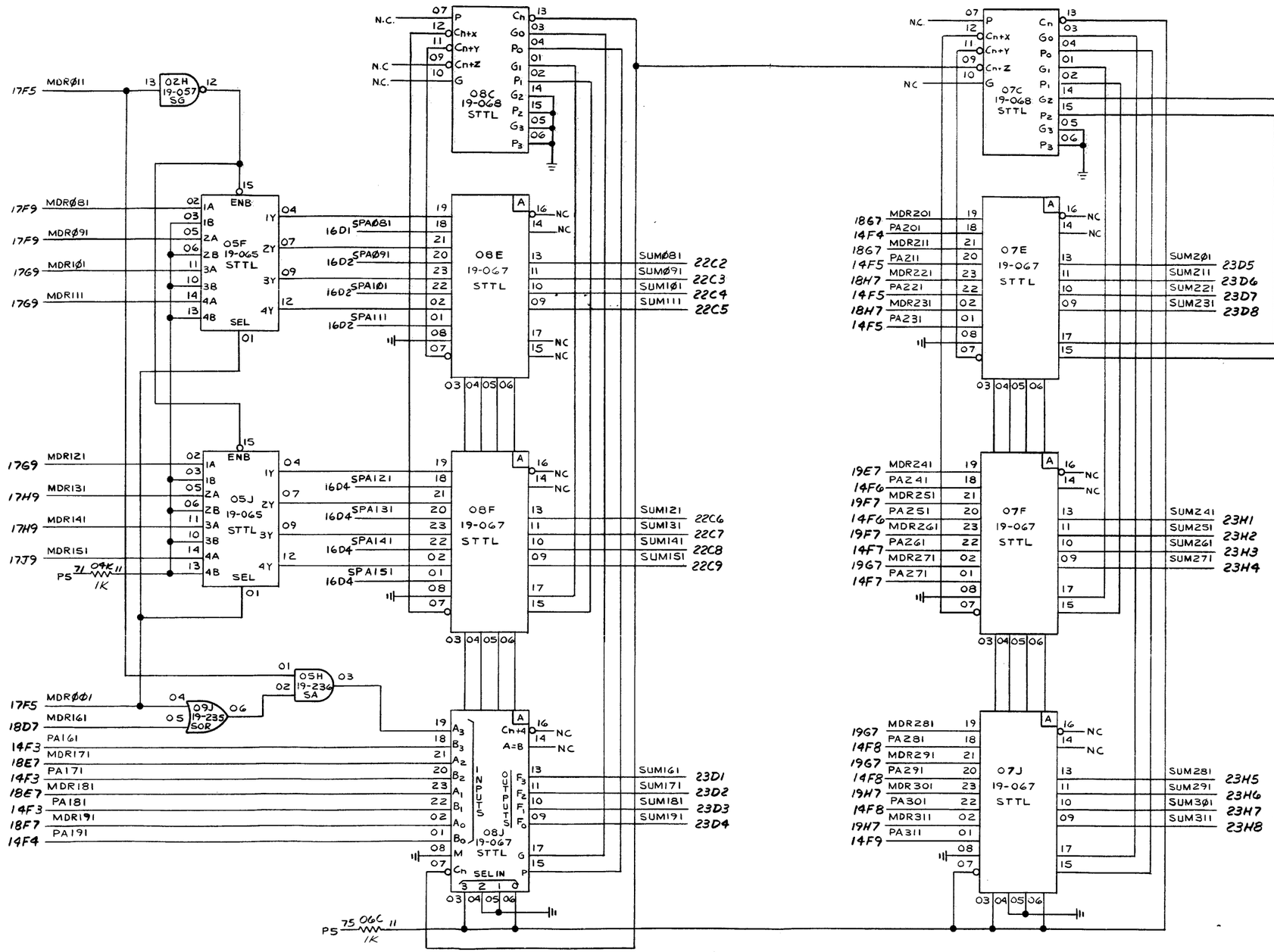
19-233 OOM
OCT F/F RMD3
23H1, 20J5, 4J1, 3J1, 21K5 MDR241
23H2, 20J6, 4J1, 3J1, 21K6 MDR251
23H3, 20J6, 4K1, 3J1, 21K6 MDR261
23H4, 20J6, 4K1, 3J1, 21K6 MDR271
23H5, 20J8, 4K1, 3J1, 21K7 MDR281
23H6, 20J8, 4K1, 3J1, 21K7 MDR291
23H7, 20J8, 4K1, 3K1, 21K7 MDR301
23H8, 20J9, 4K1, 3K1, 21K7 MDR311

202-1 DEXBØ
2N1 MAR 311
23C7 LMDRØ
22G2 UMDRØ
11R 19-057 SG
18A 19-057 SG
14R 19-057 SG
11H 19-055 SG
11M 19-059 SA
11H 19-055 SG
DISA1 18R3
DISB1 D5
EXBØ 102-1

B	A	MDR 24/31 DATA MUX
0	0	EMD
0	1	OMS
1	0	MAT FAULT
1	1	SBUS

SCALE –	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	A. WILLIAMS	DRAFT	2-7-80
		CHK	
		ENGR	

TITLE CPU-C PROCESSOR MDR BITS 24-31
PART NO. 03976
DRW NO. 35-769 R01
SHEET OF 19 – 25



REVISIONS

NOTES

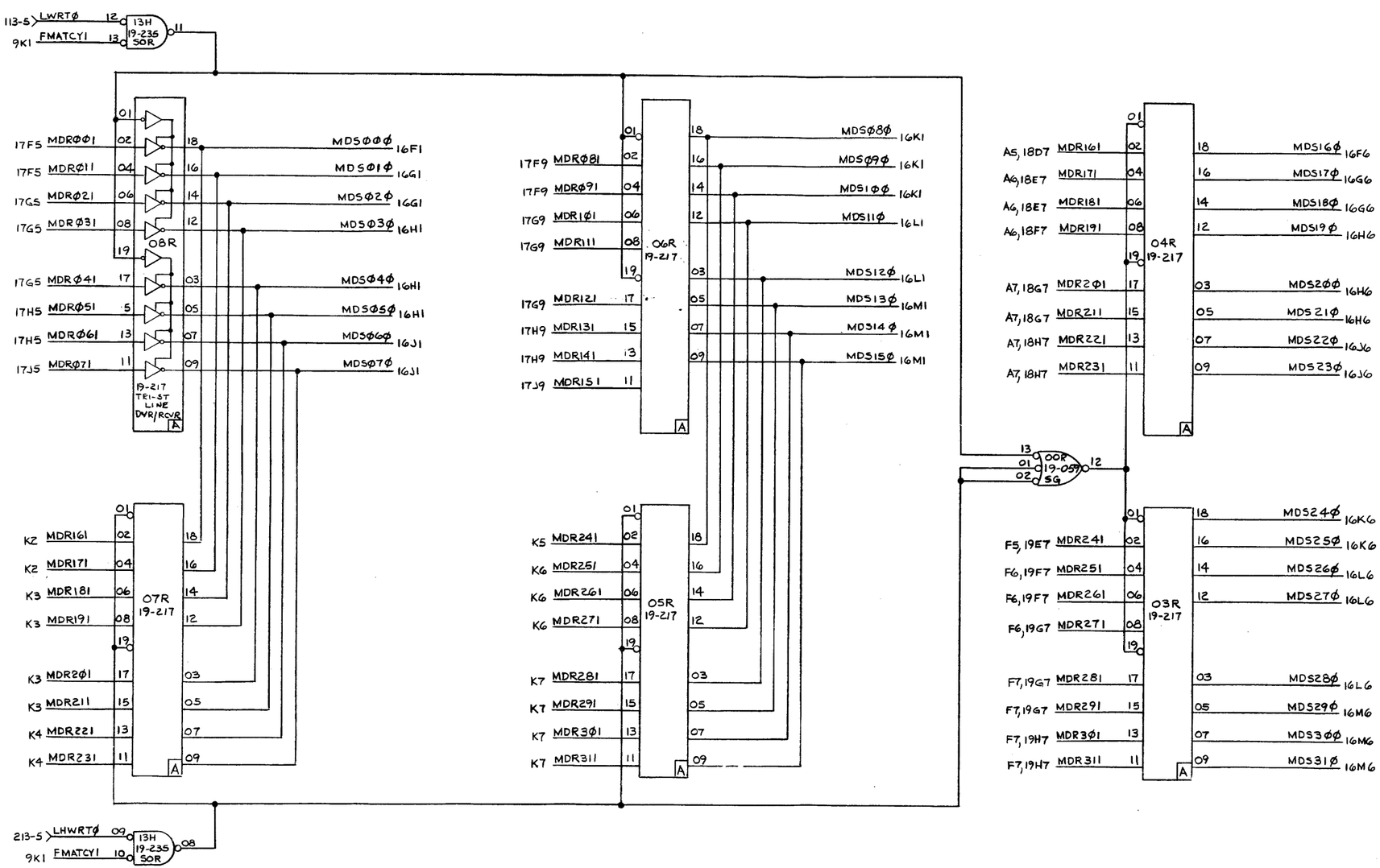
UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	E. JOHNSON	DES/DFT	1-3-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
MDR SUMMER AND EXTEND SIGN LOGIC

TASK 03976 . SHT
DWG 35-769 D08 20-25



REVISIONS

NOTES

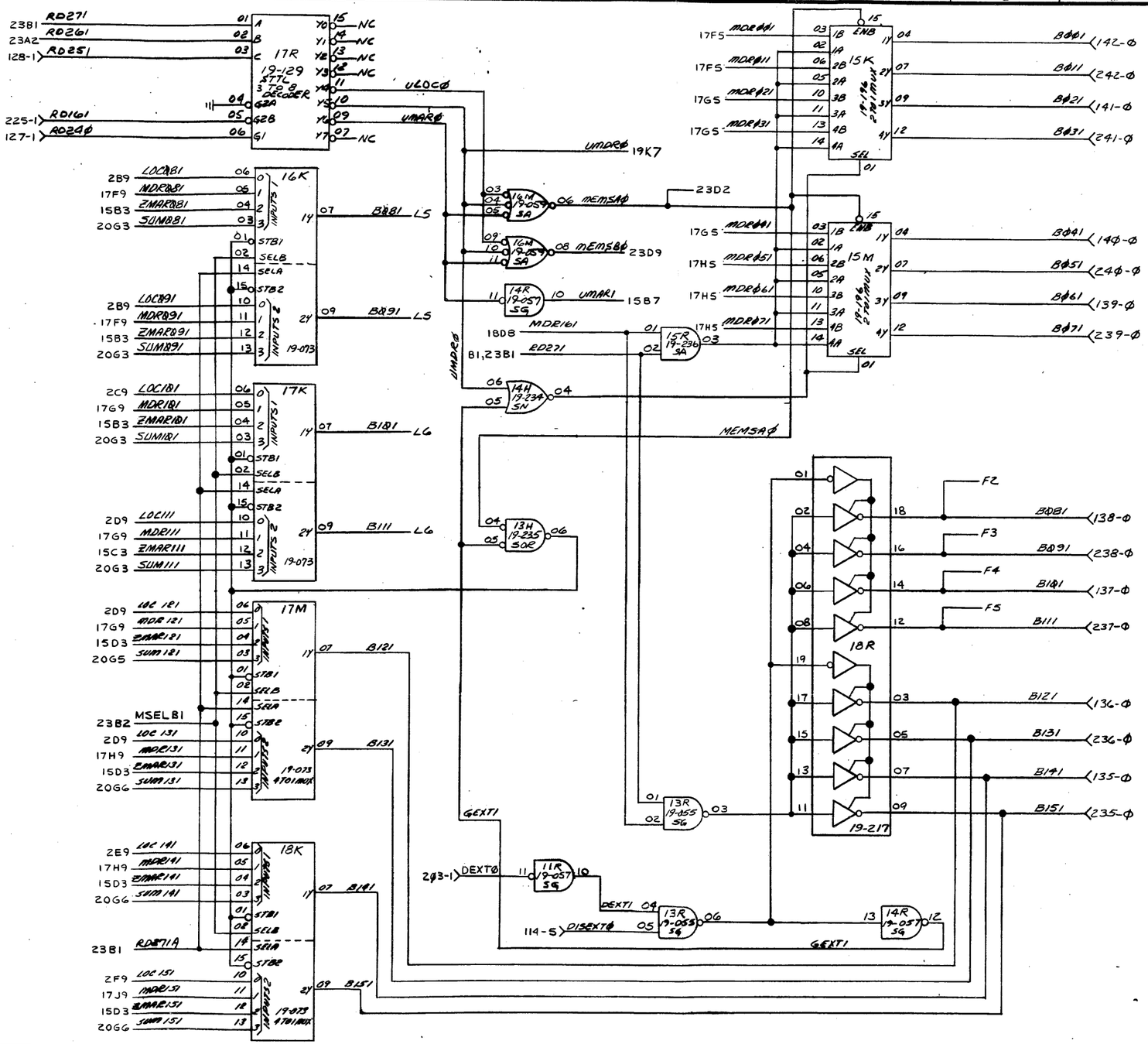
UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME	TITLE	DATE
A.WILLIAMS	DES/DFT	2-19-80
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
MDS DRIVERS

TASK 03976
DWG 35-769 D08
SHT 21 - 25



NOTES

REVISIONS

UNLESS OTHERWISE SPECIFIED	
SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
	A. WILLIAMS	DES/DFT	2-7-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C
B-BUS DRIVERS
BITS ØØ-15

TASK 03976	SHT
DWG 35-769 D08	22-25

PERKIN ELMER

REVISIONS

STB	B	A	B MUX
0	0	0	LOC
0	0	1	MDR
0	1	0	MAR
0	1	1	SUM
1	X	X	HI Z

22C4, 22B1 — 22C9 RD27IA
229-1 RD27I — 10 — 15R 19-236 5A — 08
228-1 KU26I — 09 — 14R 19-057 SG — 08
22B1 — 12 — 01R 19-055 SG — 11
214-5 MDRØ — 13
22C7 MSELB1

2F9 LOC16I
18D7 MDR16I
15F3 ZMAR16I
20G8 SUM16I
22H2 MEMSAØ
RD27IA

2F9 LOC17I
18E7 MDR17I
15F3 ZMAR17I
20G8 SUM17I

2F9 LOC18I
18E7 MDR18I
15F3 ZMAR18I
20G8 SUM18I

2H9 LOC19I
18F7 MDR19I
15F3 ZMAR19I
20G8 SUM19I

2H9 LOC20I
18G7 MDR20I
15G3 ZMAR20I
20M3 SUM20I

2H9 LOC21I
18G7 MDR21I
15H3 ZMAR21I
20M3 SUM21I

2H9 LOC22I
18H7 MDR22I
15H3 ZMAR22I
20M3 SUM22I
22G3 MEMSBØ

2K9 LOC23I
18H7 MDR23I
15H3 ZMAR23I
20M3 SUM23I

19-073 4TO1 MUX

2K9 LOC24I
19E7 MDR24I
15J3 ZMAR24I
20M5 SUM24I

2K9 LOC25I
19F7 MDR25I
15J3 ZMAR25I
20M6 SUM25I

2K9 LOC26I
19F7 MDR26I
15K3 ZMAR26I
20M6 SUM26I

2M9 LOC27I
19G7 MDR27I
15K3 ZMAR27I
20M6 SUM27I

2M9 LOC28I
19G7 MDR28I
15L3 ZMAR28I
20M8 SUM28I

2M9 LOC29I
19G7 MDR29I
15L3 ZMAR29I
20M8 SUM29I

2M9 LOC30I
19H7 MDR30I
15L3 ZMAR30I
20M8 SUM30I

19H7 MDR31I
15M3 ZMAR31I
20M8 SUM31I

125-1 RD15Ø — 14R 19-057 SG — 06

01 A, 02 B, 03 C — 19-168 LTTL 3 TO 8 DECODER — Y0 15 NC, Y1 14 NC, Y2 13 NC, Y3 12 NC, Y4 11, Y5 10 LMDRØ, Y6 09 LMARØ, Y7 07 NC
126-1 RD19I
226-1 RD13I
227-1 RD12I
04 G2A, 05 G2B, 06 G1 16R
11 — 20K — 71 — 1K — P5

01 — 14R 19-057 SG — 02 — LLOC1 — 2A6
LLOCØ

19K7
2A1

B16I (132-Ø)
B17I (232-Ø)
B18I (131-Ø)
B19I (231-Ø)
B20I (130-Ø)
B21I (230-Ø)
B22I (129-Ø)
B23I (229-Ø)
B24I (128-Ø)
B25I (228-Ø)
B26I (127-Ø)
B27I (227-Ø)
B28I (126-Ø)
B29I (226-Ø)
B30I (125-Ø)
B31I (225-Ø)

SCALE—
TOLERANCE
XXX ± .005
XX ± .02
X ± .09
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

TITLE CPU-C
B-BUS DRIVER
BITS 16-31

TAPE NO. 03976
DWG NO. 35-769 DOB
SHEET OF 23—25

CROSS REFERENCE NET#, MNEMONIC, SHEET#

NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.
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0002	ACTR09Ø	5	0064	BCTR13Ø	5	0126	EMAT291	19	0188	LMA12Ø	12	0250	MAR151	15	0312	MDSØ5Ø	16	0374	MPA 111	10	0436	PRES1	8	0498	SØ41A	13	0560	STD311	4	0622	19BØ3	2	0684	Ø1C12	5
0003	ACTR10Ø	5	0065	BCTR14Ø	5	0127	EMAT3Ø1	19	0189	LMA13Ø	12	0251	MAR161	15	0313	MDSØ6Ø	16	0375	MSTOPØ	3	0437	RFAULTØ	11	0499	SØ51 A	13	0561	SUMØ81	20	0623	25B1Ø	2	0685	ØØC06	5
0004	ACTR11Ø	5	0066	BCTR15Ø	5	0128	EMAT 311	19	0190	LMA14Ø	12	0252	MAR171	15	0314	MDS Ø7Ø	16	0376	MARSTPØ	2	0438	RPAØ81	12	0500	SØ61A	13	0562	SUMØ91	20	0624	24A1Ø	2	0686	ØØA06	5
0005	ACTR12Ø	7	0067	BPAØ81	6	0129	EIMARO	15	0191	LMA15Ø	12	0253	MAR131	15	0315	MDSØ8Ø	16	0377	MCLK1A	3	0439	RPAØ91	12	0501	SØ71 A	13	0563	SUM1Ø1	20	0625	23A1Ø	2	0687	ØØD03	5
0006	ACTR13Ø	7	0068	BPAØ91	6	0130	EIMARI	15	0192	LMA16Ø	12	0254	MAR191	15	0316	MDS Ø9Ø	16	0378	MATSTOPØ	5	0440	RPA1Ø1	12	0502	SØ31A	13	0564	SUM111	20	0626	22A1Ø	2	0688	Ø1D12	5
0007	ACTR14Ø	7	0069	BPA1Ø1	6	0131	EXBO	19	0193	LMA17Ø	12	0255	MAR2Ø1	15	0317	MDS 1ØØ	16	0379	MATENØ	9	0441	RPA 111	12	0503	SØ91 A	13	0565	SUM131	20	0627	18A1Ø	2	0689	13D01	5
0008	ACTR15Ø	7	0070	BPA 111	6	0132	ENMAAO	9	0194	LMA18Ø	12	0256	MAR211	15	0318	MDS 11Ø	16	0380	MATEN1	9	0442	RDØØØ	3	0504	S1Ø1A	13	0566	SUM151	20	0628	18AØ4	2	0690	Ø3E15	5
0009	APAØ81	6	0071	BPA121	7	0133	FPAØ81	15	0195	LMA19Ø	12	0257	MAR221	15	0319	MDS 12Ø	16	0381	MFAULTØ	15	0443	RDØ01	4	0505	S111A	13	0567	SUM161	20	0629	19BØ8	2	0691	ØØA03	5
0010	APAØ91	6	0072	BPA 131	7	0134	FPAØ91	15	0196	LMA2ØØ	12	0258	MAR231	15	0320	MDS 13Ø	16	0382	MATFLTØ	11	0444	RDØ11	4	0506	S121A	13	0568	SUM171	20	0630	25BØ7	2	0692	15FØ7	8
0011	APA1Ø1	6	0073	BPA 141	7	0135	FPA1Ø1	15	0197	LMA 21Ø	12	0259	MAR241	15	0321	MDS 14Ø	16	0383	MATO	11	0445	RDØ2Ø	4	0507	S131A	13	0569	SUM181	20	0631	22B1Ø	2	0693	15F1Ø	8
0012	APA111	6	0074	BPA151	7	0136	FPA 111	15	0198	LMA22Ø	12	0260	MAR251	15	0322	MDS 15Ø	16	0384	MSBCO	13	0446	RDØ31	4	0508	S141A	13	0570	SUM191	20	0632	23B1Ø	2	0694	15F15	8
0013	APA121	7	0075	BRFØ81	4	0137	FPA121	15	0199	LMA23Ø	12	0261	MAR261	15	0323	MDS 16Ø	16	0385	MDHSAI	17	0447	RD121	23	0509	S151A	13	0571	SUM2Ø1	20	0633	24B1Ø	2	0695	15H08	8
0014	APA131	7	0076	BRFØ91	4	0138	FPA131	15	0200	LMA24Ø	12	0262	MAR271	15	0324	MDS 17Ø	16	0386	MDSBIA	18	0448	RD131	23	0510	S161A	13	0572	SUM211	20	0634	19B11	2	0696	15H06	8
0015	APA141	7	0077	BRF1Ø1	4	0139	FPA141	15	0201	LMA25Ø	12	0263	MAR231	15	0325	MDS 18Ø	16	0387	MDHCKO	17	0449	RD141	23	0511	S171 A	13	0573	SUM 221	20	0635	18A06	2	0697	15H03	8
0016	APA151	7	0078	BRF111	4	0140	FPA151	15	0202	LMA 26Ø	12	0264	MAR291	15	0326	MDS 19Ø	16	0388	MDLCKO	18	0450	RD161	22	0512	S181 A	13	0574	SUM 231	20	0636	14MØ2	3	0698	16H03	8
0017	ACSO	5	0079	BRF121	4	0141	FPA161	14	0203	LMA27Ø	12	0265	MAR3Ø1	15	0327	MDS 2ØØ	16	0389	MATFLTI	11	0451	RD251	22	0513	S191A	13	0575	SUM241	20	0637	14MØ5	3	0699	16H06	8
0018	AWEO	5	0080	BRF131	4	0142	FPA171	14	0204	LMA28Ø	12	0266	MAR311	15	0328	MDS 21Ø	16	0390	MFAULT1	15	0452	RD 261	23	0514	S2Ø1A	13	0576	SUM251	20	0638	14MØ6	3	0700	13C06	9
0019	AØ1	8	0081	BRF141	4	0143	FPA181	14	0205	LMA29Ø	12	0267	MDRØ7Ø	16	0329	MDS 22Ø	16	0391	MDLSAI	18	0453	RD271	23	0515	S211A	13	0577	SUM261	20	0639	14M09	3	0701	2ØJØ8	9
0020	A11	8	0082	BRF151	4	0144	FPA191	14	0206	LMA 3ØØ	12	0268	MDRØ8Ø	16	0330	MDS 23Ø	16	0392	MDSBIB	18	0454	RD271A	23	0516	S221A	13	0578	SUM 271	20	0640	14M12	3	0702	2ØF12	9
0021	A21	8	0083	BRF161	4	0145	FPA2Ø1	14	0207	LMA31Ø	12	0269	MDRØ9Ø	16	0331	MDS 24Ø	16	0393	MDSBO	18	0455	RD15Ø	23	0517	S231A	13	0579	SUM281	20	0641	14M15	3	0703	11RØ2	9
0022	AIBI1	3	0084	BRF171	4	0146	FPA211	14	0208	LOCØ81	2	0270	MDR1ØØ	16	0332	MDS25Ø	16	0394	MSELBI	23	0456	RD24Ø	22	0518	S241A	13	0580	SUM 291	20	0642	14M16	3	0704	11RØ4	9
0023	ALGNØ	15	0085	BRF181	4	0147	FPA221	14	0209	LOCØ91	2	0271	MDR11Ø	16	0333	MDS26Ø	16	0395	MEMSAØ	22	0457	SØØ1	13	0519	S251 A	13	0581	SUM 3Ø1	20	0643	14M19	3	0705	11CØ6	9
0024	ACP1	5	0086	BRF191	4	0148	FPA231	14	0210	LOC1Ø1	2	0272	MDR12Ø	16	0334	MDS27Ø	16	0396	MEMSBØ	22	0458	SØ11	13	0520	S261A	13	0582	SUM 311	20	0644	19J07	3	0706	13C03	9
0025	APE1	5	0087	BRF2Ø1	4	0149	FPA241	14	0211	LOC111	2	0273	MDR13Ø	16	0335	MDS28Ø	16	0397	MDREO	23	0459	SØ21	13	0521	S271 A	13	0583	UMARI	22	0645	19J06	3	0707	98C1Ø	9
0026	ASHRD1	8	0088	BRF211	10	0150	FPA251	14	0212	LOC121	2	0274	MDR14Ø	16	0336	MDS 29Ø	16	0398	PAØ8Ø	6	0460	SØ31	13	0522	S281A	13	0584	UMARO	22	0646	19J05	3	0708	12C1Ø	9
0027	BØØ1	22	0089	BPEO	5	0151	FPA261	14	0213	LOC131	2	0275	MDRØØ1	17	0337	MDS 3ØØ	16	0399	PAØ9Ø	6	0461	SØ41	13	0523	S291A	13	0585	UMDRO	22	0647	12H08	3	0709	1ØD06	9
0028	BØ11	22	0090	BWEO	5	0152	FPA271	14	0214	LOC141	2	0276	MDRØ11	17	0338	MDS 31Ø	16	0400	PA1ØØ	6	0462	SØ51	13	0524	S3Ø1A	13	0586	WSTKO	9	0648	14K02	4	0710	1ØD05	9
0029	BØ21	22	0091	BCSO	5	0153	FPA281	14	0215	LOC151	2	0277	MDRØ21	17	0339	MDS ØØ1	16	0401	PA 11Ø	6	0463	SØ61	13	0525	S311A	13	0587	XRPA	3	0649	14K05	4	0711	22D08	9
0030	BØ31	22	0092	BCPI	5	0154	FPA291	14	0216	LOC161	2	0278	MDRØ31	17	0340	MDS Ø11	16	0402	PA 12Ø	7	0464	SØ71	13	0526	SCLK1	3	0588	XRPØØA	5	0650	14K06	4	0712	16C08	9
0031	BØ41	22	0093	BSCLRØ	3	0155	FPA3Ø1	14	0217	LOC171	2	0279	MDRØ41	17	0341	MDSØ21	16	0403	PA 13Ø	7	0465	SØ81	13	0527	SCLRØC	3	0589	XRPB	4	0651	14K09	4	0713	1ØE06	9
0032	BØ51	22	0094	BSCLRØA	3	0156	FPA311	14	0218	LOC181	2	0280	MDRØ51	17	0342	MDSØ31	16	0404	PA 14Ø	7	0466	SØ91	13	0528	SCLKØ	9	0590	XRPD	15	0652	14K12	4	0714	21J03	10
0033	BØ61	22	0095	BAØ1	8	0157	FAINCRØA	5	0219	LOC191	2	0281	MDRØ61	17	0343	MDSØ41	16	0405	PA15Ø	7	0467	S1Ø1	13	0529	SHCLKØ	8	0591	ULOCO	22	0653	14K15	4	0715	21J06	10
0034	BØ71	22	0096	BA11	8	0158	FAINCR1	5	0220	LOC2Ø1	2	0282	MDRØ71	17	0344	MDSØ51	16	0406	PAØ81	6	0468	S111	13	0530	SHARED1	8	0592	ZMARØ81	15	0654	14K16	4	0716	21J08	10
0035	BØ81	22	0097	BA21	8	0159	FAINCRØ	5	0221	LOC211	2	0283	MDRØ81	17	0345	MDSØ61	16	0407	PAØ91	6	0469	S121	13	0531	SRFØ81	8	0593	ZMAR091	15	0655	14K19	4	0717	2ØF02	10
0036	BØ91	22	0098			0160	FAINCRIA	5	0222	LOC221	2	0284	MDRØ91	17	0346	MDSØ71	16	0408	PA1Ø1	6	0470	S131	13	0532	SRFØ91	8	0594	ZMAR1Ø1	15	0656	13K02	4	0718	2ØJ03	10
0037	B1Ø1	22	0099	CAMAO	14	0161	FBINCRØ	5	0223	LOC231	2	0285	MDR1Ø1	17	0347	MDSØ81	16	0409	PA 111	6	0471	S141	13	0533	SRF1Ø1	8	0595	ZMAR111	15	0657	13K05	4	0719	22F12	10
0038	B111	22	0100	CLK1	3	0162	FBINCR1	5	0224	LOC241	2	0286	MDR 111	17	0348	MDSØ91	16	0410	PA 121	7	0472	S151	13	0534	SRF 111	8	0596	ZMAR121	15	0658	13K06	4	0720	22F09	10
0039	B121	22	0101	CLSTAO	11	0163	FBINCRØN	5	0225	LOC251	2	0287	MDR121	17	0349	MDS1Ø1	16	0411	PA 131	7	0473	S161	13	0535	SRF 121	8	0597	ZMAR131	15	0659	13K09	4	0721	22F07	10
0040	B131	22	0102	CLK1C	3	0164	FBINCRIA	5	0226	LOC261	2	0288	MDR131	17	0350	MDS 111	16	0412	PA141	7	0474	S171	13	0536	SRF131	8	0598	ZMAR141	15	0660	13K12	4	0722	22F04	10
0041	B141	22	0103	CLKØ	9	0165	FSHAREDI	8	0227	LOC271	2	0289	MDR141	17	0351	MDS 121	16	0413	PA151	7	0475	S181	13	0537	SRF 141	8	0599	ZMAR151	15	0661	02H02	4	0723	22J12	10
0042	B151	22	0104	CWRO	11	0166	FSHAREDØ	8	0228	LOC281	2	0290	MDR151	17	0352	MDS131	16	0414	PA161	14	0476	S191	13	0538	SRF151	8	0600	ZMAR161	15	0662	12C02	4	0724	22J11	10
0043	B161	23	0105	DSTOPØ	3	0167	FPRES1	8	0229	LOC291	2	0291	MDR161	18	0353	MDS 141	16	0415	PA171	14	0477	S2Ø1	13	0539	SRF 161	8	0601	ZMAR171	15	0663	11F06	4	0725	22J09	10
0044	B171	23	0106	DIRØ	4	0168	FMATCY1	9	0230	LOC3Ø1	2	0292	MDR171	18	0354	MDS 151	16	0416	PA181	14	0478	S211	13	0540	SRF 171	8	0602	ZMAR181	15	0664	11F07	4	0726	25J13	10
0045	B181	23	0107	DCLK1	3	0169	FSCLK1	9	0231	LPSTDCKØ	3	0293	MDR181	18	0355	MDS161	16	0417	PA191	14	0479	S221	13	0541	SRF 181	8	0603	ZMAR191	15	0665	19F07	4	0727	25J11	10
0046	B191	23	0108	DIR1	4	0170	FSCLKØ	9	0232	LPSTD1	3	0294	MDR191	18	0356	MDS171	16	0418	PA 2Ø1	14	0480	S231	13	0542	SRF 191	8	0604	ZMAR2Ø1	15	0666	19F06	4	0728	25J1Ø	10
0047	B2Ø1	23	0109	DISSTK1	8	0171	FDUAØ	9	0233	LPSTDØ	3	0295	MDR2Ø1	18	0357	MDS 181	16	0419	PA 211	14	0481	S241	13	0543	SRF 2Ø1	8	0605	ZMAR211	15	0667	Ø9F07	4	0729	25J09	10
0048	B211	23	0110	DISSTKØ	8	0172	FNCEO	15	0234	LLOC1	23	0296	MDR211	18	0358	MDS191	16	0420	PA221	14	0482	S251	13	0544	STD151	4	0606	ZMAR221	15	0668	Ø1E05	5	0730	24F13	10
0049	B221	23	0111	DUAO	9	0173	FPACLK1	15	0235	LMARO	23	0297	MDR221	18	0359	MDS2Ø1	16	0421	PA231	14	0483	S261	13	0545	STD161	4	0607	ZMAR231	15	0669	13D04	5	0731	24F11	10
0050	B231	23	0112	DIRTO	8	0174	GMA 251	10	0236	LMDRO	23	0298	MDR231	18	0360	MDS211	16	0422	PA241	14	0484	S271	13	0546	STD171	4	0608	ZMAR241	15	0670	Ø4E15	5	0732	24F1Ø	10
0051	B241	23	0113	DEXBO	19	0175	GMA 261	10	0237	LSSTDO	4	0299	MDR241	19	0361	MDS221	16	0423	PA251	14	0485	S281	13	0547	STD181	4	0609	ZMAR251	15	0671	Ø5E15	5	0733	24F09	10
0052	B251	23	0114	DISA1	19	0176	GMA 271	10	0238	LSSTDCKØ	4	0300	MDR251	19	0362	MDS 231	16	0424	PA261	14	0486	S291	13	0548	STD191	4	0610	ZMAR261	15	0672	Ø1D02	5	0734	19K11	10
0053	B261	23	0115	DISB1	19	0177	GMA 281	10	0239	LØ1	8	0301	MDR261	19	0363	MDS 241	16	0425	PA 271	14	0487	S3Ø1	13	0549	STD2Ø1	4	0611	ZMAR271	15	0673	Ø1D08	5	0735	22K03	10
0054	B271	23	0116	DISEXTØ	22	0178	GETSSTE1	3	0240	L11	8	0302	MDR271	19	0364	MDS 251	16	0426	PA 281	14	0488	S311	13	0550	STD211	4	0612	ZMAR281	15	0674	Ø2E15	5	0736	25J17	10
0055	B281	23	0117	DEXTØ	22	0179	GETSSTEØ	9	0241	LHWRTO	21	0303	MDR281	19	0365	MDS261	16	0427	PA 291	14	0489	SLFØ1	8	0551	STD221	4	0613	ZMAR291	15	0675	ØØE06	5	0737	25J15	10
0056	B291	23	0118	DEXT1	22	0180	GEXT1	22	0242	LWRTO	21	0304	MDR291	19	0366	MDS271	16	0428	PA 3Ø1	14	0490	SLF11	8	0552	STD231	4	0614	ZMAR3Ø1	15	0676	ØØD11	5	0738	24F17	10
0057	B3Ø1	23	0119	DRD1	15	0181	HALTO	9	0243	MAR081	15	0305	MDR3Ø1	19	0367	MDS281	16	0429	PA 311	14	0491	SLF21	8	0553	STD241	4	0615	ZMAR311	15	0677	Ø6C03	5	0739	24F15	10
0058	B311	23	0120	EPSTD1	3	0182	ILOCO	2	0244	MAR091	15	0306	MDR311	19	0368	MDS291	16	0430	PSEL1	9	0492	SLF31	8	0554	STD 251	4	0616	18B06	2	0678	ØØC11	5	0740	24J17	10
0059	BCTRØ8Ø	5	0121	ESSTDØ	4	0183	IMARO	2	0245	MAR1Ø1	15	0307	MDSØØØ	16	0369	MDS3Ø1	16	0431	PSW1Ø1	9	0493	SLF41	8	0555	STD261	4	0617	18BØ3	2	0679	ØØE05	5	0741	24J15	10
0060	BCTR09Ø	5	0122	ENMAAØA	9	0184	LMAØ8Ø	12	0246	MAR 111	15	0308	MDSØ1Ø	16	0370	MDS 311	16	0432	PSW111	9	0494	SØ01 A	13	0556	STD271	4	0618	25A1Ø	2	0680	Ø5H08	5	0742	19H03	10
0061	BCTR1ØØ	5	0123	EALI	9	0185	LMA09Ø	12	0247	MAR121	15	0309	MDSØ2Ø	16	0371	MPA Ø81	10	0433	PMEM1	9	0495	SØ11 A	13	0557	STD281	4	0619	18A12	2	0681	12D03	5	0743	24J13	10
0062	BCTR11Ø	5	0124	ENRPAO	9	0186	LMA1ØØ	12	0248	MAR131	15	0310	MDSØ3Ø	16	0372	MPAØ91	10	0434	PSW211	9	0496	SØ21 A	13	0558	STD 291	4	0620	19B06	2	0682	Ø1E06	5	0744	24J11	10

NOTES

REVISIONS

UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME	TITLE	DATE
J.BIELSKIE	DES/DFT	5-16-80
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C

TASK 03976 SHT 24-25
DWG 35-769 D08

BRUNING 44-3 · 40"

CROSS REFERENCE NET#, MNEMONIC, SHEET#

NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.
0745	24J1Ø	10	0807	16AØ6	13	0869	ØSFØ1	20	0931	GND		0993	CLRAO	11	1055			1117			1179			1241			1303			1365			1427		
0746	24JØ9	10	0808	16AØ7	13	0870	ØSFØ3	20	0932	GND		0994	MATRSRO	9	1056			1118			1180			1242			1304			1366			1428		
0747			0809	16AØ8	13	0871	ØSF12	20	0933	GND		0995	11D08	9	1057			1119			1181			1243			1305			1367			1429		
0748	16DØ8	11	0810	16AØ9	13	0872	ØSJØ4	20	0934	GND		0996	DENCLKØ	15	1058			1120			1182			1244			1306			1368			1430		
0749	Ø3B12	11	0811	16A1Ø	13	0873	ØSJØ7	20	0935	GND		0997	Z1J11	10	1059			1121			1183			1245			1307			1369			1431		
0750	19FØ4	11	0812	16A11	13	0874	ØSJØ9	20	0936	GND		0998	13D13	11	1060			1122			1184			1246			1308			1370			1432		
0751	19F1Ø	11	0813	16A12	13	0875	ØSJ12	20	0937	GND		0999	CAGDIRO	14	1061			1123			1185			1247			1309			1371			1433		
0752	19F13	11	0814	16A13	13	0876	Ø8C12	20	0938	GND		1000	SPAØ31	16	1062			1124			1186			1248			1310			1372			1434		
0753	Ø4BØ9	11	0815	16A14	13	0877	Ø3C11	20	0939	GND		1001	SPAØ91	16	1063			1125			1187			1249			1311			1373			1435		
0754			0816	16A66	13	0878	Ø9J06	20	0940	GND		1002	SPA1Ø1	16	1064			1126			1188			1250			1312			1374			1436		
0755	Ø4B11	11	0817	Ø6BØ8	15	0879	Ø5H03	20	0941	GND		1003	SPA111	16	1065			1127			1189			1251			1313			1375			1437		
0756	Ø4BØ6	11	0818	Ø6C11	15	0880	Ø8F17	20	0942	GND		1004	SPA121	16	1066			1128			1190			1252			1314			1376			1438		
0757	Ø4BØ3	11	0819	Ø6B12	15	0881	Ø8F15	20	0943	GND		1005	SPA131	16	1067			1129			1191			1253			1315			1377			1439		
0758	ØØBØ3	11	0820	Ø9EØ6	15	0882	Ø8J17	20	0944	GND		1006	SPA141	16	1068			1130			1192			1254			1316			1378			1440		
0759	ØØBØ6	11	0821	13D1Ø	15	0883	Ø8J15	20	0945	GND		1007	SPA151	16	1069			1131			1193			1255			1317			1379			1441		
0760	ØØBØ8	11	0822	13C11	15	0884	Ø8C13	20	0946	GND		1008	GND		1070			1132			1194			1256			1318			1380			1442		
0761	Ø6C1Ø	11	0823	Ø9DØ6	15	0885	Ø6C11	20	0947	GND		1009	GND		1071			1133			1195			1257			1319			1381			1443		
0762	Ø2CØ9	11	0824	Ø5H06	15	0886	Ø7C11	20	0948	GND		1010	Ø7E17	20	1072			1134			1196			1258			1320			1382			1444		
0763	Ø1BØ6	11	0825	Ø2BØ6	15	0887	Ø7C12	20	0949	GND		1011	07E15	20	1073			1135			1197			1259			1321			1383			1445		
0764	Ø1BØ8	11	0826	Ø9MØ7	17	0888	Ø7F17	20	0950	GND		1012	ØØR12	21	1074			1136			1198			1260			1322			1384			1446		
0765	Ø1BØ3	11	0827	Ø9MØ9	17	0889	Ø7F15	20	0951	GND		1013	MATRSDO	19	1075			1137			1199			1261			1323			1385			1447		
0766	Ø2B1Ø	11	0828	Ø8MØ7	17	0890	Ø7J17	20	0952	GND		1014	Ø9DØ9	19	1076			1138			1200			1262			1324			1386			1448		
0767	Ø4CØ8	11	0829	Ø8MØ9	17	0891	Ø7J15	20	0953	GND		1015	11M12	19	1077			1139			1201			1263			1325			1387			1449		
0768	Ø3CØ6	11	0830	Ø7MØ7	17	0892	13H11	21	0954	GND		1016	GND		1078			1140			1202			1264			1326			1388			1450		
0769	Ø3CØ7	11	0831	Ø7MØ9	17	0893	13HØ8	21	0955	GND		1017	10KØ6	11	1079			1141			1203			1265			1327			1389			1451		
0770	Ø3CØ9	11	0832	Ø6MØ7	17	0894	13HØ6	22	0956	GND		1018	10RØ6	11	1080			1142			1204			1266			1328			1390			1452		
0771	Ø5DØ8	11	0833	Ø6MØ9	17	0895	15RØ3	22	0957	GND		1019	11R12	11	1081			1143			1205			1267			1329			1391			1453		
0772	Ø5DØ9	11	0834	Ø9KØ7	17	0896	14HØ4	22	0958	GND		1020	ØIC06	11	1082			1144			1206			1268			1330			1392			1454		
0773	22HØ3	12	0835	Ø9KØ9	17	0897	13RØ6	22	0959	GND		1021	MCLK1	3	1083			1145			1207			1269			1331			1393			1455		
0774	22HØ6	12	0836	Ø8KØ7	17	0898	13RØ3	22	0960	GND		1022	ASHRDØ	8	1084			1146			1208			1270			1332			1394			1456		
0775	22HØ8	12	0837	Ø8KØ9	17	0899	14RØ3	23	0961	GND		1023	20J06	9	1085			1147			1209			1271			1333			1395			1457		
0776	22H11	12	0838	Ø7KØ7	17	0900	14RØ6	23	0962	GND		1024	READØ	11	1086			1148			1210			1272			1334			1396			1458		
0777	21HØ3	12	0839	Ø7KØ9	17	0901	LLOCO	23	0963	GND		1025			1087			1149			1211			1273			1335			1397			1459		
0778	21HØ6	12	0840	Ø6KØ7	17	0902	2ØK11	23	0964	GND		1026			1088			1150			1212			1274			1336			1398			1460		
0779	21HØ8	12	0841	Ø6KØ9	17	0903	16H11	14	0965	GND		1027			1089			1151			1213			1275			1337			1399			1461		
0780	21H11	12	0842	13HØ3	15	0904	GND		0966	GND		1028			1090			1152			1214			1276			1338			1400			1462		
0781	24M13	12	0843	Ø4KØ7	18	0905	GND		0967	GND		1029			1091			1153			1215			1277			1339			1401			1463		
0782	24M11	12	0844	Ø4KØ9	18	0906	GND		0968	GND		1030			1092			1154			1216			1278			1340			1402			1464		
0783	24M1Ø	12	0845	Ø3KØ7	18	0907	GND		0969	GND		1031			1093			1155			1217			1279			1341			1403			1465		
0784	24MØ9	12	0846	Ø3KØ9	18	0908	GND		0970	GND		1032			1094			1156			1218			1280			1342			1404			1466		
0785	24M17	12	0847	Ø2KØ7	18	0909	GND		0971	GND		1033			1095			1157			1219			1281			1343			1405			1467		
0786	24M15	12	0848	Ø2KØ9	18	0910	GND		0972	GND		1034			1096			1158			1220			1282			1344			1406			1468		
0787	19HØ6	12	0849	Ø1KØ7	18	0911	GND		0973	GND		1035			1097			1159			1221			1283			1345			1407			1469		
0788	22M17	12	0850	Ø1KØ9	18	0912	GND		0974	GND		1036			1098			1160			1222			1284			1346			1408			1470		
0789	22M15	12	0851	Ø9J11	18	0913	GND		0975	GND		1037			1099			1161			1223			1285			1347			1409			1471		
0790	22M13	12	0852	Ø4MØ7	19	0914	GND		0976	GND		1038			1100			1162			1224			1286			1348			1410			1472		
0791	22M11	12	0853	Ø4MØ9	19	0915	GND		0977	GND		1039			1101			1163			1225			1287			1349			1411			1473		
0792	22M1Ø	12	0854	Ø3MØ7	19	0916	GND		0978	GND		1040			1102			1164			1226			1288			1350			1412			1474		
0793	22MØ9	12	0855	Ø3MØ9	19	0917	GND		0979			1041			1103			1165			1227			1289			1351			1413			1475		
0794	20HØ6	12	0856	Ø2MØ7	19	0918	GND		0980	GND		1042			1104			1166			1228			1290			1352			1414			1476		
0795	25K12	12	0857	Ø2MØ9	19	0919	GND		0981	GND		1043			1105			1167			1229			1291			1353			1415			1477		
0796	25K11	12	0858	Ø1MØ7	19	0920	GND		0982	GND		1044			1106			1168			1230			1292			1354			1416			1478		
0797	23KØ3	12	0859	Ø1MØ9	19	0921	GND		0983	GND		1045			1107			1169			1231			1293			1355			1417			1479		
0798	23RØ6	12	0860	Ø9JØ8	19	0922	GND		0984	GND		1046			1108			1170			1232			1294			1356			1418			1480		
0799	20FØ4	12	0861	14RØ4	19	0923	GND		0985	SUM 121	20	1047			1109			1171			1233			1295			1357			1419			1481		
0800	15H11	12	0862	18AØ8	19	0924	GND		0986	SUM 141	20	1048			1110			1172			1234			1296			1358			1420			1482		
0801	16AØ1	13	0863	11RØ8	19	0925	GND		0987	18BØ8	2	1049			1111			1173			1235			1297			1359			1421			1483		
0802	16AØ2	13	0864	11HØ6	19	0926	GND		0988	GESSTD1	9	1050			1112			1174			1236			1298			1360			1422			1484		
0803	16AØ3	13	0865	11H38	19	0927	GND		0989	ØIB11	5	1051			1113			1175			1237			1299			1361			1423			1485		
0804	16AØ4	13	0866	22H12	20	0928	GND		0990	FMINTCT2	19	1052			1114			1176			1238			1300			1362			1424			1486		
0805	16AØ5	13	0867	Ø4K11	20	0929	GND		0991	JAMSHRDI	19	1053			1115			1177			1239			1301			1363			1425			1487		
0806	13AØ1	13	0868	ØSFØ4	20	0930	GND		0992	JAMDIRT2	19	1054			1116			1178			1240			1302			1364			1426			1488		

NOTES

REVISIONS					
READØ WAS ADDED TO NET 1024.					
E.C.J.		4494	M	10-23-80	R01

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
J. BIELSKIE		DES/DFT	5-17-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-C

TASK 03976 | SHT 25-25

DWG 35-769 R01 D08

IRONING 44-131 4/67

TEST POINTS

T.P.	MNEMONIC	SHT.
TPA	FDATA (115-6)	5
TPB	BRST1 (114-6)	5
TPC	(113-6)	6
TPD	GND (112-6)	6
TPE	(111-6)	6
TPF	(110-6)	6
TPG	GND (116-6)	5
TPH	(109-6)	6
TPJ	EXOSCØ (108-6)	9
TPK	INHFSØ (107-6)	13
TPM	CLKID (106-6)	9
TPN	ENEXOØ (105-6)	9

STRAPPING INFO.

FROM	TO	SHT
00A-72	00A-10	5
02A-73	02A-09	6

CABLE CONNECTOR MAP

CONN	TERM. NO.	ROW 2	ROW 1
6	16		
	15		
	14		
	13		
	12		
	11		
	10		
	09		
	08		
	07		
	06		
	05		
	04		
	03		
	02		
	01		
	00		
5	24	GND	GND
	23		
	22		
	21		
	20		
	19		
	18		
	17		CWRØ
	16	MDHSAI	ENMAAØ
	15	CAMAØ	PA3Ø1
	14	MDRESØ	DISEXTØ
	13	LHWRTØ	LWRTØ
	12	PSBCØ	MSBCØ
	11	PMEMI	MFAULTØ
	10	MDLCKØ	MDHCKØ
	09	MDSBØ	MDLSAI
	08		HALTØ
	07	GND	GND
	06	FSCLKI	FSCLKØ
	05	GND	GND
	04	LPSTDØ	LSSTDØ
	03	CLSTAØ	MATSTOPØ
	02	RESULTØ	MARSTPØ
	01	ILOCØ	IMARØ
	00	GND	GND
4	24	GND	GND
	23		
	22		
	21	GND	GND
	20		
	19		
	18	GND	GND
	17		
	16		
	15	GND	GND
	14		
	13		
	12	GND	GND
	11	S171	S161
	10	S191	S181
	09	GND	GND
	08	S211	S201
	07	S231	S221
	06	GND	GND
	05	S251	S241
	04	S271	S261
	03	GND	GND
	02	S291	S281
	01	S311	S300
	00	GND	GND
3	16		
	15		
	14		
	13		
	12		
	11		
	10		
	09		
	08		
	07		
	06		
	05		
	04		
	03		
	02		
	01		
	00		

FOR SPARE GATES LISTING SEE SHEET 8

PART NO.	~~REF DESIGNATION~~	~~SPARE OUTPUT NO.~~

BACK PANEL MAP

CONN	TERM. NO.	ROW 1	ROW 2
2	43	GND	GND
	42	DMA14Ø	DMA15Ø
	41	DMA12Ø	DMA13Ø
	40	DMA1ØØ	DMA11Ø
	39	DMA08Ø	DMA09Ø
	38	DMA06Ø	DMA07Ø
	37	DMA04Ø	DMA05Ø
	36	DMA02Ø	DMA03Ø
	35	DMA00Ø	DMA01Ø
	34	GND	GND
	33	GND	GND
	32	DMA17Ø	DMX15Ø
	31	DMA16Ø	DMX14Ø
	30	LOADØ	DMX13Ø
	29	ANSØ	DMX12Ø
	28	SOTØ	DMX11Ø
	27	EOTØ	DMX1ØØ
	26	XREQØ	DMX09Ø
	25	QUEØ	DMX08Ø
	24	GND	GND
	23	GND	GND
	22	FAULTØ	TPCØ
	21	DMARSØ	
	20	GND	GND
	19	GND	GND
	18	MDS3ØØ	MDS31Ø
	17	MDS28Ø	MDS29Ø
	16	MDS26Ø	MDS27Ø
	15	MDS24Ø	MDS25Ø
	14	MDS22Ø	MDS23Ø
	13	MDS2ØØ	MDS21Ø
	12	MDS18Ø	MDS19Ø
	11	MDS16Ø	MDS17Ø
	10	GND	GND
	09	GND	GND
	08	MDS14Ø	MDS15Ø
	07	MDS12Ø	MDS13Ø
	06	MDS1ØØ	MDS11Ø
	05	MDS08Ø	MDS09Ø
	04	MDS06Ø	MDS07Ø
	03	MDS04Ø	MDS05Ø
	02	MDS02Ø	MDS03Ø
	01	MDS00Ø	MDS01Ø
	00	GND	GND

BACK PANEL MAP

ROW 1	ROW 2	TERM. NO.	CONN.
GND	GND	43	2
YS21	YS31	42	
YS01	YS11	41	
YD101	YD111	40	
YD081	YD091	39	
IRØ6Ø	IRØ7Ø	38	
IRØ4Ø	IRØ5Ø	37	
IRØ2Ø	IRØ3Ø	36	
IRØØØ	IRØ1Ø	35	
GND	GND	34	
GND	GND	33	
FPPFLTØ	LMRQØ	32	
SERØ	SMBSYØ	31	
DISBØ	DISAØ	30	
GDIRØ	RD271	29	
RD251	RD261	28	
RD241	RD121	27	
RD141	RD131	26	
RD15Ø	RD161	25	
GND	GND	24	
GND	GND	23	
RDØØ1	RD011	22	
RD021	RD031	21	
GND	GND	20	
GND	GND	19	
RD041	RD051	18	
RD301	RD311	17	
RD281	RD291	16	
PSW161	PSW111	15	
PSW261	PSW271	14	
PSW181	MSTOPØ	13	
OPSTOPØ	DSTOPØ	12	
FPPFØ	RSTOPØ	11	
GND	GND	10	
GND	GND	09	
BWRTØ	TRAPØ	08	
SCLRØ	CLFLRØ	07	
SVØ	BCNTØ	06	
TACKØ2Ø	TACKØ3Ø	05	
TACKØØØ	TACKØ1Ø	04	
SYNØ	DAØ	03	
DRØ	CMDØ	02	
SRØ	ADRSØ	01	
GND	GND	00	
GND	GND	43	0
D14Ø	D15Ø	42	
D12Ø	D13Ø	41	
D1ØØ	D11Ø	40	
D08Ø	D09Ø	39	
D06Ø	D07Ø	38	
D04Ø	D05Ø	37	
D02Ø	D03Ø	36	
D000	D01Ø	35	
GND	GND	34	
GND	GND	33	
B161	B171	32	
B181	B191	31	
B201	B211	30	
B221	B231	29	
B241	B251	28	
B261	B271	27	
B281	B291	26	
B301	B311	25	
GND	GND	24	
GND	GND	23	
CLK1B	CLK1A	22	
CLK1C	SCLK1	21	
GND	GND	20	
GND	GND	19	
NCEØ	FNCEØ	18	
DUAØ	PSELI	17	
DMAHWØ	LMBSYØ	16	
LERØ	WRTØ	15	
LMA3ØØ	LMA31Ø	14	
LMA28Ø	LMA29Ø	13	
LMA26Ø	LMA27Ø	12	
LMA24Ø	LMA25Ø	11	
GND	GND	10	
GND	GND	09	
LMA22Ø	LMA23Ø	08	
LMA2ØØ	LMA21Ø	07	
LMA18Ø	LMA19Ø	06	
LMA16Ø	LMA17Ø	05	
LMA14Ø	LMA15Ø	04	
LMA12Ø	LMA13Ø	03	
LMA1ØØ	LMA11Ø	02	
LMA08Ø	LMA09Ø	01	
GND	GND	00	

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV PG	9/9/80

CONNECTORS 132-1 & 221-2 WERE SPEC AS MATRSDØ, & MATRSRØ. SHEETS 2,5,9,11,12, 14,17 & 18 WERE R02. IN AREA E9 35770 WAS SPEC AS R00.

D.B.P.	GV	4527	M	10-29-80 R01

RELEASED FOR PRODUCTION
ENG. PG DATE 11/17/80

AREA N9 35-770 WAS R01. REVISED SHTS 4,5,6 & 20.

JLV	GV	4650	MS	3-26-81 R02

REVISED SHTS 15 & 16

HN	HN	4717	R	07-13-81 R03

AREA N9: 35-770 WAS R02. REVISED SHTS 1,8,11, 20, 9 & 10

JLV	GV	4772	M	10-1-81 R04

AREA N9, 35-770 WAS R03. REVISED SHTS 1, 8, 9, 10, 11, 19 & 20. SHT 1 ADD TO BACK PANEL MAP FPPFLTØ AT CONN 1, ROW 1 PIN 32 & BWRTØ AT CONN 1, ROW 1, PIN 08.

KR	GV	4908	M	12-15-81 R05 X

REV'D SHTS 1, 2, 4, 5, 7, 8, 9, 11, 12, 14 & 15.

JAH	GV	5090	MS	8-23-82 R06 X

UNLESS OTHERWISE SPECIFIED

SCALE:

TOLERANCE:

DIMENSIONS ARE IN INCHES

.XXX ±.005 .X ±.03
.XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
V. PERRI	E JOHNSON	DES/DFT	7-6-80
R. CERO		SUPV	11-19-80
E. GREENSTEIN		SYS. TEST	11-19-80
P BALAS		ENG	11-19-80
D. FRANKENBERGER		MGR	11-19-80
R. BARKER		QC	11-19-80

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE
CPU-D

TASK 03976

DWG 35-770 R06 D08

SHT 1 -20

REVISION	06	02		01	03	01	01	03	04	02	04	02		02	02	01	01	01	01	03
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

USED IN MANUAL; 47-004

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

35-770 R08
BOARD REV LEVEL

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL.

PRINTING 44-131 4/79

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Oceanport, N.J. 07757

REVISIONS				
IN AREA R6 EFWRT1 WAS CROSS REFERENCED AS 7J7 ONLY				
AH	GU	4327	10/29/80	R01
AREA G-5, D7C10 DID GO TO GND. ADDED CROSS REF. IN AREA G8				
AH	GU	5090	8-23-82	R02

886 SCLR1 → 24K 19-124 SB → DCLRØ 6A3, 7B2, 7A8

→ 24K 19-124 SB → ACLRØ B7, 9A3, 5B6, 9F7, 8J8

→ 24K 19-124 SB → BCLRØ 9C1, 11J7, 12E5, 13K1

107-1 SCLRØB → 23K 19-057 SG → 24K 19-124 SB → CCLRØ M7, 5F5, 6A7, 10D6, 11L1, 12J6, 5J7

6A6 XREQØ → 14M 19-236 SA → XREQØA 8H9

P5 → 14K 270 → 232-1 LMRQØ

14K 19-063 SDF → NC

7D2 CLSØ

FMREQ1 → 05C 19-064 SF → FSOT1 7K3, 7E1

6N8 SOTØA → FSOTØ → 7J4, 5J5, 5A3, 5J7

5M5 FBRTRDØ → 06B 19-055 SG → 8M5 LOAD1

7G1 CLADAØ

FLADR1 → 05F 19-063 SDF → FLADRØ 7K4, 8H3

FLADR1 → 06B 19-055 SG → 05B 19-236 SA → FERDØ 5G6 → BRWRTØ 8H2

05E 19-063 SDF → 05B 19-236 SA → FEFW1 5G8

XRPØSB F9

05A 70 1K P5

06D 19-063 SDF → FLDARB1 NC

FLDARBØ A8, 7K7

EFWRT1 7J7, 5M7

FLDARA1 4B

FLDARAØ 7K5, 8H3

4M3 LMBSY1 → N6 DMASEL1 → 5N8 BRST1 → G8 SMBSY1 → 07C 19-241 SN → HALTØ 4G6, 6H3, 9F7 → 108-S

11 08D 19-057 SG → 10 HALT1 9B5

13 08D 19-057 SG → 12 PSELIA → 217-Ø

DMASEL1 G5, 4J2, 8H4, 10A7, 7J8, 9F8, 5E9

9N6 SCLKIA → 05C 19-064 SF → DMASELØ 15K2, 4J1, 7K9

CCLRØ H2

9L4 AIB11A

9L4 AIB1Ø

G1 ACLRØ

06E 19-131 SDF

06C 19-131 SDF

5G7 ERD1 → 08C 19-126 STTL

FQEOT1 5B4

FQEOTØ 5B7, 7A1

4M3 LMBSY1 → 4E2 FDUA1 → 07D 19-241 SN → DMALM1 4J7 → 05D 19-235 SOR → 9N5 FBØ → 9F6 FSCLK1 → 07E 19-058 SG → CLSTØ 7A2

4E2 FDUAØ → 05B 19-236 SA → DMBSY1 9F8

N4 FLDARBØ

M5 FLDARA1 → 07E 19-058 SG

5G6 FERDØ

5G8 FEFWØ

06B 19-055 SG

5L6 FBRTRD1 → 06B 19-055 SG → 8H8 EOT1

FDEOT1

06D 19-063 SDF → NC

5M8 BRST1

FLMRQØ 15F2

G5, 4J9 SMBSY1

6N8 SOT1A → 09D 19-063 SDF → XRPØSB N4

07D 19-241 SN → DMASM1 4J9

SCALE–	NAME	TITLE	DATE	TITLE CPU-D
TOLERANCE XXX ± .005, X.X ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	D STINE	DRAFT	3-29-78	REFRESH CONTENTION EDMA CONTENTION
		CHK		
		ENGR		

TASK NO. 03976 SHEET OF 2 — 21
DWG. NO. 35-770 R02 D08

REVISIONS

UNLESS OTHERWISE SPECIFIED	
SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
	E. JOHNSON	DES / DFT	
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE CPU-D
INSTRUCTION REGISTER YD & YS FIELDS

TASK 03976
DWG 35-770 D08
SHT 3 - 20

NOTES

PERKIN-ELMER

REVISIONS				
AREA J2, ADDED 1K RES. IN LOC. 23K. AREA 18, ADDED 789				
ALL	5090	MS	8-23-82	R01

P5 71 20K 1K 11 → P5Z J3

5B4 DUAI

117-Ø DUAØ 05 23K 19-057 SG 06

9N6 CLKØB

DS D Q 20J 19-063 SDF DC 04 02 05 03 06 01 → 2F8, FDUAI, FDUAØ 2K7

5H4 DUAØ 02 22K 19-234 SN 03 01 → FDUSKP1 9F8

2H1 ACLRØ

DS D Q 20J 19-063 SDF DC 10 12 09 11 08 13 → NC

222-1 RDØ11 01 13R 19-236 SA 02 03 → RDØ11D 6A5,12E8,7A6

14E9 16XRP 04 13R 19-236 SA 06

121-1 RDØE1 05

09 15M 19-057 SG 08 → RDØ1ØD A7

11 15M 19-057 SG 10 → RDØ21D 6A5,12E8

RDØ2ØD A7,7A6

10D1 XXRP 03 13R 19-236 SA 08

115-5 PA3Ø1 10

PA3ØID 6A1

05 15M 19-057 SG 06 → PA3ØØD 6A1

01 12M 19-058 SG 12

02 13 09 14H 19-055 SG 06 → DMEMØ 6A5

12C8 RDØ31D

E6 RDØ2ØD 09

10 12M 19-058 SG 08

E5 RDØ1ØD 11

05

09 14R 19-057 SG 08

09 17D 19-060 SG 08 → PMEMI 6A2,G6,9B4,9F7

10C1 GGDIRØ 10

10C3 2IRØ 12

13 ← 211-5

6R2 GSIRØ 09 17E 19-236 SA 08

10G5 CMR2Ø 10

2R6 DMASELØ 09 21H 19-055 SG 08

10 → 15K 19-057 SG 02 → PDUAI 9B8,10J5,6H2 10M4

PDUAØ 6A5,10H6,10D6,9B9

12 21H 19-055 SG 11 → 08D 19-057 SG 04 → DDUAI 5J3,7J5,7J7

DDUAØ 5B3

2N6 DMASEL1 13

216-Ø LMBSYØ → 23K 19-057 SG 12 → LMBSY1 9B9,6G,2G7,2G5

P5 72 23K 10 1K E1 P5Z → 18J 19-236 SA 05 04 06 → LMBSYØA G6

04 12E 19-236 SA 06

6C3 DAWT1 05

01 CPU 13

5G6 FERDØ 10 DMA 09

29M 19-126 SG 08 → WRTØ 215-Ø

103-5 MATSTOPØ 01 20C 19-236 SA 02 03 → GMATSTOPØ 9H2,9MZ

P5 70 08A 12 47K 2200 pF 10 08A 72 11 71 08A

P5 70 09A 12 1K

DS D Q 09D 19-063 SDF DC 10 12 09 11 08 13

14 19 15 EXC EXR 08A 19-042 Q Q1 13 NC 04

5N8 BRST1 02 01 11 03

8M5 LOADI 08 09E 19-234 SN 10

8M5 ANSI 09

09C 19-236 SA 08

10 04R 19-125 SBO 01 02 03 → EOTØ 8G8

2K5 HALTØ 12 17E 19-236 SA 11

D8 PMEMI 13

116-5 ENMAAØ

9B5 05 22K 19-234 SN 04

02 21H 19-055 SG 03 06

01 9H5 FERI 09

117-5 CWRØ 10 20H 19-059 SA 08

N3 LMBSYØA 11

N2 LMBSY1 08 22K 19-234 SN 10

9H5 FERØ 09

03

6A2 CWRØ 04 20H 19-059 SA 06

05

212-5 PSBCØ

112-5 MSBCØ

9B4 PSBCØ 09 23K 19-057 SG 08 → PSBC1 9B7

9B5 MSBCØ 11 23K 19-057 SG 10 → MSBC1 9B7

P5 71 15K 1K 11

231-1 SMBSYØ 09 15K 19-057 SG 08 → SMBSY1 9B7,2F8

12 22K 19-234 SN 13

2K8 DMASM1

9B5 GENMAAI

2K7 DMALM1

01 13 12 11 06 05 04 03 02 NC 10 09 CPU MAT DMA → 22M 19-062 SG

08 → LERØ 115-Ø

01 13 12 11 06 05 04 03 02 NC 10 09 CPU MAT DMA → 23M 19-062 SG

08 → SERØ 131-1

SCALE—	NAME	TITLE	DATE
TOLERANCE .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	D STINE	DRAFT	3-29-78
		CHK	
		ENGR	

TITLE CPU-D LOCAL MEMORY TIMING & CONTROL

TASK NO. 03976 SHEET OF 4 — 20

DWG NO. 35-770 R01 D08

PERKIN ELMER

Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
IN AREA M 7 02D04 WAS CONNECTED TO 03A10.				
DJ	9927		10-29-80	R01
AREA J1 ADDED CONN. 00A73 TO 00B03.				
JLW	4G30	MS	3-25-80	R02
AREA J-7, ADDED CROSS REF. &B8 TO BRWRT1. ADDED IC 15K69				
JAH	5070	MS	8-23-82	R03

H3 ENAOSCØ

01A 19-057 SG

00B 19-055 SG

68 PF (9 73 00A)

01B 19-235 SOR

E4

DOSCØ

75 00A 2.2K

74 00A 1K

P5

00B 19-055 SG

06 00A 76 1K

72 00A 10

05 00A 77 4.7uH

80 00A 02 9-35 pf

M6 FBRTRDI 03
M4 FDRDY1 04
EJ4 FLADR1 05

00D 19-058 SG

01D 19-236 SA

7F2 STI 09

02D 19-055 SG

9N5 CLK1

DS 00E 19-064 SF

NC

01A 19-057 SG

02

2F5 FSOTØ 12
G5 FERDI 13

02D 19-055 SG

R8 BRST1 04
05
4N2 DDUAØ 09
2G7 FQEOT1 10
4A2 DUAI 11

01E 19-241 SN

06

J7 BRWRT1 01

02D 19-055 SG

03 09

H2 FDAI 02
H3 FDAØ 01
G7 ERDI 02
K2 FDBI 04
G8 FEFW1 05
01
G8 FEFWØ 02

00H 19-060 SG

06

00D 19-058 SG

12

00D 19-058 SG

08

15	16	17	
1	0	0	RD HW
0	1	0	WRT HW
1	1	0	RD/SET
1	0	1	RD FW
0	1	1	WRT FW
1	1	1	BRST RD
0	0	1	BRST WRT

P5 71 01A 1K 11 5XRP

DOSCØ F1

01C 19-064 SF

03 04 05 06 15

01A 19-057 SG

03 04

ZH2 CCLRØ 10

01D 19-236 SA

09 08

01B 19-235 SOR

08 ENAOSCØ B1,8H3

10

MEMORY TO EDMA-CONTROL

4R2 DDUAI 01
9N5 CLKIF 02

01D 19-236 SA

03

L6 FBRTRDI 03
4A1 DUAØ 04

03C 19-059 SA

06
05
FDRDYO
7D1 CLRDYØ

XRPØ5 7L2

12 01A 1K 70 P5

DS 00E 19-064 SF

10 09 07 14

FDRDY1 B2

XRPØ5

16J4 RDATIS1

02 04 05 06 01

02H ERD 19-063 SDF

03H 19-059 SA

12 13

FERD1 8B1, 8H4, A3, 17M1, 7K6

2J4 FLADR1
2G1 ACLRØ

FERDØ 4K4, 7K5, 8H4 2K5, 2A8

2F5 FSOTØ 04

03D 19-236 SA

06

03C 19-059 SA

08

BRTRD1 05

8H2, 7B1

03B 19-057 SG

01 02 BRTRDØ 7E1

DS 02E 19-064 SF

03 01 02 06 15

FBRTRDØ 2G4, 8H2

FBRTRD1 B2, H4, 2B8

2F7 FQEOT Ø

02H EWRT 19-063 SDF

08

2F4 FSOTØ 09

03D 19-236 SA

08

03C 19-059 SA

12

BRWRT1 B3, 8H2, 8B4, 8B8

2H2 CCLRØ

03 15K 19-057 SG 04 BWRTØ 108-1

2R5 EFWRT1 04

02D 19-055 SG

06

8G8 EOT1 05

FBRWRT1 NC

FBRWRTØ 8H3

12 03D 19-236 SA 11

BRSTØ 0114-6 TPB

03B 19-057 SG 04 BRST1 B3, 2G6, 2B9, 4H5

P5 70 00K 1K 12 09 07 ENB

NC 02 I0 02M Z0 03
NC 05 I1 19-118 Z1 06
NC 11 I2 Z2 10 NC
NC 14 I3 Z3 13 NC

QUAD BUS TRANSCEIVER

B0 B1 B2 B3

P5 72 01K 180 10
131-2 DMA16Ø
71 01K 180 11
132-2 DMA17Ø
72 02K 390 10
71 02K 11

01 04 12 15 NC NC

EDMA TO MEMORY OPERATION-DECODE

01 22R 19-057 SG 02 DMAHWØ 116-Ø

09

12 19-060 13 SG 08 DMAR3Ø 121-2

2N6 DMASEL1

TPG 116-6

05 01A 19-057 SG 06 FDA1A TPA 115-6

FDAAØ 7B1

FDA1 B4, 8B1, 7B1

FDB1 B4, 8B3

FDAØ B4, 8B4

FDC1 8B3

FDCØ 8B2

SCALE–	NAME	TITLE	DATE
TOLERANCE .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	A. WILLIAMS	DRAFT	3-14-80
		CHK	
		ENGR	

TITLE SCHEMATIC
CPU-D
EDMA TO LOC.
MEM CONTROL

PART NO 03976
DWG NO 35-770R03D08
SHEET 5 OF 20

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
AREA F6; ADDED CAP. 02A CONNECTED TO 05ADB. AREA E9; ADDED CAP. 04A CONNECTED TO 05A13				
LTR	4650	MS	3-26-81	R01

MEMORY OPERATION DECODE

EDMA PROTOCOL LOGIC

NOTES:
1. NORMALLY STRAPPED TO GND.

SCALE—	NAME	TITLE	DATE
TOLERANCE: XXX ± .005, XX ± .02, X ± .10, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	A. WILLIAMS	DRAFT	2-15-80
		CHK	
		ENGR	

TITLE CPU-D
PROC. MEM. OP. DECODE
EDMA PROTOCOL LOGIC

TAB NO. 03976 SHEET OF
DWG NO. 35-770 R01 D08 6 — ?0

PERKIN ELMER
Computer Systems Division
Oceanport N.J 07757

REVISIONS				
AREA B-2, 11A05 DID GO TO LMDR1 (10C, 12N9).				
AA	4/1/80	SO30 mls	8-23-82	ROM

5H2 FDA1
5J1 FDAAØ
5J6 BRTRD1
2F7 FQEOTØ
2H1 DCLRØ
2M8 CLSTØ
11B 19-058 SG
08E 19-059 SA
12A 19-236 SA
5K6 BRTRDØ
2E4 FSOT1
11A 19-057 SG
CLRDYØ 5J5
CLSØ 2A5
STI 5B3
CLADAØ 2G5

C6 RMSR1
9C9 STMDR1
09E 19-234 SN
MDSBØ 209-5
11A 19-057 SG
12B 19-055 SG
MDHSA1 216-5
6G2 FBIRØ
6H9 EVDAT1
6L2 GRD1
6G2 FEIRØ
14B 19-059 SA
MDLSA1 109-5
9L2 DSTOPØA
12A 19-236 SA
6L3 RDFWØ
9L4 AIBI1
10A
19-126
MDHCLKØ 110-5
12B 19-055 SG
09A 19-058 SG
AMDRCKØ 3H8
6A2 RDØØØD
4E5 RDØ11D
4E6 RDØ2ØD
12D7 RDØ31D
12E5 DRFALTØ
07C 19-241 SN
RMSR1 A2
11A 19-057 SG
READ MAT STATUS REGISTER
(PR2, RFAULT)
6L3 GRDØ
6G2 FEIRØ
12B 19-055 SG
MDLCKØ 214-5
XXRD 10D1
10D 19-063 SDF
NC
9R8 MCLKØ
9N6 SCLK1A
2H1 DCLRØ
09B 19-236 SA
CLSTAØ 203-5

5M3 XRP05
10D7 ENCE1
R5 EEDCLKØ
R7 OEDCLKØ
09C 19-236 SA
D01H 19-063 SDF
FENCE1 15E2
NC

2G4 FSOT1
02B 19-057 SG
LDMALØ 16K7,15J6
2F5 FSOTØ
DDUA1
2J5 FLADRØ
05H
19-126 SG
ILDMAØ 16K7,15J6
5G6 FERDØ
2M5 FLDARAØ
9N4 CLK1D
4R2 DDUA1
5G5 FERDI
05B 19-236 SA
EEDCLKØ 17M1,K2
07H
5G8 FEFWØ
15B9 DL3Ø1
4R2 DDUA1
2R5 EFWRT1
2R4 FLDARBØ
HW WRT
READ
FW WT
19-062 SG
OEDCLKØ 18M1,K2
2R6 DMASEL1
00B 19-055 SG
DMAWRTØ 17M6, 18M6
09A 19-058 SG
LWRTØ 113-5
10B 19-057 SG
6D4 EDAT1
6D3 DAWT1
2R6 DMASELØ
09A 19-058 SG
LHWRTØ 213-5

SCALE–	NAME	TITLE	DATE	TITLE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	A. WILLIAMS	DRAFT		CPU-D MEMORY CONTROL LOGIC
		CHK		
		ENGR		

TABP NO. 03976 | SHEET 7 OF 20
DWG NO. 35-770R01 D08

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
DELETED 19-066A 19J 06 FROM SPARES TABLE				
JLV	41	4772 M	10-1-81	R01
DELETED 19-055 19H08 FROM SPARE TABLE.				
KRW	41	A900	19 12-15-81	R02 X
AREA B-D 7&8, ADDED 18J & 19H. IN SPARES TABLE DELETED FOLLOWING: 19-055(19H-11), 19-235(21C-6), 19-226(18J-3), 19-057(15K-4), 19-236(14M-6), ADDED '87 CROSS REF. (AREA H-2) TO ENXCVRØ.				
JAH	41	5090	MG	8-23-82 R03 X

FERDI 5G6
FEFWØ 5G6
DL3Ø1 15B9
FDA1 5H12
FDCØ 5M2
FEFWI 5G8
FDBI 5K2
FDCI 5M2
FDAØ 5H3
BRWRTI 5J7
SCLRI 2E1
FPFØ 6J8
FPGI 6J8
PROSCI 6M9
ENXCVRØ G2
BRWRTI 5J7
DMASELI 2M6
BRTRDI 5J6
BRWRTØ 2K5
BRWRTI 5J7
FBRTRDØ 5M5
FBRWRTØ 5M7
ENAOSCØ 5H3
FLADRØ 2J5
FLDARAØ 2M5
XREQØA 2E3
FERDØ 5G6
DMASELI 2R6
FERDI 5G6
DANSI
129-2 ANSØ
130-2 LOADØ
P5
4R5
127-2 EØTØ
2B8, 5M7 EØTI
5G7 SOTØA
2G1 ACLRØ

EMDENBØ 17M1
OMDENBØ 18M1
ENXCVRØ 16G2, 15F2, B7
ENIDØ 15F2
RESCØ 6N6
HOST1 6A7
GEOT1 6A8
FPFØ 6J8
ANSI 4H5
LOAD1 2G5, 4H5
P5
P5
P5

10E 19-126 SG
04E 19-062 SG
08C 19-126 SG
03M 19-118 QUAD BUS XCVR

P/O DMA PROTOCOL LOGIC

PART NO.	REF DESIGNATION	SPARE OUTPUT NO.
19-126	24M	6
19-063	23J	5/6
19-241	22H	5
19-165	22A	5/6
19-235	21K	3,6
19-235	21C	8,11
19-063	20E	5/6
19-059	19B	6
19-064	19E	5/6
19-057	18B	,12
19-236	17A	6
19-036	16P	6,8,11
19-062	16R	12
19-067	16B	7/9
19-126	16A	6
19-057	15K	6,12
19-055	15F	6
19-063	15B	5/6
19-063	14F	5/6
19-057	14E	2,6
19-057	14D	12
19-055	13A	8
19-057	12A	4
19-236	12E	3
19-055	12A	3
19-057	11A	2,
19-057	10B	4,6
19-234	09E	13
19-236	09C	11
19-236	09B	11
19-057	08D	2
19-055	05D	8,11
19-125	04E	6
19-069	04C	5/6
19-057	03B	6
19-241	01E	5
19-235	01B	3,6
19-057	01A	10,12

SCALE –
TOLERANCE: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
A. WILLIAMS	DRAFT	2-29-80
	CHK	
	ENGR	

TITLE SCHEMATIC CPU-D
TASK NO. 03976
DWG NO. 35-770103D48
SHEET 8 OF 20

PERKIN ELMER
Computer Systems Division
Oceanport, N.J 07757

CLOCKSINGLE STEP CONTROL

REVISIONS				
IN AREA N5 MSTOPØA WAS NOT CROSS REFERENCED TO 12B2				
JLM	4527		10/29/80	R01
ADDED 11K1 TO "CLKIE" & "FBØ" AREAS N4 & N5.				
JLM	4772	M	10-15-81	R02
AREA J4 RES 19A WAS 330Ω.				
NAU	4928	M	12-15-81	R03
AREA B,C,D-8 & 9, 16D/0 DID GO TO UMDRI. ADDED 21C & 19M.				
NAU	5090	MS	8-23-82	R04

SCALE—
TOLERANCE: XXX ± .005; XX ± .02; X ± .03; ANGLES ± 1°; UNLESS OTHERWISE SPECIFIED

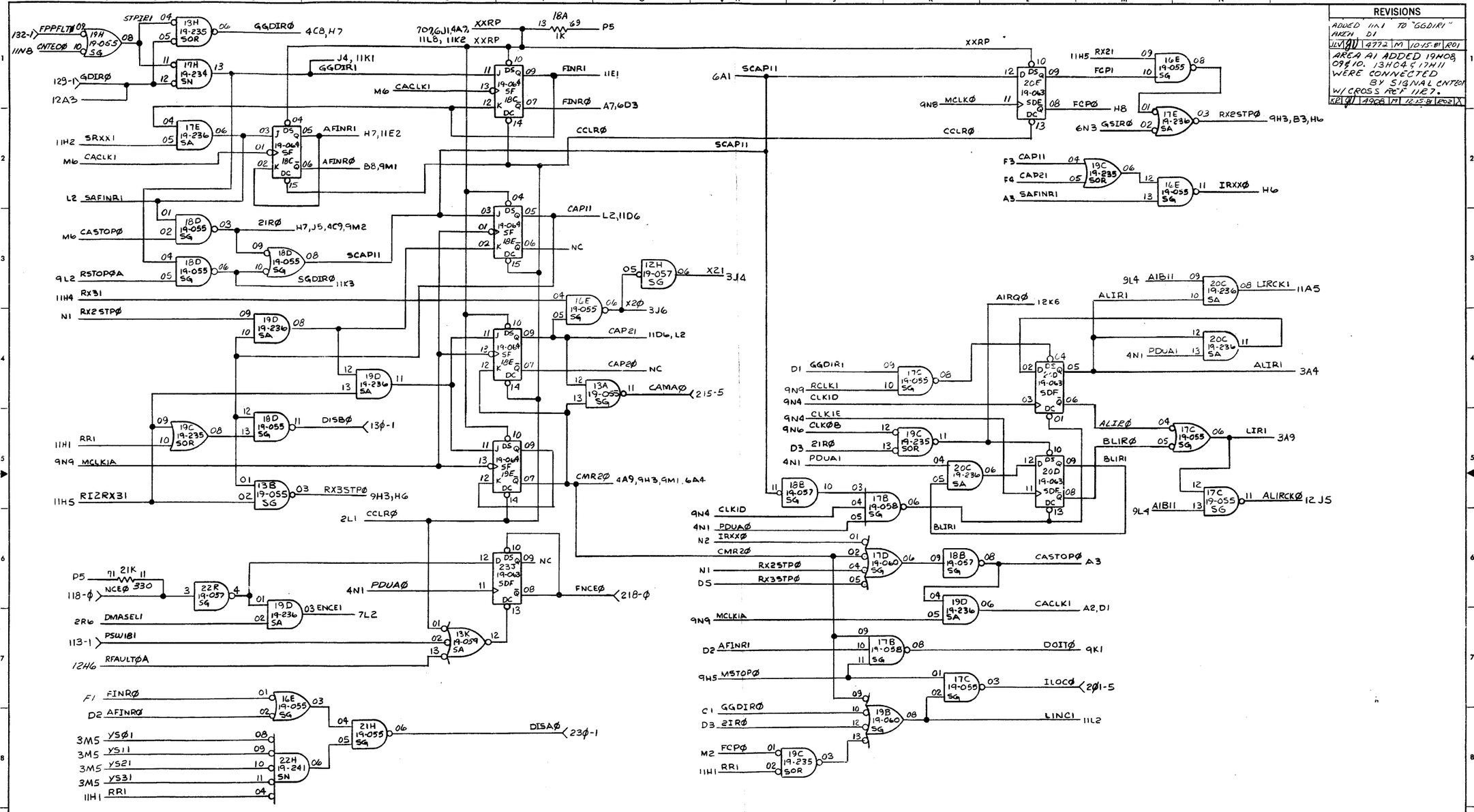
NAME	TITLE	DATE
BSTINE	DRAFT	
	CHK	
	ENGR	

TITLE CPU-D
CLOCKS & STOPS

DWG NO. 03976
REV 35-770 rev D08
SHEET 9 OF 22

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
ADDED 11N1 TO "GGDIR1" AREA D1				
JLV	4772	M	10-15-81	R01
AREA A1 ADDED 19N08, 09 & 10. 13H04 & 17H11 WERE CONNECTED BY SIGNAL CNTE0 W/CROSS REF 11R7.				
KPJ	4908	M	12-15-81	R02



SCALE–	NAME	TITLE	DATE	TITLE CPU-D
TOLERANCE XXX ± .005, XX ± .02, X ± .09, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	A. WILLIAMS	DRAFT	2-15-80	CALCULATE ADDRESS LOGIC
		CHK		
		ENGR		
				TABR NO. 03976
				SYS NO. 35-770 R02D08
				SHEET 10 OF 25

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS					
IN AREA A7 & A8 085 & 08T WERE NOT SPEC.					
037	BV	4527		10-29-80	R01
AREA K2: 19J01 WAS CCLR0 DESTINATION 2L1. ADDED 14J					
111	BV	4772	M	10-1-81	R02
AREA N8 18B06 WAS CONNECTED TO 17H11 BY SIGNAL CNTE01 W/ CROSS REF 10A1. AREA N7 ADDED 10A1 TO CNTE0Ø					
KE	HH	4908	M	12-15-81	203 X
AREA B7-B9, IC's 085 & 08T WERE 21-099 F02, 10K;					
4M	VU	5089	VMS	8-20-82	R04 X

REPEAT COUNTER

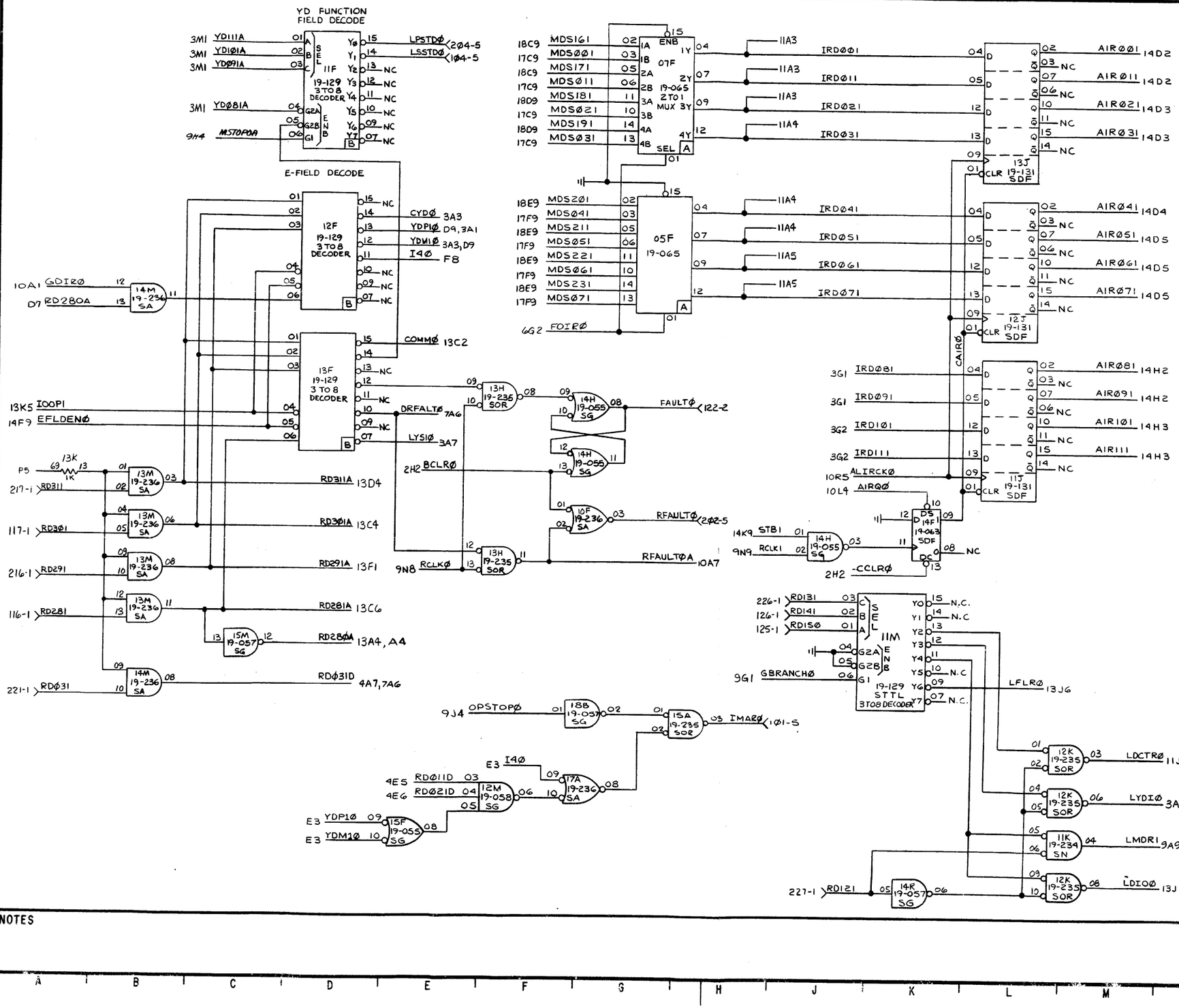
LENGTH REGISTER

SCALE—	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	A. WILLIAMS	DRAFT	
		CHK	
		ENGR	

TITLE: CPU-D

TASK NO. 03976 SHEET OF 11 — 20

DWG NO. 35-770 R14 D08



REVISIONS

IN AREA B2 11F06 WAS SPEC AS CONNECTED TO 13M01 AREA A5.					
WP	AW	4527		10-29-80	R01
AREA N-9, CROSS REF. ON "LMDR1" WAS 7A2.					
JAH	AW	5090	MS	8-23-82	R02 X

UNLESS OTHERWISE SPECIFIED

SCALE:		TOLERANCE:	
DIMENSIONS ARE IN INCHES		.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME		TITLE	DATE
	A. WILLIAMS	DES / DFT	3-4-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC CPU-D
INSTRUCTION REG
DEST. DECODE
SOURCE DECODE

TASK 03976 SHT 12 -20
DWG 35-770 R02 D08

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

I/O CONTROL

I/O DATA

SKIP F/F

CONTROL IN F/F

CONTROL OUT F/F

DATA F/F

SYNC F/F

18M 19-118 QUAD BUS TRANSCEIVER

18R 19-118 QUAD BUS TRANSCEIVER

19M 19-118 QUAD BUS TRANSCEIVER

19R 19-118 QUAD BUS TRANSCEIVER

NOTES:
1. INSTALL JUMPER FROM A TO B IN ORDER TO INSURE A 350 ns MINIMUM WIDTH ON THE ADDRESS CONTROL LINE (ADRSO)

SCALE—	NAME	TITLE	DATE
TOLERANCE	E. JOHNSON	DRAFT	
		CHK	
		ENGR	

TITLE CPU-D I/O CONTROL AND DATA

TAPE NO. 03976 SHEET OF

DWG NO. 35-770 D08 13

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
IN AREA R5 & R8 055 & 05T WERE NOT SPEC.				
JJR	GV	4527	10/29/80	R01
AREAS N-L & N-B. IC'S 055 & 05T WERE 21-039 F02 10K.				
HH	GV	5090	MS 8-23-82	R02

P5 01 — 70 — 16A 12 — 1K — 19

S BUS DRIVERS

16A 19-240

111-4	S161	02	18	S161A 13N7
211-4	S171	04	16	S171A 13N7
110-4	S181	06	14	S181A 13N7
210-4	S191	08	12	S191A 13M7
108-4	S201	17	03	S201A 13L7
208-4	S211	15	05	S211A 13L7
107-4	S221	13	07	S221A 13L7
207-4	S231	11	09	S231A 13L7

19A 19-240

105-4	S241	02	18	S241A 13J7
205-4	S251	04	16	S251A 13J7
104-4	S261	06	14	S261A 13J7, 11J6
204-4	S271	08	12	S271A 13J7, 11J6
102-4	S281	17	03	S281A 13H7, 3D1, 3D5, 11J5
202-4	S291	15	05	S291A 13G7, 3D2, 3D6, 11J5
101-4	S301	13	07	S301A 13G7, 3D3, 3D7, 11J4
201-4	S311	11	09	S311A 13G7, 3D4, 3D8, 11J4

"B" BUS MULTIPLEXORS

20R 19-196 2TO1 MUX

13N9	IO161	02	1A
12N1	AIRØØ1	03	1B
13N7	IO171	05	2A
12N1	AIRØ11	06	2B
13N9	IO181	11	3A
12N2	AIRØ21	10	3B
13M9	IO191	14	4A
12N2	AIRØ31	13	4B

01 SEL; ENB 15

1Y 04 B161 132-Ø
2Y 07 B171 232-Ø
3Y 09 B181 131-Ø
4Y 12 B191 231-Ø

21R 19-196 2TO1 MUX

13K9	IO241	02	1A
12M4	AIRØ81	03	1B
13J9	IO251	05	2A
12M4	AIRØ91	06	2B
13J9	IO261	11	3A
12M5	AIR1Ø1	10	3B
13J9	IO271	14	4A
12M5	AIR111	13	4B

01 SEL; ENB 15

1Y 04 B241 128-Ø
2Y 07 B251 228-Ø
3Y 09 B261 127-Ø
4Y 12 B271 227-Ø

21M 19-196 2TO1 MUX

13M9	IO201	02	1A
12N3	AIRØ41	03	1B
13L9	IO211	05	2A
12N3	AIRØ51	06	2B
13L9	IO221	11	3A
12N3	AIRØ61	10	3B
13K9	IO231	14	4A
12N4	AIRØ71	13	4B

01 SEL; ENB 15

1Y 04 B201 130-Ø
2Y 07 B211 230-Ø
3Y 09 B221 129-Ø
4Y 12 B231 229-Ø

20M 19-073 4TO1 MUX

13H9	IO281	06	INPUTS1 0
3M1	YDØ81A	05	1
11N3	LEN281	04	2
3M3	YSØ1	03	3
		02	BSEL
		15	2STB
		01	1STB
		14	ASEL
13G9	IO291	10	INPUTS2 0
3M1	YDØ91A	11	1
11N2	LEN291	12	2
3M3	YS11	13	3

1Y 07 B281 126-Ø
2Y 09 B291 226-Ø

20K 19-073 4TO1 MUX

13G9	IO301	06	INPUTS1 0
3M1	YDIØ1A	05	1
11N1	LEN3Ø1	04	2
3M3	YS 21	03	3
		02	BSEL
		15	2STB
		01	1STB
		14	ASEL
13G9	IO311	10	INPUTS2 0
3M1	YDI11A	11	1
11		12	2
3M3	YS 31	13	3

1Y 07 B301 125-Ø
2Y 09 B311 225-Ø

STB	B	A	"B" MUX
0	0	0	IO
0	0	1	YDI
0	1	0	LENGTH
0	1	1	YSI
1	X	X	HIZ

RD "B" SOURCE DECODE

ULIOØ 13J1

11K 19-234 SN; 20H 19-059 SA → UMDR1 9B8

BRANCHØ 9G1

13K 19-059 SA

229-1 RD271
228-1 RD261
128-1 RD251
127-1 RD240
225-1 RD161

12R 19-129 3TO8 DECODER

01	A	Y0 15 NC
02	B	Y1 14 NC
03	SEL	Y2 13
		Y3 12
		Y4 11
04	G2A	Y5 10 NC
05	G2B	Y6 09 NC
06	G1	Y7 07

ULYSIØ 3A7

19H 19-055 SG (01, 02 → 03)

ASEL1

19H 19-055 SG (04, 05 → 06)

14J 19-060 SG (09, 10, 12, 13 → 08)

23K 19-057 SS (08, 03 → 04) STBØ

STB1 12H6

P5 71 16XRP 1K 9A6

13R 19-236 SA (12, 13 → 11) EFLDENØ 12A5

9G1 BRANCHØ

S BUS BUFFERS

P5 01 — 055 — 21-099 F05 5ØΩR

02	MD5170	18C7
03	MD5190	18D7
04	MD5210	18F7
05	MD5230	18F7
06	MD5250	18H7
07	MD5270	18J7
08	MD5290	18L7
09	MD5310	18L7
10		

P5 01 — 05T — 21-099 F05 5ØΩR

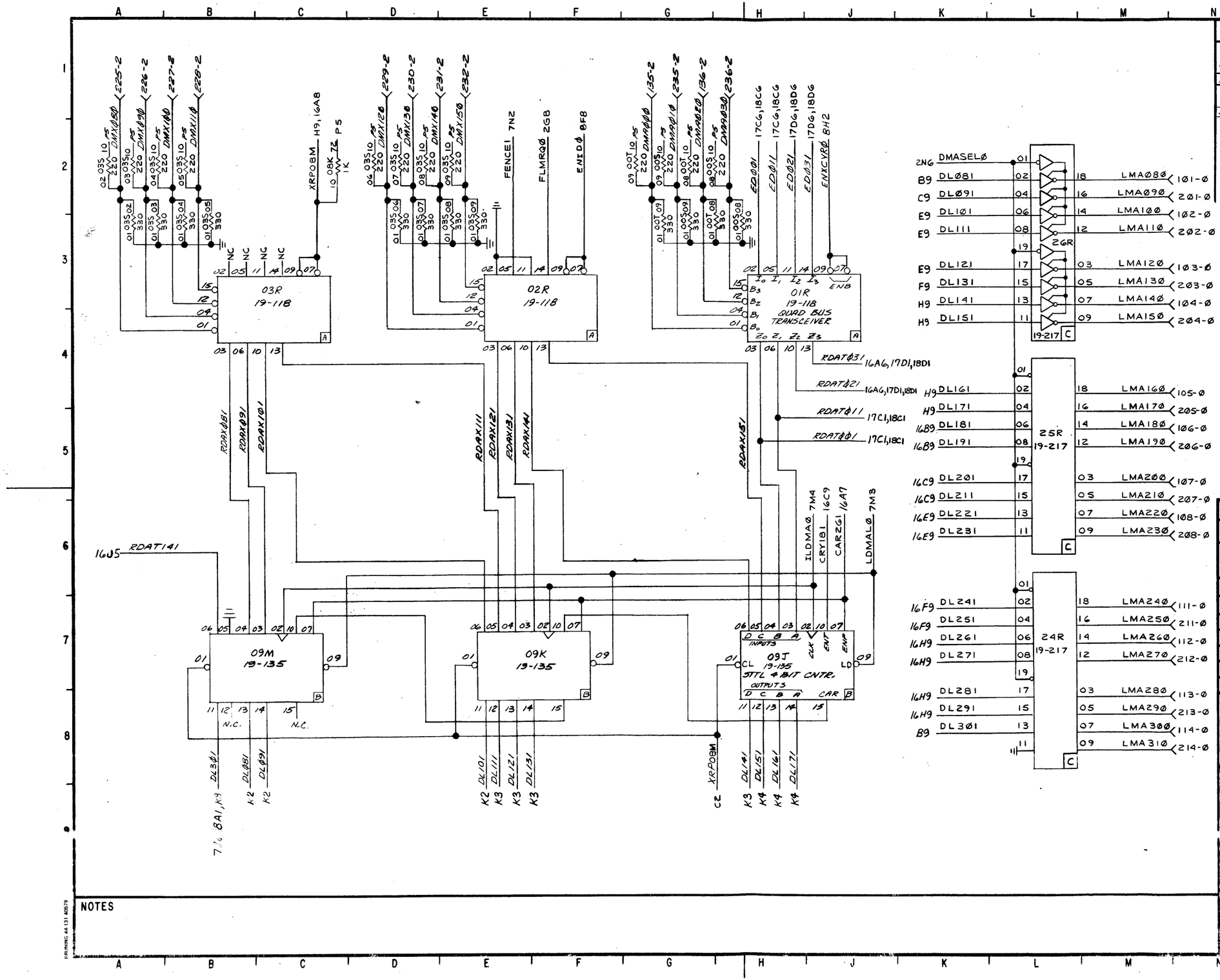
02	MD5160	18C7
03	MD5180	18D7
04	MD5200	18E7
05	MD5220	18F7
06	MD5240	18H7
07	MD5260	18J7
08	MD5280	18K7
09	MD5300	18L7
10		

SCALE – | TOLERANCE .XX ± .005, .X ± .02, ANGLES ± 1° | UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
E. JOHNSON	DRAFT	
	CHK	
	ENGR	

TITLE CPU-D
"S" BUS BUFFERS
"B" BUS DRIVERS
"B" SOURCE DECODE

TASK NO. 03976 | SHEET OF 14
DWG NO. 35-770R02 D02



REVISIONS

RELABELED RESISTORS AS FOLLOWS : 005, 035, & 007 WERE 007, 037, & 005 RESP					
HN	MH	4717	R	07-13-81	R01
01R07&09 AND 02R07 & 09 WERE CONNECTED TO ENXCVRØ.					
JAH	JJ	5090	MS	8-23-82	R02

UNLESS OTHERWISE SPECIFIED

SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
	E. JOHNSON	DES / DFT	1-14-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

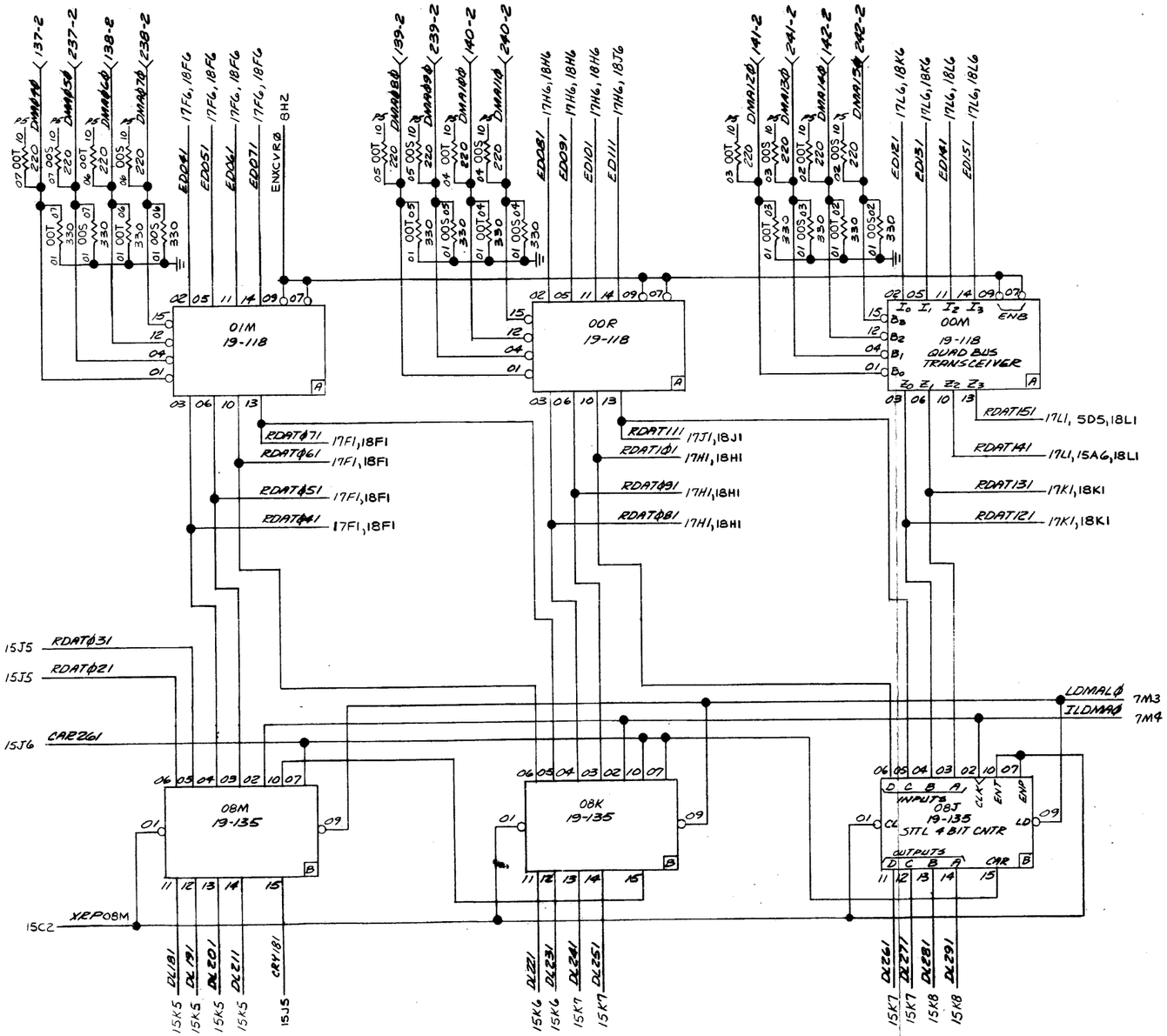
Computer Systems Division
Oceanport, N.J. 07757

TITLE
CPU-D
EDMAS DATA XCVRS
EDMAR ADDRESS 08-17

TASK 03976 SHT 15-20
DWG 35-770 R02 D08

NOTES

FIRNING 44131 40579



REVISIONS

RELABELED RESISTORS AS FOLLOWS : 005, 035, 007 WERE 007, 037 & 008 RESP				
HN	[illegible]	4717	R	07-13-81 R01

NOTES

UNLESS OTHERWISE SPECIFIED

SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
	E. JOHNSON	DES / DFT	1-14-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

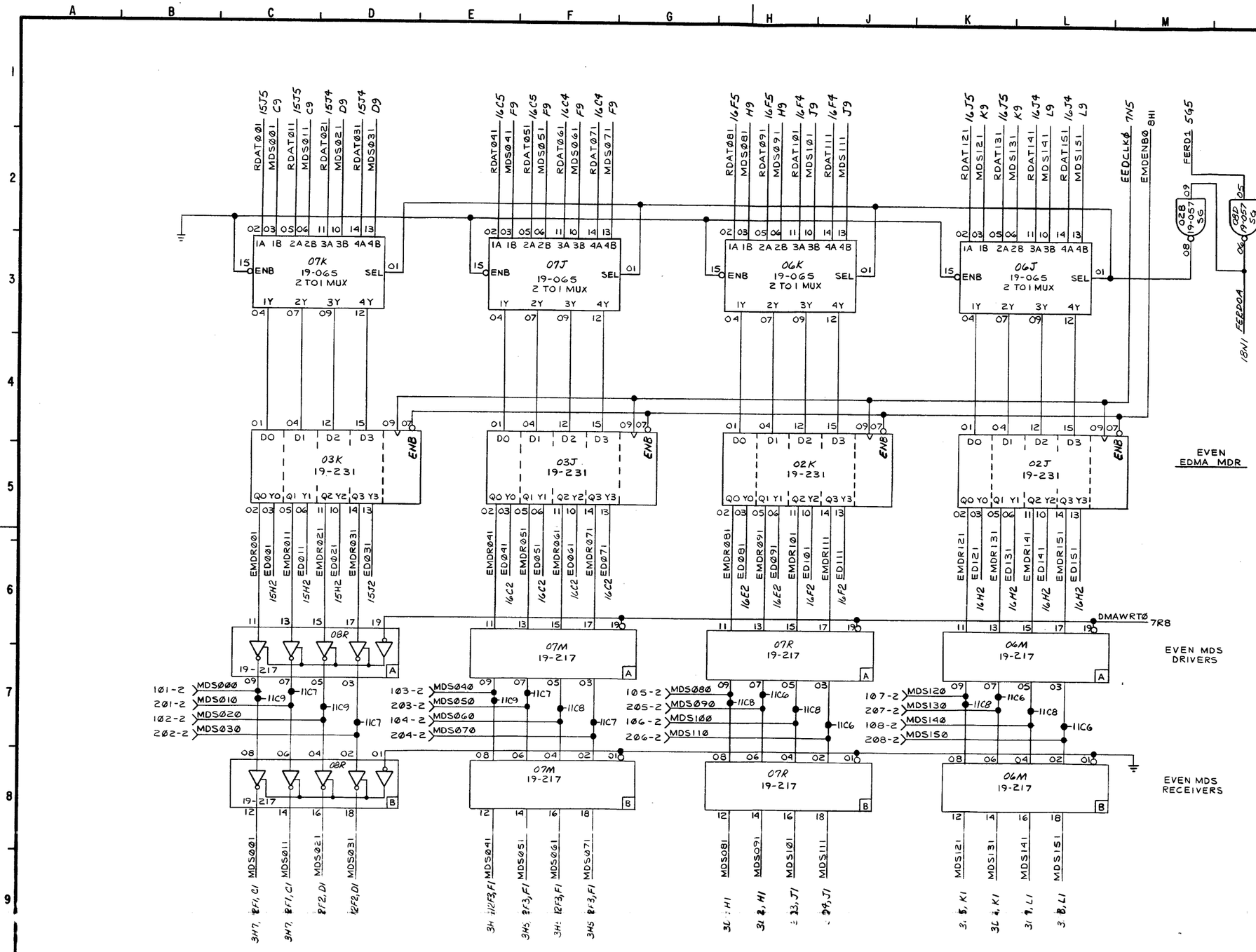
Computer Systems Division
Oceanport, N.J. 07757

TITLE CPU-D

EDMAS DATA XCVRS
EDMA ADDRESS 18-29

TASK 03976 SHT 16-20

DWG 35-770 R01 D08



REVISIONS				
IN AREAS C7, F7, H7 & L7 "MDS" LINES WERE NOT CROSS REFERENCED TO ANY OTHER SHEET.				
LTR	BY	4527		10-29-80	R01

NOTES

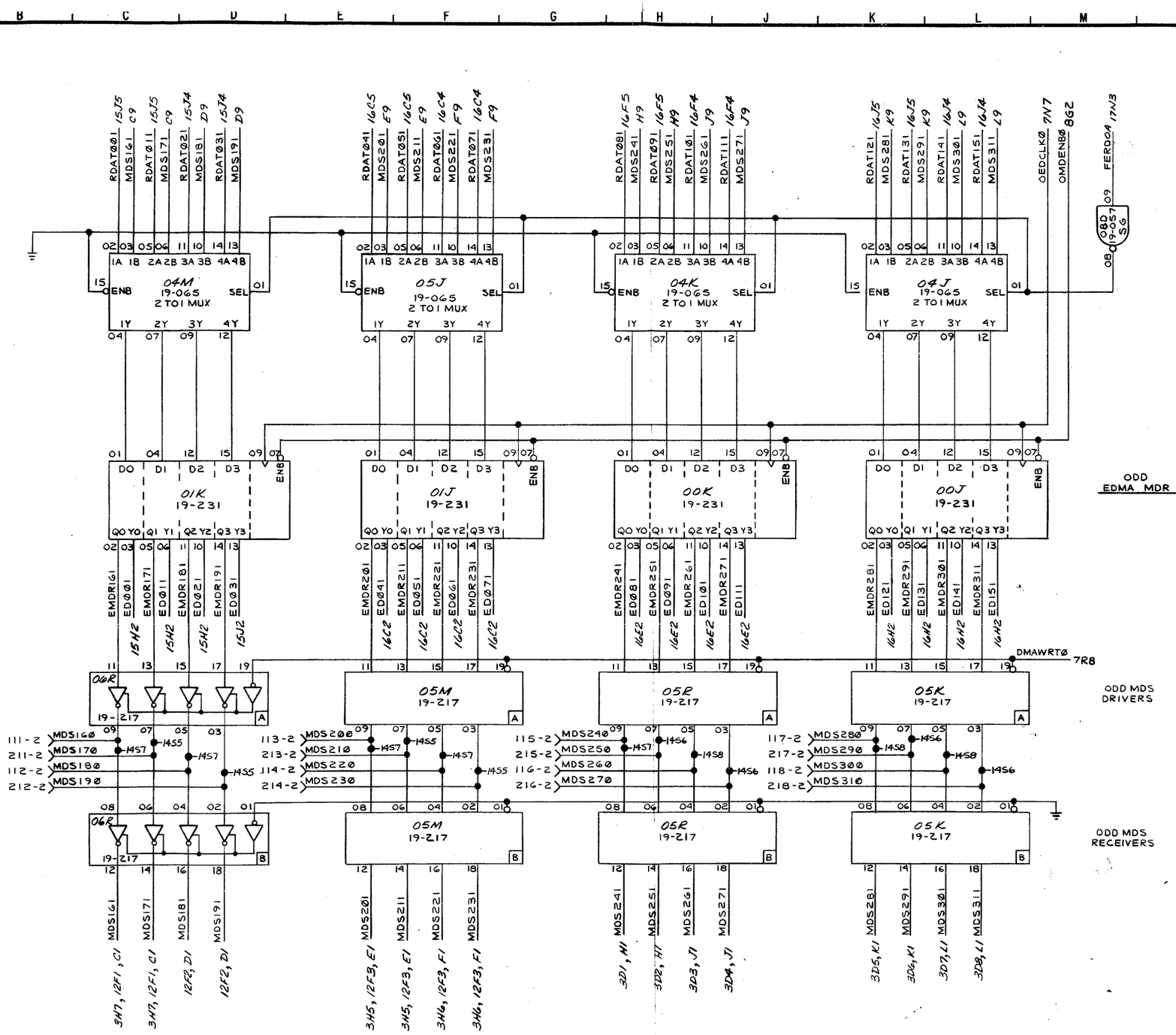
UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME	TITLE	DATE
E. JOHNSON	DES / DFT	
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-D
EDMA MDR 0/15

TASK 03976	SHT
DWG 35-770 R01 D08	17 -20



REVISIONS				
IN AREAS C7 F7 H7 & L7 "MDS" LINES WERE NOT CROSS REFERENCED TO ANY OTHER SHEET.				
N.P		4527		10-29-80 R01

NOTES

UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME	TITLE	DATE
E. JOHNSON	DES / DFT	
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-D
EDMA MDR 16-31

TASK 03976 | SHT 18-20
DWG 35-770 R01 D08

CROSS REFERENCE NET#, MNEMONIC, SHEET#

NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.
0001	AIRØØ1	12	0063	CLKIC	9	0125	DL2Ø1	16	0187	EDØ11	15	0249	ENCE1	10	0311	FQEOTØ	2	0373	IO271	13	0435	MDSØ2Ø	17	0497	MCLKØ	9	0559	RCLK1	9	0621	5311	14	0683	XREQØØ	6
0002	AIRØ11	12	0064	CLK1D	9	0126	DL211	16	0188	EDØ21	15	0250	FADV1	9	0312	FLADE1	2	0374	IO281	13	0436	MDSØ3Ø	17	0498	MCLK1A	9	0560	RESCO	8	0622	5161A	14	0684	XREQØA	2
0003	AIRØ21	12	0065	CLK1E	9	0127	DL221	16	0189	EDØ31	15	0251			0313	FLADRØ	2	0375	IO291	13	0437	MDSØ4Ø	17	0499	MSTOPØ	9	0561	RDFWO	6	0623	5171A	14	0685	ZIRØ	10
0004	AIRØ31	12	0066	CLK1F	9	0128	DL231	16	0190	EDØ41	16	0252	FCPØ	10	0314	FDUAØ	4	0376	IO3Ø1	13	0438	MDSØ5Ø	17	0500	MSTOPØA	9	0562	RRØ	6	0624	5181A	14	0686	YDØ81	3
0005	AIRØ41	12	0067	CLKØ	9	0129	DL241	16	0191	EDØ51	16	0253	FCP1	10	0315	FDUA1	4	0377			0439	MDSØ6Ø	17	0501	MRESTPØ	9	0563	RSTOPØA	9	0625	5191A	14	0687	YDØ91	3
0006	AIRØ51	12	0068	CLKØA	9	0130	DL251	16	0192	EDØ61	16	0254	FDUSKT1	4	0316	FEFWØ	5	0378	ILDMAØ	7	0440	MDSØ7Ø	17	0502	MFAULTØ	9	0564	RX2STPØ	10	0626	52Ø1A	14	0688	YD101	3
0007	AIRØ61	12	0069	CLKØB	9	0131	DL261	16	0193	EDØ71	16	0255	FENCE1	7	0317	FEFW1	5	0379	ILOCØ		0441	MDSØ8Ø	17	0503	MSBC1	4	0565	RX3STPØ	10	0627	5211A	14	0689	YD111	3
0008	AIRØ71	12	0070	CACLK1	10	0132	DL271	16	0194	EDØB1	16	0256			0318	FBØ	9	0380	IRXKØ	10	0442	MDSØ9Ø	17	0504	MSBCØ	4	0566	RSTOPØ	9	0628	5221A	14	0690	YDØB1A	3
0009	AIRØB1	12	0071	CASTOPØ	10	0133	DL281	16	0195	EDØ91	16	0257	ST1	5	0319	FSCLK1	9	0381			0443	MDS1ØØ	17	0505	MATSTOPØ	4	0567	RX4STPØ	11	0629	5231A	14	0691	YDØ91A	3
0010	AIRØ91	12	0072	CAPI1	10	0134	DL291	16	0196	EDIØ1	16	0258	FTITI		0320	FSCLKØ	9	0382	IOSTOPØ	13	0444	MDS11Ø	17	0506	MDSBØ	7	0568	RR1	11	0630	5241A	14	0692	YD1Ø1A	3
0011	AIR1Ø1	12	0073	CAPZ1	10	0135	DL3Ø1	16	0197	EDI11	16	0259	FWI	6	0321	FOIRØ	6	0383	IWARØ	12	0445	MDS12Ø	17	0507	MDWSA1	7	0569	RI2O	11	0631	5251A	14	0693	YD111A	3
0012	AIR111	12	0074	CAMAØ	10	0136	DMAØØØ	15	0198	EDI21	16	0260	FERD	9	0322	GBRANCHØ	9	0384	I4O	12	0446	MDS13Ø	17	0508	MDLSA1	7	0570	RX21	11	0632	526IA	14	0694	YSØ1	3
0013	ALIRCKØ	10	0075	CAR26I	16	0137	DMAØ1Ø	15	0199	EDI31	16	0261	FSIRI	9	0323	GDIRØ	10	0385	LMAØBØ	15	0447	MDS14Ø	17	0509	MREAD1	6	0571	RX31	11	0633	5271A	14	0695	YS11	3
0014	ALIQØ	10	0076	CCLRO	2	0138	DMAØ2Ø	15	0200	EDI41	16	0262	FPD1	6	0324	GEOTI	8	0386	LMA9Ø	15	0448	MDS15Ø	17	0510	MDHCLKØ	7	0572	RI2RX31	11	0634	528IA	14	0696	YS21	3
0015	ALIR1	10	0077	CLADAØ	7	0139	DMAØ3Ø	15	0201	EDI51	16	0263	FPE1	6	0325	GGDIRØ	10	0387	LMA1ØØ	15	0449	MDS16Ø	18	0511	MDLCLKØ	7	0573	RFAULTØA	12	0635	529IA	14	0697	YS31	3
0016	ALIRØ	10	0078	CLSØ	7	0140	DMAØ4Ø	16	0202	EEDCLKØ	7	0264	FPF1	6	0326	GGDIR1	10	0388	LMA11Ø	15	0450	MDS17Ø	18	0512	MDRBØ	11	0574	RDØØ1	6	0636	53ØIA	14	0698	YS121	3
0017	AIBIØ	9	0079			0141	DMAØ5Ø	16	0203	EMDENBØ	8	0265	FPC1	6	0327	GMATSTOPØ	4	0389	LMA12Ø	15	0451	MDS18Ø	18	0513	OEDCLKØ	7	0575	RDØØØD	6	0637	531IA	14	0699	YS131	3
0018	AIBIIA	9	0080	CLRLYO	7	0142	DMAØ6Ø	16	0204	ENXCVRØ	8	0266	FPFØ	6	0328	GRDØ	6	0390	LMA13Ø	15	0452	MDS19Ø	18	0514	OMDENBØ	8	0576	RDØ11	4	0638	5B291	13	0700	YS141	3
0019	AIBI1	9	0081	CLSTØ	2	0143	DMAØ7Ø	16	0205	EMDRØØ1	17	0267	FPG1	6	0329	GRDI	6	0391	LMA14Ø	15	0453	MDS2ØØ	18	0515	OSCØ	9	0577	RDØ21	4	0639	58Ø	13	0701	YS151	3
0020	ACLRØ	2	0082	CMRZØ	10	0144	DMAØBØ	16	0206	EMDR011	17	0268	FPG6	6	0330	GSIRØ	6	0392	LMA15Ø	15	0454	MDS21Ø	18	0516	OPSTOPØ	9	0578	RDØ1ØD	4	0640	SDFF1	13	0702	YDCLKØ	3
0021	AMDRØØ1	3	0083	CNTEØØ	11	0145	DMAØ9Ø	16	0207	EMDR021	17	0269	FBIRI	2	0331	GDATØ	13	0393	LMA16Ø	15	0455	MDS22Ø	18	0517	NOCNTØ	11	0579	RDØ11D	4	0641	SYNØ	13	0703	YSCLKØ	3
0022	AMDRØ11	3	0084	STPIR1	10	0146	DMA1ØØ	16	0208	EMDR031	17	0270	FBIRØ	7	0332	HALTØ	2	0394	LMA17Ø	15	0456	MDS23Ø	18	0518	NCEØ	10	0580	RDØ2ØD	4	0642	SMBSYØ	4	0704	YDTIØ	12
0023	AMDRCKØ	7	0085	COMMØ	12	0147	DMA11Ø	16	0209	EMDR041	17	0271	FOIR1	6	0333	HALT1	2	0395	LMA18Ø	15	0457	MDS24Ø	18	0519	PA3Ø1	4	0581	RDØ21D	4	0643	SMBSY1	4	0705	YDMIØ	12
0024	ANS1	8	0086	COMSTPØ	13	0148	DMA12Ø	16	0210	EMDR051	17	0272	FRD1	6	0334	HOST1	8	0396	LMA19Ø	15	0458	MDS25Ø	18	0520	PA3ØØD	4	0582	RDØ31D	12	0644	SCLRØB	2	0706	14KØ6	2
0025	ANSØ	8	0087	CRY181	15	0149	DMA13Ø	16	0211	EMDR061	17	0273	ØABØ2	6	0335	IRØØØ	11	0397	LMA2ØØ	15	0459	MDS26Ø	18	0521	PA3Ø1	4	0583	RDØ31	12	0645	SCLR1	2	0707	Ø7E12	2
0026	AFINRØ	10	0088	CYDØ	12	0150	DMA14Ø	16	0212	EMDR071	17	0274			0336	IRØ1Ø	11	0398	LMA21Ø	15	0460	MDS27Ø	18	0522	PSBCØ	4	0584	RDØ41	9	0646	SCLK1A	9	0708	Ø78ØB	2
0027	AFINR1	10	0089	CWRØ	6	0151	DMA15Ø	16	0213	EMDRØB1	17	0275	FMREQ1	2	0337	IRØ2Ø	11	0399	LMA22Ø	15	0461	MDS28Ø	18	0523	PSPC1	4	0585	RDØ51	9	0647	SCLK1	9	0709	ØGB03	2
0028	AMSTOPØ	9	0090	CMDØ	13	0152	DMXØBØ	15	0214	EMDR091	17	0276	Ø9DØG	2	0338	IRØ3Ø	11	0400	LMA23Ø	15	0462	MDS29Ø	18	0524	PDUAØ	4	0586	RD121	12	0648	SCAP11	10	0710	ØGEØ2	2
0029	ADVØ	9	0091	CAIRØ	12	0153	DMXØ9Ø	15	0215	EMDR101	17	0277	FLMREQØ	2	0339	IRØ4Ø	11	0401	LMA24Ø	15	0463	MDS3ØØ	18	0525	PDUA1	4	0587	RD131	12	0649	SERØ	4	0711	ØGE15	2
0030	ASEL1	14	0092	CLFLRØ	13	0154	DMX1ØØ	15	0216	EMDR111	17	0278	FDEOT1	2	0340	IRØ5Ø	11	0402	LMA25Ø	15	0464	MDS31Ø	18	0526	PMEM1	4	0588	RD141	12	0650	SOTØ	6	0712	ØGCØ2	2
0031	ADESØ	13	0093	DØØØ	13	0155	DMX11Ø	15	0217	EMDR121	17	0279	FLDARA1	2	0341	IRØ6Ø	11	0403	LMA26Ø	15	0465	MDSØØ1	17	0527	PROSC1	6	0589	RD15Ø	12	0651	SOTØA	6	0713	ØGCØ7	2
0032	B1G1	14	0094	DØ1Ø	13	0156	DMX12Ø	15	0218	EMDR131	17	0280	FLDARAØ	2	0342	IRØ7Ø	11	0404	LMA27Ø	15	0466	MDSØ11	17	0528	PSELIA	2	0590	RD161	14	0652	SOT1A	6	0714	ØGC1Ø	2
0033	B171	14	0095	DØ2Ø	13	0157	DMX13Ø	15	0219	EMDR141	17	0281	FEIRØ	6	0343	IRDØØ1	12	0405	LMA28Ø	15	0467	MDSØ21	17	0529	PSZ	4	0591	RD240	14	0653	STDØ	14	0715	ØGBØ8	2
0034	B181	14	0096	DØ3Ø	13	0158	DMX14Ø	15	0220	EMDR151	17	0282	FLDARBØ	2	0344	IRDØ11	12	0406	LMA29Ø	15	0468	MDSØ31	17	0530	PSW181	10	0592	RD251	14	0654	STB1	14	0716	ØGB11	2
0035	B191	14	0097	DØ4Ø	13	0159	DMX15Ø	15	0221	EMDR161	18	0283	FAULTØ	12	0345	IRDØ21	12	0407	LMA3ØØ	15	0469	MDSØ41	17	0531	PSW271	13	0593	RD261	14	0655	SAFINR1	10	0717	Ø5BØG	2
0036	B2Ø1	14	0098	DØ5Ø	13	0160	DMASELØ	2	0222	EMDR171	18	0284	FPTFØ	13	0346	IRDØ31	12	0408	LMA31Ø	15	0470	MDSØ51	17	0532	PSW261	13	0594	RD271	14	0656	SGDIRØ	10	0718	ØBCØB	2
0037	B211	14	0099	DØGØ	13	0161	DMASEL1	2	0223	EMDR181	18	0285	FCOMMØ	13	0347	IRDØ41	12	0409	LOADØ	8	0471	MDSØ61	17	0533	QUEØ	6	0595	RD281	12	0657	SRXX1	11	0719	Ø5BØB	2
0038	B221	14	0100	DØ7Ø	13	0162	DMASMI	2	0224	EMDR191	18	0286	FCOUTØ	13	0348	IRDØ51	12	0410	LOAD1	8	0472	MDSØ71	17	0534	RDATØB1	15	0596	RD291	12	0658	SBØ	13	0720	ØGFØ7	3
0039	B231	14	0101	DØ8Ø	13	0163	DMALMI	2	0225	EMDE2Ø1	18	0287	FDATØ	13	0349	IRDØG1	12	0411	LERØ	4	0473	MDSØ81	17	0535	RDATØ11	15	0597	RD3Ø1	12	0659	TPCØ	6	0721	ØGFØ4	3
0040	B241	14	0102	DØ9Ø	13	0164	DMBZYI	2	0226	EMDR211	18	0288	FSYNØ	13	0350	IRDØ71	12	0412	LMBSYOA	4	0474	MDSØ91	17	0536	RDATØ21	15	0598	RD311	12	0660	TRAPØ	9	0722	Ø4FØ4	3
0041	B251	14	0103	DIØØ	13	0165	DSTOP1	9	0227	EMDR221	18	0289	FSYN1	13	0351	IRDØB1	3	0413	LMBSYØ	4	0475	MDS1Ø1	17	0537	RDATØ31	15	0599	RD28ØA	12	0661	TACKØØØ	13	0723	Ø4FØ7	3
0042	B261	14	0104	DI1Ø	13	0166	DSTOPØ	9	0228	EMDR231	18	0290	ENCEØ	10	0352	IRDØ91	3	0414	LMBSY1	4	0476	MDS111	17	0538	RDATØ41	16	0600	RD281A	12	0662	TACKØ1Ø	13	0724	Ø4FØ9	3
0043	B271	14	0105	DI2Ø	13	0167	DSTOPØA	9	0229	EMDR241	18	0291	FINRØ	10	0353	IRD1Ø1	3	0415	LMRQØ	2	0477	MDS121	17	0539	RDATØ51	16	0601	RD291	12	0663	TACKØ2Ø	13	0725	Ø4F12	3
0044	B281	14	0106	DI3Ø	13	0168	DOITØ	10	0230	EMDR251	18	0292	FINR1	10	0354	IRD111	3	0416	LYDIØ	12	0478	MDS131	17	0540	RDATØG1	16	0602	RD3Ø1A	12	0664	TACKØ3Ø	13	0726	11K13	3
0045	B291	14	0107	DI4Ø	13	0169	DCLKØ	9	0231			0293	FCIN1	13	0355	IRD121	3	0417	LYSIØ	12	0479	MDS141	17	0541	RDATØ71	16	0603	RD311A	12	0665	TPC	6	0727	1ØFØ4	3
0046	B3Ø1	14	0108	DI5Ø	13	0170	DANTI	6	0232			0294	FDAAØ	5	0356	IRD131	3	0418	LIR1	10	0480	MDS151	17	0542	RDATØB1	16	0604	RFAULTØ	12	0666	TPE	6	0728	11H11	3
0047	B311	14	0109	DAØ	13	0171	DMEMØ	4	0233	EMDR261	18	0295	FDAØ	5	0357	IRD141	3	0419	LINC1	10	0481	MDS161	18	0543	RDATØ91	16	0605	RMSR1	7	0667	TPF	6	0729	Ø9FØ4	3
0048	BRWRTØ	8	0110	DRØ	13	0172	DMAWRTØ	7	0234	EMDR271	18	0296	FDA1	5	0358	IRD151	3	0420	LEN2B1	11	0482	MDS171	18	0544	RDATIØ1	16	0606	S161	14	0668	TPH	6	0730	Ø9F01	3
0049	BRWRT1	5	0111	DISAØ	10	0173	DCLR1	2	0235	EMDR281	18	0297	FDB1	5	0359	INHFSØ	13	0421	LEN291	11	0483	MDS181	18	0545	RDATI11	16	0607	S171	14	0669	ULIØØ	14	0731	Ø9F13	3
0050	BRTRDØ	5	0112	DISBØ	10	0174	DDUAØ	4	0236	EMDR291	18	0298	FDC1	5	0360	IOOP1	13	0422	LEN3Ø1	11	0484	MDS191	18	0546	RDATI21	16	0608	S181	14	0670	ULIS1Ø	14	0732	Ø9F1Ø	3
0051	BRTRD1	5	0113	DLØB1	15	0175	DDUA1	4	0237	EMDE3Ø1	18	0299	FDCØ	5	0361			0423	LPSTDØ	12	0485	MDS2Ø1	18	0547	RDATI31	16	0609	S191	14	0671	UMDR1	14	0733	14EØ4	3
0052	BCLRØ	2	0114	DLØ91	15	0176	DUAØ	4	0238	EMDR311	18	0300	FBRTRDØ	5	0362	IO161	13	0424	LSSTDØ	12	0486	MDS211	18	0548	RDATI41	16	0610	S2Ø1	14	0672	WRTØ	7	0734	Ø3HØB	3
0053	BCNTØ	13	0115	DLI81	15	0177	DUA1	6	0239			0301	FBRTRD1	5	0363	IO171	13	0425	LDNALØ	7	0487	MDS221	18	0549	RDATI51	16	0611	S211	14	0673	SXRP	5	0735	Ø3HØ6	3
0054	SMSTOPØ	9	0116	DLI11	15	0178	DOSCØ	5	0240			0302	FDRDYØ	5	0364	IO181	13	0426	LHWRTØ	7	0488	MDS231	18	0550	PDAXØB1	15	0612	S221	14	0674	16XRP	14	0736	ØBF1Ø	3
0055	BRANCHØ	9	0117	DLI21	15	0179	DMAHWØ	5	0241			0303	FDRDY1	5	0365	IO191	13	0427	LWRTØ	7	0489	MDS241	18	0551	PDAXØ91	15	0613	S231	14	0675	XRPØ5	5	0737	ØBF13	3
0056	BRSTØ	5	0118	DLI31	15	0180	DMARSØ	5	0242			0304	FDA1A	5	0366	IO2Ø1	13	0428	LMDR1	12	0490	MDS251	18	0552	PDAX1Ø1	15	0614	S241	14	0676	XRPØBK	6	0738	ØBF01	3
0057	BRST1	5	0119	DLI41	15	0181	DMA16Ø	5	0243			0305	FBRWRTØ	5	0367	IO211	13	0429	LDCTRD	12	0491	MDS261	18	0553	PDAX111	15	0615	S251	14	0677	XRPØBM	16	0739	ØBFØ4	3
0058	BLIR1	10	0120	DLI51	15	0182	DMA17Ø	5	0244			0306	FERDØ	5	0368	IO221	13	0430	LFLRØ	12	0492	MDS271	18	0554	PDAX121	15	0616	S261	14	0678	XRPSB	2	0740	1ØFØ6	3
0059	BLIRØ	10	0121	DLI61	15	0183	DMS1	8	0245	EXMATI	6	0307	EECDI	5	0369	IO231	13	0431	LTRCKI	10	0493	MDS281	18	0555			0617			0679			0741		
0060	CLK1	9	0122	DLI71	15	0184	DISEXTP	11	0246			0308	FSOTØ	2	0370	IO241	13	0432	LDIØØ	12	0494	MDS291	18	0556	PDAX141	15	0618	S281	14	0680	X2O	3	0742	12M12	4
0061	CLK1A	9	0123	DLI81	15	0185	DRFALTØ	12	0247	EXOSC	9	0309	FSOT1	5	0371	IO251	13	0433	MDSØØØ	17	0495	MDS3Ø1	18	0557	PDAX151	15	0619	S291	14	0681	X21	10	0743	12MC3	4
0062	CLK1E	9	0124	DLI91	16	0186	EDØØ1	15	0248	EDAT1	6	0310	FQEOT1	2	0372	IO261	13	0434	MDSØ1Ø	17	0496	MDS311	18	0558	RCLKØ	9	0620	S3Ø1	14	0682	XXRP	10	0744	12M11	4

NOTES

REVISIONS

NET B4 WAS CMTEØ1, SHT 11.					
KR	Ø11	4908	M	12-15-81	R01 X

UNLESS OTHERWISE SPECIFIED

SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
V. PERRI	BLUSK	DES/DFT	6-10-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-D
EDMA MDR 0/15

TASK 03976	SHT
DWG 35-770 R01 D08	19 - 20

CROSS REFERENCE NET#, MNEMONIC, SHEET#

NETS	MNEMONIC	SH	NETS	MNEMONIC	SH	NETS	MNEMONIC	SH	NETS	MNEMONIC	SH	NETS	MNEMONIC	SH	NETS	MNEMONIC	SH	NETS	MNEMONIC	SH	NETS	MNEMONIC	SH	NETS	MNEMONIC	SH	NETS	MNEMONIC	SH	NETS	MNEMONIC	SH
0745	17E08	4	0807	04D09	6	0869	13E08	9	0931	16M08	13	0993	05J09	18	1055	GND	18	1117			1179			1241			1303			1365			1427		
0746	21J06	4	0808	04D05	6	0870	16B15	9	0932	16M06	13	0994	05J12	18	1056		18	1118			1180			1242			1304			1366			1428		
0747	09E10	4	0809	05A03	6	0871	13C06	9	0933	16M03	13	0995	04K04	18	1057		18	1119			1181			1243			1305			1367			1429		
0748	17E11	4	0810	04D04	6	0872	19C03	10	0934	16M11	13	0996	04K07	18	1058		18	1120			1182			1244			1306			1368			1430		
0749	20H08	4	0811	05A08	6	0873	19C06	10	0935	13K06	13	0997	04K09	18	1059		4	1121			1183			1245			1307			1369			1431		
0750	22K10	4	0812	05A11	6	0874	16E08	10	0936	15J05	13	0998	04K12	18	1060		13	1122			1184			1246			1308			1370			1432		
0751	20H06	4	0813	01D06	6	0875	20C11	10	0937	15J02	13	0999	04J04	18	1061		13	1123			1185			1247			1309			1371			1433		
0752	22K13	4	0814	03B09	6	0876	17C08	10	0938	18H12	13	1000	04J07	18	1062		13	1124			1186			1248			1310			1372			1434		
0753	09C08	4	0815	03A11	6	0877	17B06	10	0939	16H06	13	1001	04J09	18	1063		13	1125			1187			1249			1311			1373			1435		
0754	08A04	4	0816	02A77	6	0878			0940	18J11	13	1002	04J12	18	1064		13	1126			1188			1250			1312			1374			1436		
0755	09D03	4	0817	03A08	6	0879	20C06	10	0941	18H06	13	1003	04J01	18	1065		13	1127			1189			1251			1313			1375			1437		
0756	09D09	4	0818	03A10	6	0880	17D06	10	0942	17H04	13	1004			1066		2	1128			1190			1252			1314			1376			1438		
0757	09D10	4	0819	04H03	6	0881	17B03	10	0943	17K06	13	1005			1067		2	1129			1191			1253			1315			1377			1439		
0758	08A14	4	0820	04H12	6	0882	16E03	10	0944	16K13	13	1006			1068		2	1130			1192			1254			1316			1378			1440		
0759	08A15	4	0821	11C15	6	0883	22H06	10	0945	16H12	13	1007			1069		7	1131			1193			1255			1317			1379			1441		
0760	08A10	4	0822	03A06	6	0884	22R04	10	0946	15J09	13	1008			1070		3	1132			1194			1256			1318			1380			1442		
0761	02N09	5	0823	04B03	6	0885	19E12	10	0947	17K11	13	1009			1071		3	1133			1195			1257			1319			1381			1443		
0762	01A08	5	0824	03A03	6	0886	19D11	10	0943	17K03	13	1010	09C06	7	1072		3	1134			1196			1258			1320			1382			1444		
0763	00B02	5	0825	04A05	6	0887	19C08	10	0949	17J05	13	1011	11F06	12	1073		3	1135			1197			1259			1321			1383			1445		
0764	00B03	5	0826	03A05	6	0888	19D08	10	0950	16K15	13	1012	13K12	10	1074		3	1136			1198			1260			1322			1384			1446		
0765	00B12	5	0827	12B11	7	0889	10K02	11	0951	16K14	13	1013	13A05	9	1075		3	1137			1199			1261			1323			1385			1447		
0766	01B13	5	0828	11B12	7	0890	10K05	11	0952	15H06	13	1014	13A01	9	1076		4	1138			1200			1262			1324			1386			1448		
0767	00H17	5	0829	11B04	7	0891	10K06	11	0953	18H03	13	1015	11A12	7	1077	GND	4	1139			1201			1263			1325			1387			1449		
0768	00B11	5	0830			0892	10K09	11	0954	16J06	13	1016	15F08	12	1078			1140			1202			1264			1326			1388			1450		
0769	00D06	5	0831	11B06	7	0893	10K12	11	0955	14R04	13	1017	15K10	13	1079	GND	5	1141			1203			1265			1327			1389			1451		
0770	02D08	5	0832	11A06	7	0894	10K15	11	0956	14R02	13	1018	12K11	13	1080	GND	5	1142			1204			1266			1328			1390			1452		
0771	01D11	5	0833	12B08	7	0895	10K16	11	0957	18M06	13	1019	GND	6	1081	GND	5	1143			1205			1267			1329			1391			1453		
0772	01E06	5	0834	12A06	7	0896	10K19	11	0958			1020		7	1082	EFWRT1		1144			1206			1268			1330			1392			1454		
0773	02D03	5	0835	11B08	7	0897	09E04	11	0959			1021		8	1083	ERD1		1145			1207			1269			1331			1393			1455		
0774	00H06	5	0836	05B03	7	0898	09H06	11	0960	16J09	13	1022		8	1084	EOT1		1146			1208			1270			1332			1394			1456		
0775	00D12	5	0837	10B02	7	0899	10J09	11	0961	19A19	14	1023	GND	8	1085			1147			1209			1271			1333			1395			1457		
0776	00D08	5	0838	07A06	8	0900	12H08	11	0962	11K10	14	1024		8	1086			1148			1210			1272			1334			1396			1458		
0777	01A04	5	0839	07A11	8	0901	07E06	11	0963	13K08	14	1025		9	1087	GENMAA1		1149			1211			1273			1335			1397			1459		
0778	01C06	5	0840	07A03	8	0902	12H12	11	0964	14J09	14	1026		9	1088			1150			1212			1274			1336			1398			1460		
0779	01C05	5	0841	07A08	8	0903	20A02	11	0965	14J12	14	1027	GND	11	1089	EOT0		1151			1213			1275			1337			1399			1461		
0780	01D08	5	0842	02B02	8	0904	20A04	11	0966	19H03	14	1028		11	1090	ENMAA0		1152			1214			1276			1338			1400			1462		
0781	00E06	5	0843	06A14	8	0905	20A06	11	0967	09J15	15	1029		11	1091	ENAOSC0		1153			1215			1277			1339			1401			1463		
0782	01A02	5	0844	02C05	8	0906	20A08	11	0968	09K15	15	1030		11	1092	FERI		1154			1216			1278			1340			1402			1464		
0783	03D06	5	0845	08B08	8	0907	20A10	11	0969	08M10	16	1031		11	1093	14H11		1155			1217			1279			1341			1403			1465		
0784	01D03	5	0846	10F10	8	0908	20A12	11	0970	07K04	17	1032		12	1094	EFLDEN0		1156			1218			1280			1342			1404			1466		
0785	03C06	5	0847	10F08	8	0909	22A09	11	0971	07K07	17	1033		12	1095	21H03		1157			1219			1281			1343			1405			1467		
0786	03D08	5	0848	09H08	8	0910	22A09	11	0972	07K09	17	1034		12	1096	FPC0		1158			1220			1282			1344			1406			1468		
0787	02D06	5	0849	10F11	8	0911	20B08	11	0973	07K12	17	1035		12	1097	09B08		1159			1221			1283			1345			1407			1469		
0788	03D03	5	0850	10E04	8	0912	20B12	11	0974	07J04	17	1036		13	1098	12B06		1160			1222			1284			1346			1408			1470		
0789	02M03	5	0851	04E08	8	0913	21B14	11	0975	07J07	17	1037		14	1099	CLSTA0		1161			1223			1285			1347			1409			1471		
0790	02M06	5	0852	13A06	9	0914	21B13	11	0976	07J09	17	1038		14	1100	10D06		1162			1224			1286			1348			1410			1472		
0791	02D11	5	0853	15B12	9	0915	21B10	11	0977	07J12	17	1039		14	1101	FERD0A		1163			1225			1287			1349			1411			1473		
0792	03H12	5	0854	15B09	9	0916	21A14	11	0978	06K04	17	1040		14	1102			1164			1226			1288			1350			1412			1474		
0793	02H08	5	0855	17A11	9	0917	21A13	11	0979	06K07	17	1041		14	1103			1165			1227			1289			1351			1413			1475		
0794	02H09	5	0856	13C09	9	0918	21A12	11	0980	06K09	17	1042		14	1104			1166			1228			1290			1352			1414			1476		
0795	00C07	5	0857	13C10	9	0919	21A11	11	0981	06K12	17	1043		17	1105			1167			1229			1291			1353			1415			1477		
0796	11D06	6	0858	15F03	9	0920	13H08	12	0982	06J04	17	1044		17	1106			1168			1230			1292			1354			1416			1478		
0797	11D08	6	0859	13C05	9	0921	14F11	12	0983	06J07	17	1045		17	1107			1169			1231			1293			1355			1417			1479		
0798	11E12	6	0860	17A12	9	0922	11M13	12	0984	06J09	17	1046		17	1108			1170			1232			1294			1356			1418			1480		
0799	11D12	6	0861	14A09	9	0923	11M12	12	0985	06J12	17	1047		17	1109			1171			1233			1295			1357			1419			1481		
0800	10B12	6	0862	14A10	9	0924	11M11	12	0986	02B08	17	1048		17	1110			1172			1234			1296			1358			1420			1482		
0801	10C03	6	0863	13B12	9	0925	14R06	12	0987	04M0C	18	1049		17	1111			1173			1235			1297			1359			1421			1483		
0802	10B10	6	0864	15C01	9	0926	11F05	12	0988	04M07	18	1050		17	1112	GND	5	1174			1236			1298			1360			1422			1484		
0803	09B03	6	0865	15A06	9	0927	13F12	12	0989	04M09	18	1051		18	1113	GND	6	1175			1237			1299			1361			1423			1485		
0804	09B06	6	0866	12C08	9	0928	12M06	12	0990	04M17	18	1052		18	1114	GND	6	1176			1238			1300			1362			1424			1486		
0805	03B08	6	0867	16B05	9	0929	21K11	13	0991	05J04	18	1053		18	1115	VAJ06	11	1177			1239			1301			1363			1425			1487		
0806	04D08	6	0868	12D05	9	0930	21K12	13	0992	05J07	18	1054		18	1116	FPPFLT0	10	1178			1240			1302			1364			1426			1488		

NOTES

REVISIONS

ADDED MNEMONICS FOR NEW NETS 1112 THRU 1114.					
JLV	JV	4650	MS	4-21-81	R01
ADDED MNEMONICS FOR NEW NET 1115.					
JLV	JV	4772	M	10-1-81	R02
ADDED NET 1116.					
KR	JV	4908	M	12-13-81	R03 X

UNLESS OTHERWISE SPECIFIED

SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
V. PERRI	BLUSK	DES/DFT	6-10-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
CPU-D
EDMA MDR 0/15

TASK	SHT
03976	
DWG 35-770 R03 D08	20 - 20

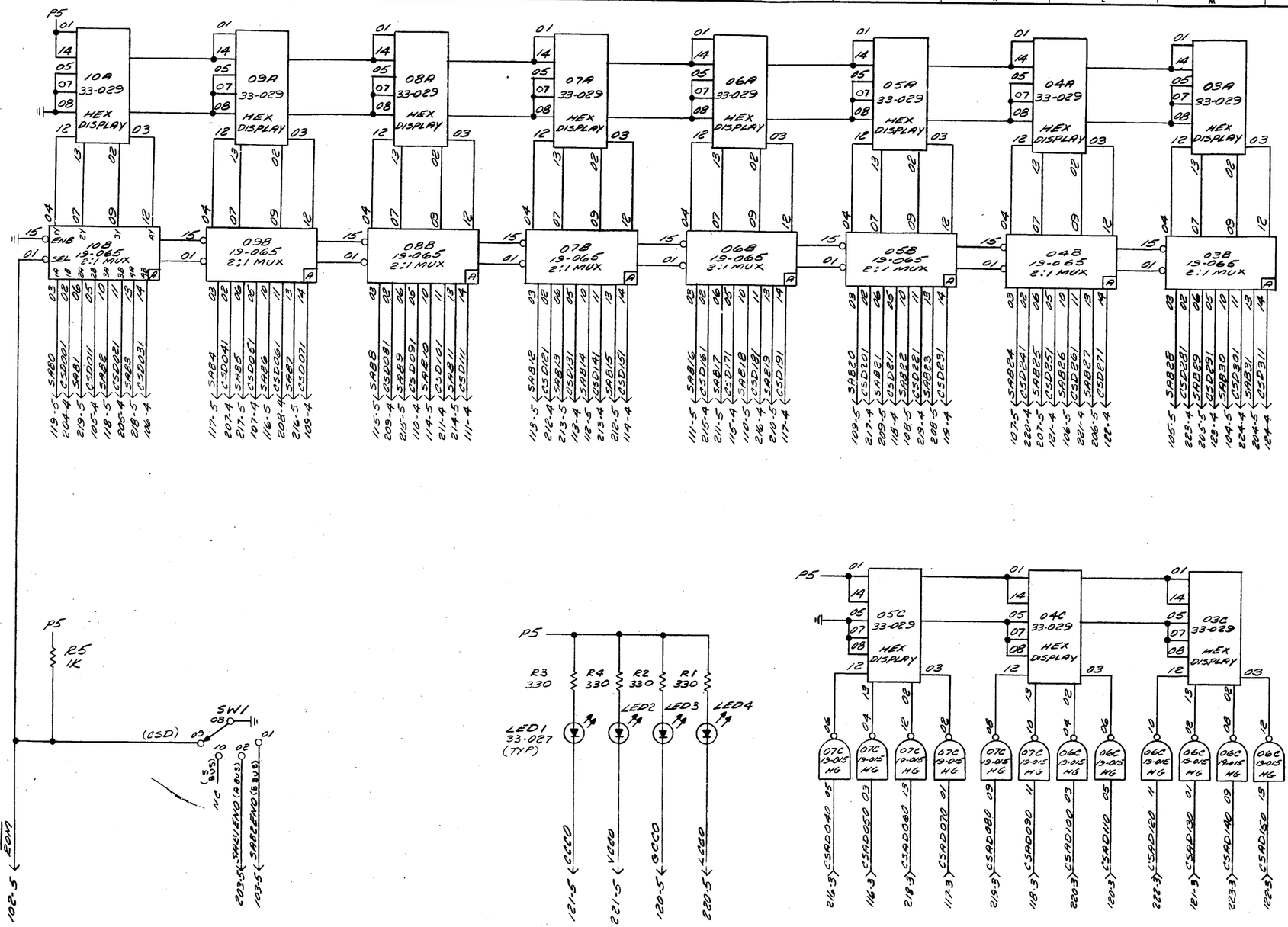
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS			
PRODUCTION APPROVAL		INIT	DATE
	DES		12.13.75
	PROD		

AREA F,G-7
LED4 WAS TO 'CCCO'
LED3 WAS TO 'VCCO'
LED1 WAS TO 'GCCO'
LED2 WAS TO 'LCCO'
PINOS OF 03A-10A WAS N.C.

WM	3071 -01		3-2-76	R01

RELEASED FOR PRODUCTION
ENG. [signature] DATE 4-9-76



BOARD AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL	
BOARD	REV
36-612	R01

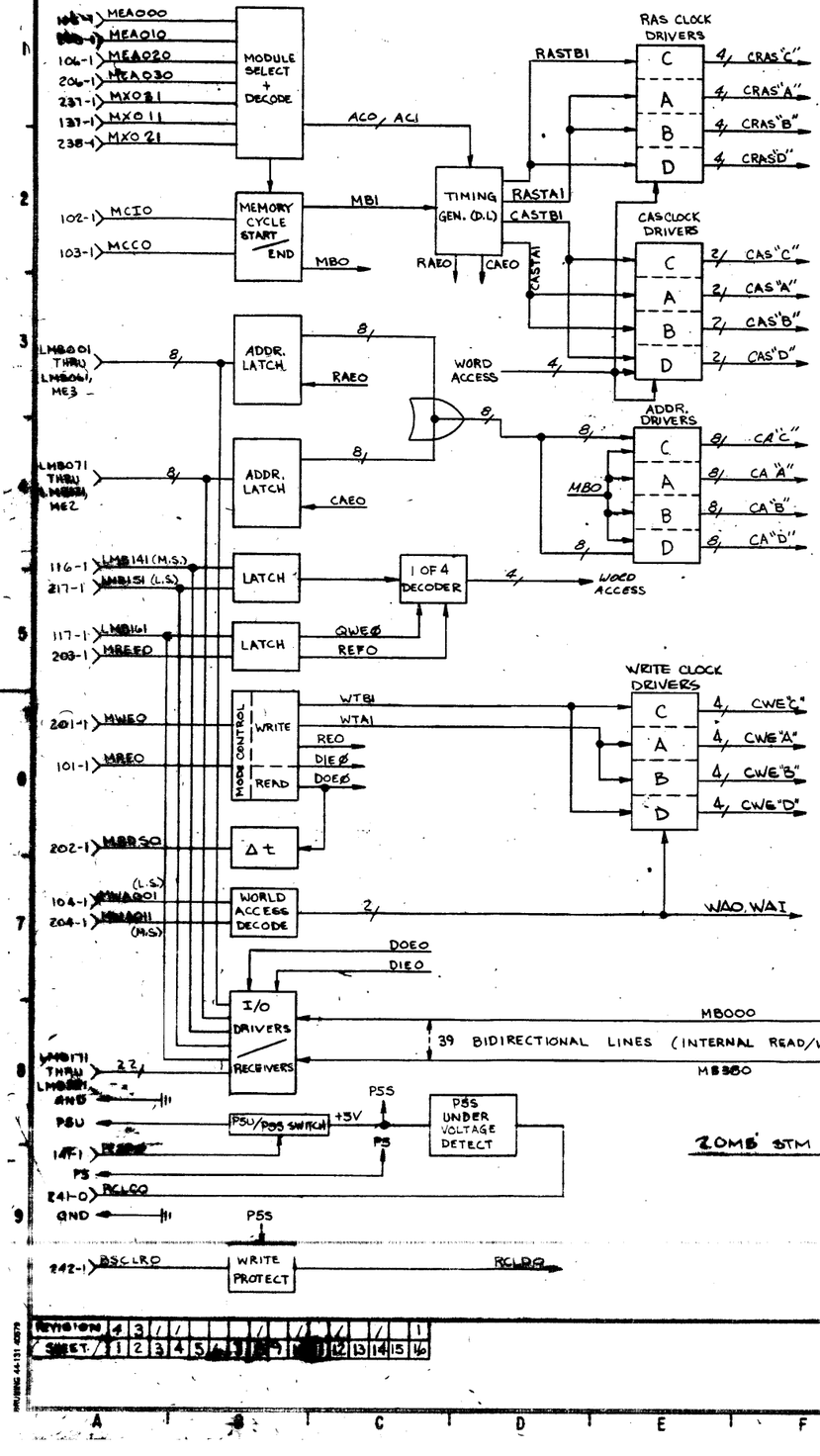
SCALE-	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	P.EDWARDS	DRAFT	3-30-76
	E.OLERO	CHK	3-30-76
	T.FYFE	ENGR	3-30-76
	J.JAMES	SYS TST	3-30-76
	V.PISARCIK	MGR	3-30-76

TITLE FUNCTIONAL SCHEMATIC 8/32 TEST DISPLAY

TASK NO. 03071 DWG NO. 36-612 R01 DUP

SHEET OF 1—1

BRUNING 44-231 24538



20MB STM BLOCK DIAGRAM

TEST POINT		
E4	PSU	SHT 16
E5	PSS	SHT 16

STRAPPING INFORMATION					
STAKE	MNEMONIC	SHT	STAKE	MNEMONIC	SHT
E	—	2	B	—	2
E1	—	2	B1	CCO	2
E2	—	2	B2	GND	2
E3	—	2	C	—	2
			C1	BREFO	2

BACK PANEL MAP		TERM. NO.	CONN.
ROW 1	ROW 2		
GND	GND	43	
	BSCLRO	42	
PPSDO	RCLCO	41	
		40	
		39	
	MX021	38	
MX011	MX031	37	
LMB381	LMB371	36	
LMB361	LMB351	35	
GND	GND	34	
GND	GND	33	
LMB341	LMB331	32	
LMB321	LMB311	31	
LMB301	LMB291	30	
LMB281	LMB271	29	
LMB261	LMB251	28	
LMB241	LMB231	27	
LMB221	LMB211	26	
LMB201	LMB191	25	
GND	GND	24	
		23	
		22	
		21	
		20	
GND	GND	19	
LMB181	LMB171	18	
LMB161	LMB151	17	
LMB141	LMB131	16	
LMB121	LMB111	15	
LMB101	LMB091	14	
LMB081	LMB071	13	
LMB061	LMB051	12	
LMB041	LMB031	11	
GND	GND	10	
GND	GND	09	
LMB021	LMB011	08	
LMB001		07	
MEA020	MEA030	06	
MEA000	MEA010	05	
MWA001	MWA011	04	
MCCO	MREFO	03	
MCIO	MRDSØ	02	
MREO	MWEO	01	
GND	GND	00	

REVISIONS			
PRE PRODUCTION APPROVAL	INIT	DEV	DATE 12/9/81

SEE SHEET 16 FOR REVISION
AREA A9, UPDATED REVISION RECORD
AREA A9, FO1 & FO2 WERE R00

GPS		4499	M	10-8-80	R01

REVISED SHTS 2,3. AREA L,M-3&4: DELETED STRAPPING TABLES 2&3.

JAT		4707	E	6-9-81	R02

ADDED A25 & A37 TO TABLE OF SPARES. AREA A9: REVISED REV LEVEL OF PARTS LIST. REVISED SHTS 2,4,8,10,12 & 16.

JAT		4733	M3	6-10-81	R03

RELEASED FOR PRODUCTION
ENG. _____ DATE 12/9/81

REVISED SHTS 1&2.

KR		4900	E	12-3-81	R04

A37					
A35					
A46	19-240	01	35-764 F01		R04
A48	19-136	01	35-764 F02		R04
A46	19-088	12	35-764 F03		R02
REF.	PC NO.	SPARE OUTPUT	35-764 F04		R02

USED IN MANUAL 47-004
PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

PT. NO.	VARIATION
F01	AS SHOWN, SHTS 1-16, FOR VARIATIONS SEE SHTS, 2, 3, 8, 10 THRU 15
F02	AS SHOWN, SHTS 1-16, 2, 3, 8, 10 THRU 15
F03	AS SHOWN, SHTS 1-16, FOR VARIATIONS SEE SHTS, 2, 3, 8 THRU 15
F04	AS SHOWN, SHTS 1-16

UNLESS OTHERWISE SPECIFIED

SCALE: NONE	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
G. SHINN	S. TRIMARCHI	DES / DFT	11-9-79
R. CERO		SUPV	10-16-81
E. GREENSTEIN		TEST	10-16-81
P. OBRDA		ENG	10-16-81
L. PEZZI / D. FRANK		MGR	10-16-81
R. A. BARKER		QC	10-16-81

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
STM 2.0MB

TASK 03979	SHT
DWG 35-764 R04D08	1 - 16

REVISION	4	3	1										1
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

REVISIONS				
ADDED NOTE 8. AREAS F/M9: REMOVED TABLES 1&2. AREA M4,5S: REMOVED REFS TO TABLES 1&2.				
JAT	611	4707	E	6-9-81	E001
AREA D4: STRAP WAS BETWEEN B1&B2. ADDED CONN. BETWEEN TP-C 1 A78-12.				
JAT	611	4733	M5	6-10-81	E002
AREA G3, M6 E9, IC'S A62, A47 & A77 WERE 19-249 FXX. ADDED NOTE 9.				
KR	611	4900	E	12-3-81	E003

NOTES,
1. INTERNAL REFRESH OPTION IS AVAILABLE ON F03 AND F04, AND IS ENABLED IN A SPECIAL APPLICATIONS ONLY TO ENABLE, CONNECT C-C1, DISCONNECT B-B2 AND CONNECT B-B1
2.
3. SWITCHES ARE SHOWN IN POSITION DECODING MODULE 0.
4. UNLESS OTHERWISE SPECIFIED ALL LOGIC IS POWERED FROM P5S
5.
6. ◉ DENOTES INTERNAL CONNECTION ON IC'S
7. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE 1/8W, 5%
8. FOR STRAPPING INFORMATION AT LOCATION A56 & A63 REFER TO APPROPRIATE MAINTENANCE MANUAL.
9. IC LOCATIONS SHOWN IN PARENTHESIS REPRESENT ALTERNATE USE OF 19-249 FXX.

UNLESS OTHERWISE SPECIFIED

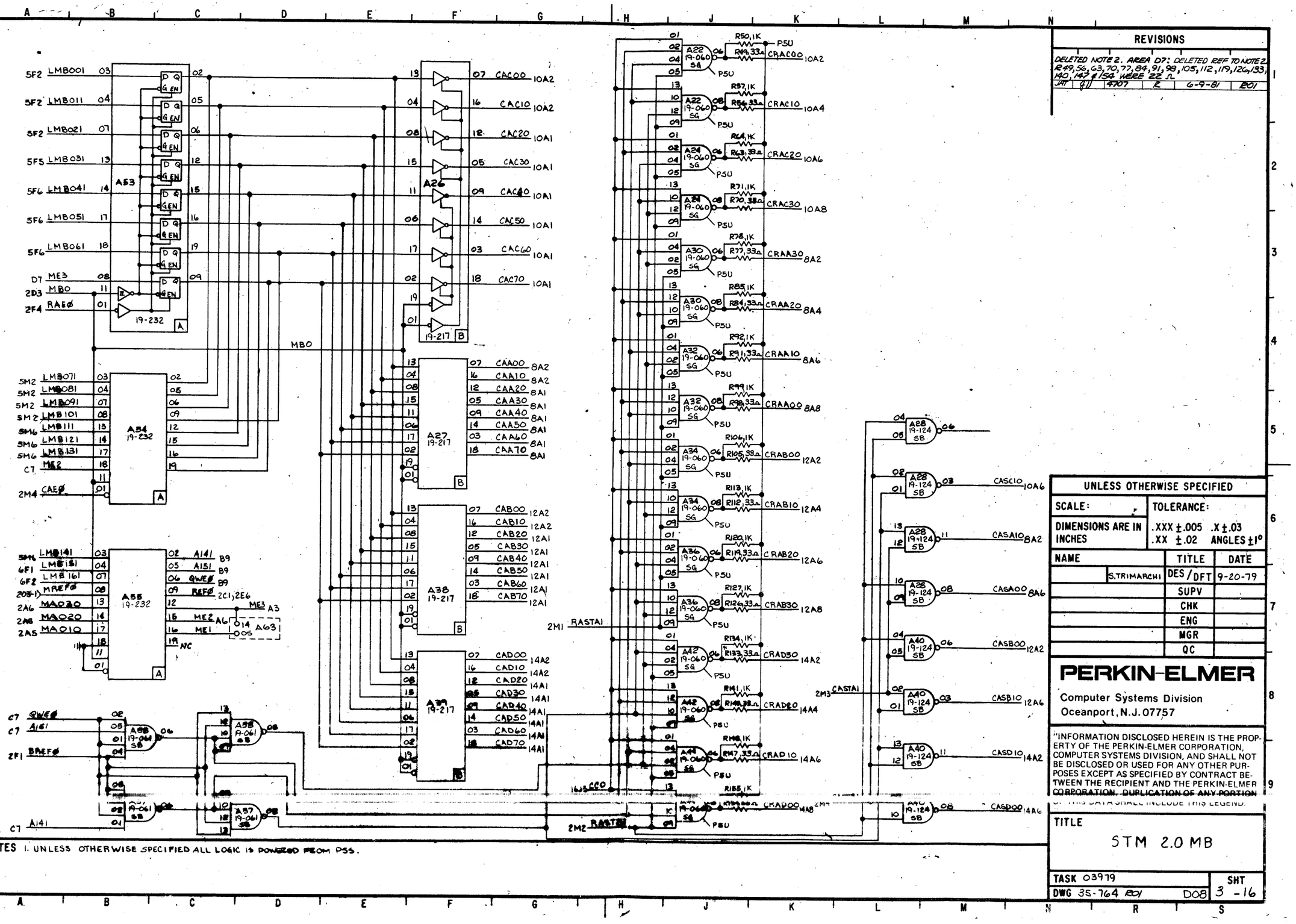
SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME	TITLE	DATE
S.TRIMARCHI	DES/DFT	9-21-79
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE
STM 2.0 MB

TASK 03979 | SHT 2 - 16
DWG 35-764 R03 D08



NOTES 1. UNLESS OTHERWISE SPECIFIED ALL LOGIC IS POWERED FROM P5S.

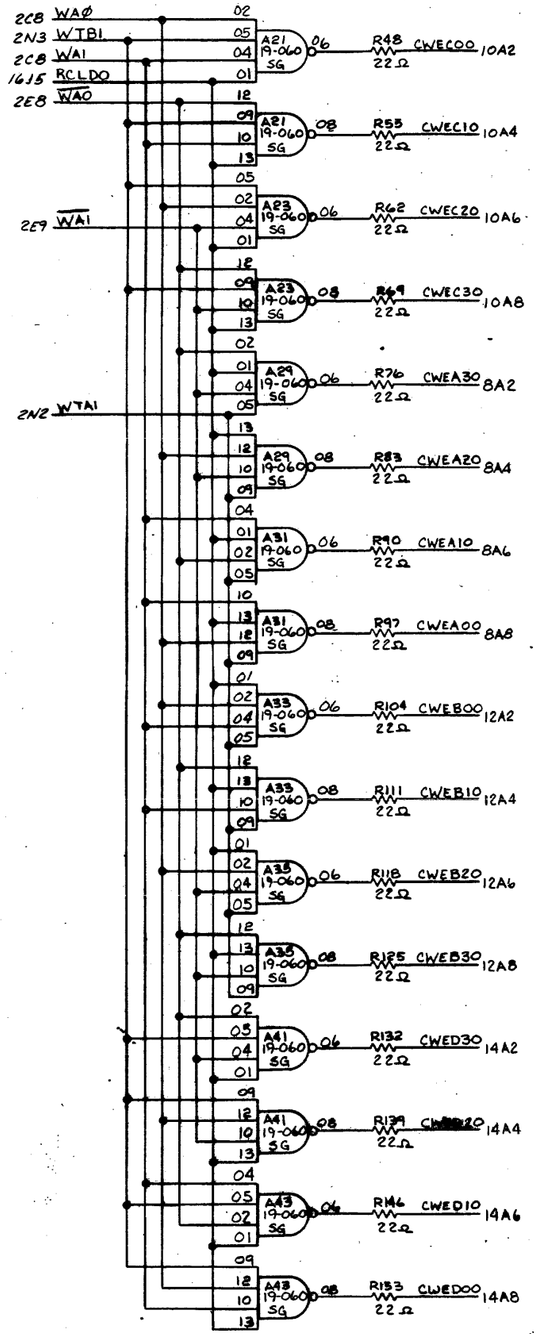
REVISIONS					
DELETED NOTE 2. AREA D7: DELETED REF TO NOTE 2. R49,56,63,70,77,84,91,98,105,112,119,126,133,140,147 & 154 WERE 22 Ω.					
JAY	411	4707	E	6-9-81	E01

UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02	ANGLES ±1°
NAME	TITLE	DATE
S.TRIMARCHI	DES/DFT	9-20-79
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE
STM 2.0 MB

TASK 03979	SHT
DWG 35-764 E01 D08	3 - 16



NOTES 1. UNLESS OTHERWISE SPECIFIED ALL LOGIC IS POWERED FROM P5S
2.

BRUNING 44-131-40079

REVISIONS

ABEA G/A: REMOVED A25 & A37.				
JAT	JJ	4733	MS	6-10-81	201

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	S.TRIMARCHI	DES/DFT	9-21-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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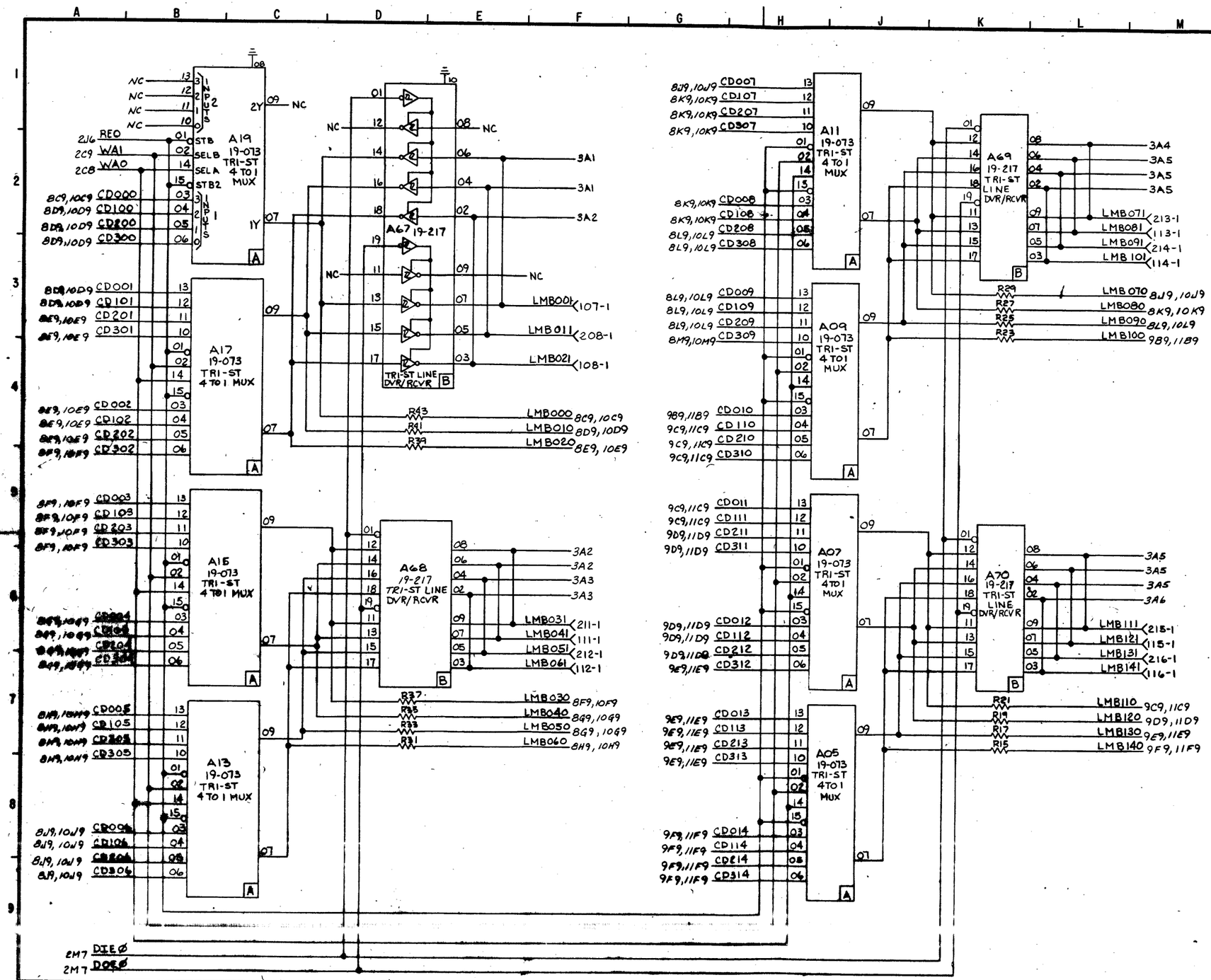
TITLE
STM 2.0 MB

TASK 03979	SHT
DWG 35-764 E01 D08	4 - 16



NOTES 1. UNLESS OTHERWISE SPECIFIED:

A) ALL LOGIC POWERED FROM P5
B) ALL RES. ARE 82Ω 1/8 W ±5%

REVISIONS

UNLESS OTHERWISE SPECIFIED			
SCALE:		TOLERANCE:	
DIMENSIONS ARE IN INCHES		.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME		TITLE	DATE
	S.TRIMARCHI	DES/DFT	8-17-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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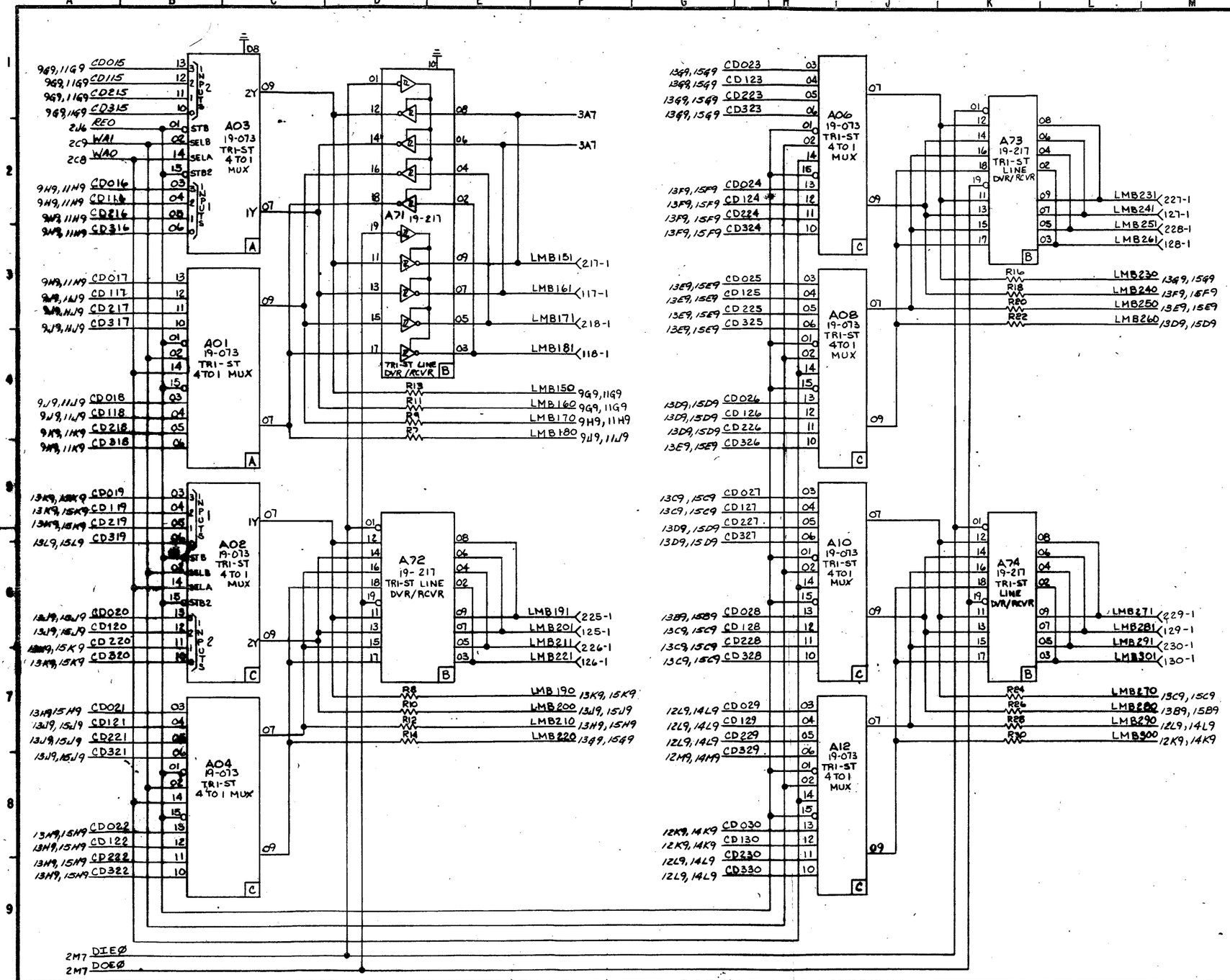
TITLE

STM 2.0MB

TASK 03979 | SHT 5 - 16

DWG 35-764 D08



NOTES 1. UNLESS OTHERWISE SPECIFIED:

A) ALL LOGIC IS POWERED FROM PS
B) ALL RES ARE 82 Ω 1/8 W 5%.

REVISIONS

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	S.TRIMARCHI	DES / DFT	8-19-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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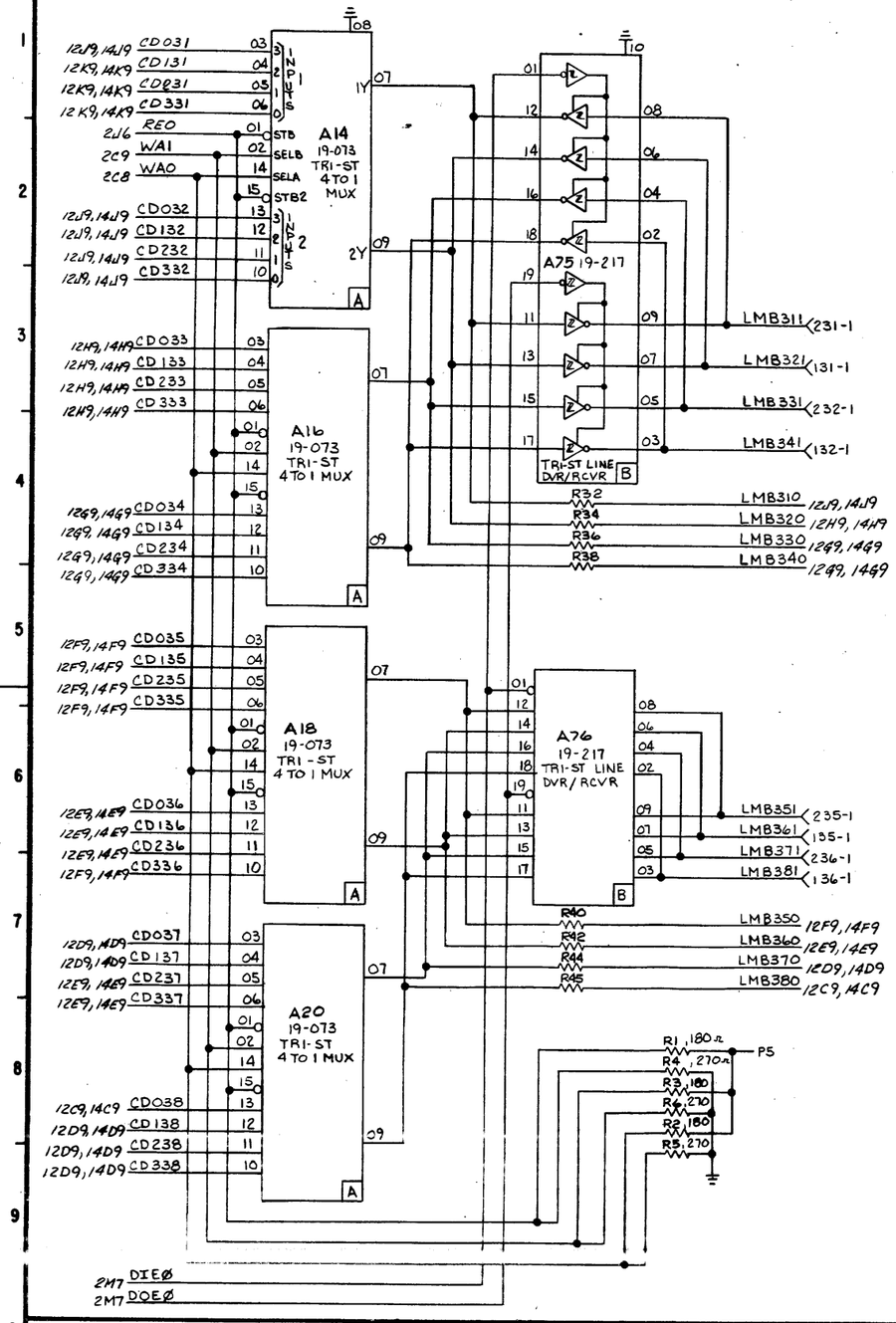
TITLE

STM 2.0 MB

TASK 03979	SHT
DWG 35-764 D08	6 - 16



NOTES 1. UNLESS OTHERWISE SPECIFIED:

A) ALL LOGIC IS POWERED BY P5
B) ALL RES ARE 82Ω, 1/8 W ± 5%.

BRUNING 44-131 40579

REVISIONS

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	S.TRIMARCHI	DES/DFT	8-19-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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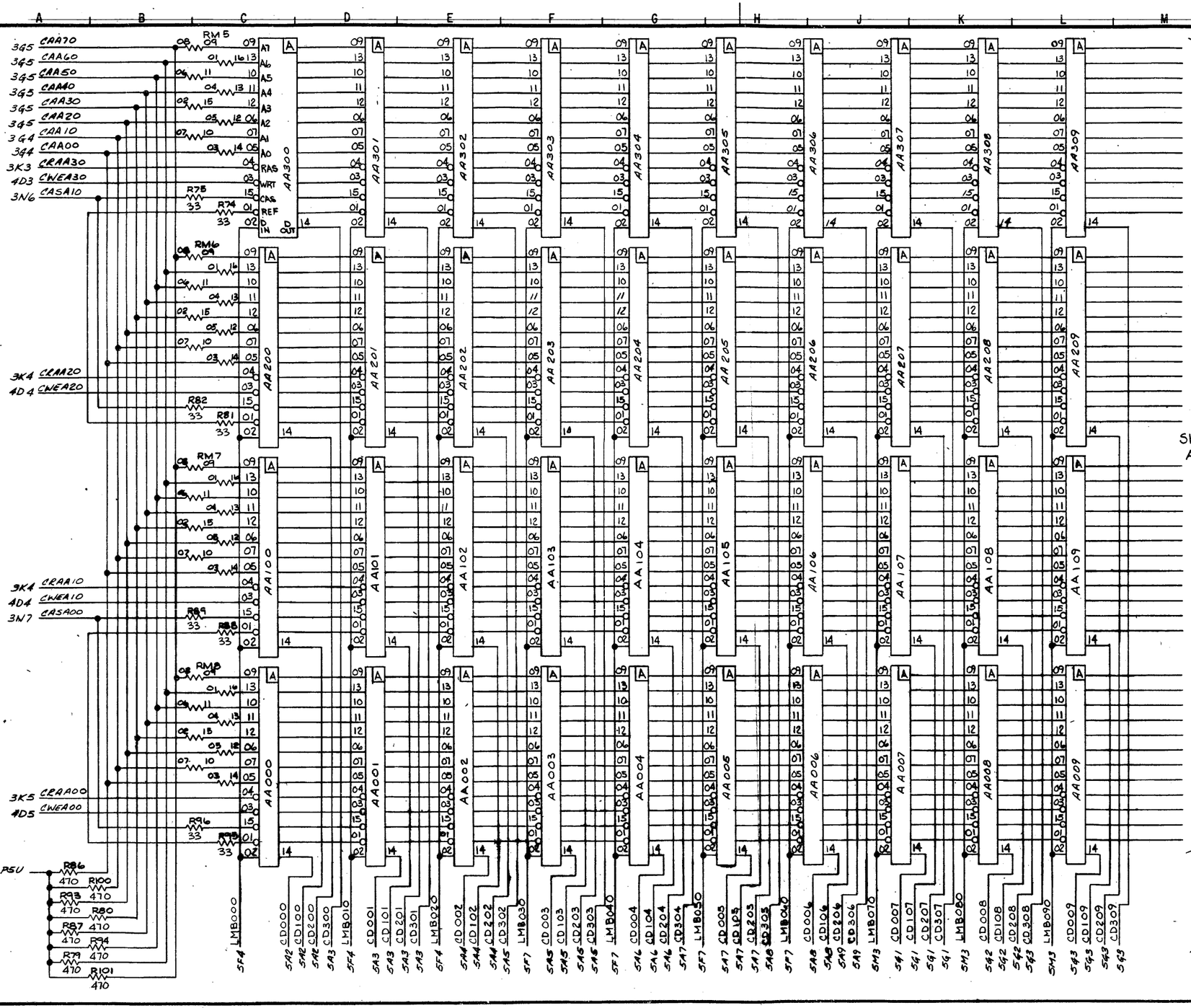
TITLE
STM 2.0 MB

TASK 03979 | SHT 7 - 16
DWG 35-764 D08



SHEET 9
A-A

REVISIONS					
AREAS A2 & A6. REMOVED CROSS-REF'S TO A25 (PG4)					
JAT	GJ	4733	MS	6-10-81	R01

NOTES

1. PER F01 VARIATION : AA000 THRU AB338 ARE 19-274 (16K RAM)
   PER F02 " AA000 " AD338 ARE 19-274 (16K RAM)
   PER F03 " AA000 " AB338 ARE 19-281 (64K RAM)
   PER F04 VARIATION : AA000 THRU AD338 ARE 19-281 (64K RAM)
2. UNLESS OTHERWISE SPECIFIED ALL LOGIC IS POWERED BY PSU
3. ALL RESISTORS ARE ¼W, ± 5%
4. RESISTORS MODULES ARE 21-073, 33Ω.

BRUNING 14-131 4079

UNLESS OTHERWISE SPECIFIED			
SCALE:		TOLERANCE:	
DIMENSIONS ARE IN INCHES		.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME		TITLE	DATE
	S.TRIMARCHI	DES / DFT	8-13-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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Computer Systems Division
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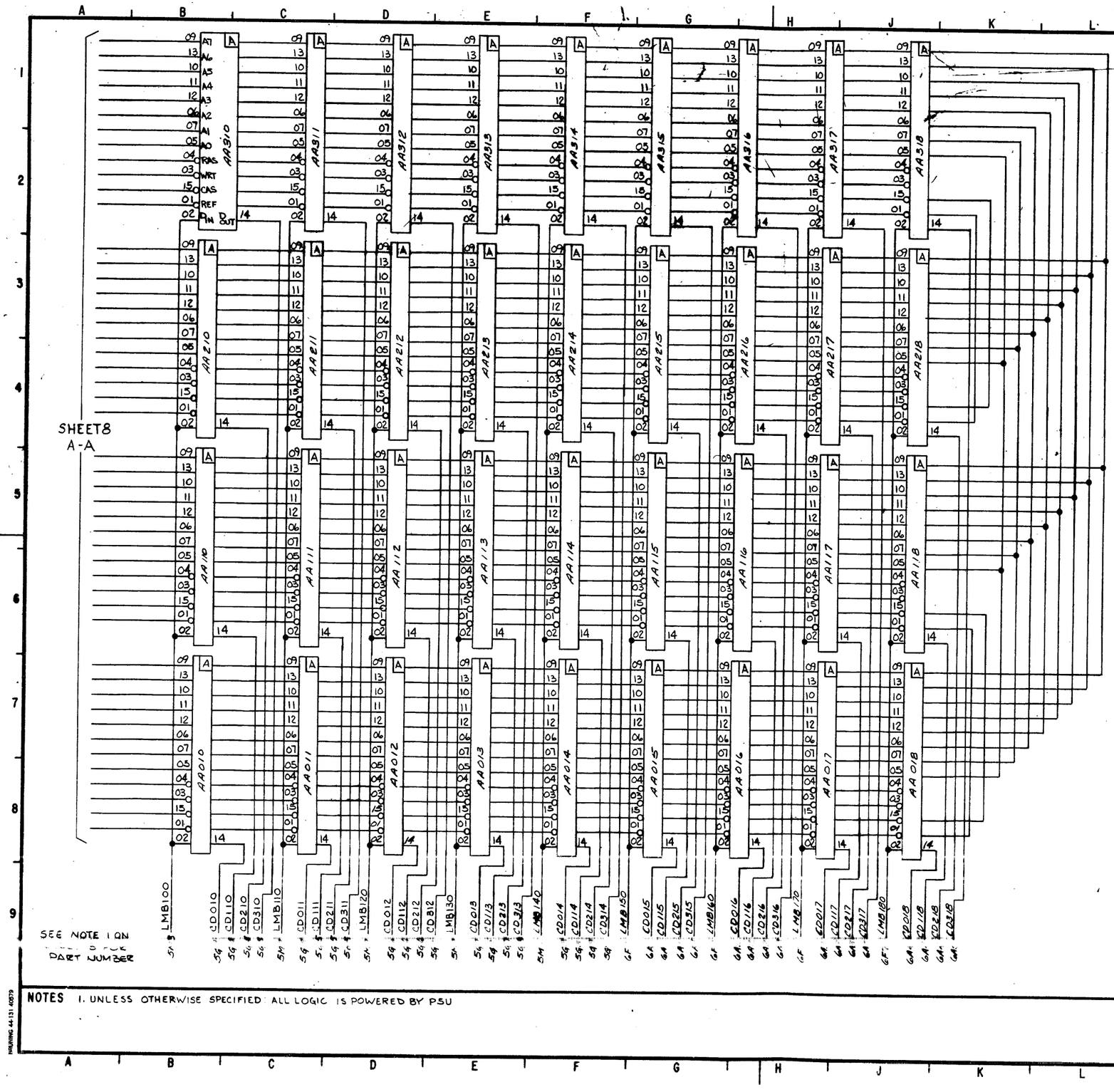
TITLE
STM 2.0 MB

TASK 03979	SHT
DWG 35-764 R01 D08	8 - 16



SHEET 8
A-A

SEE NOTE 1 ON
PART NUMBER

NOTES 1. UNLESS OTHERWISE SPECIFIED ALL LOGIC IS POWERED BY PSU

HRUNING 44-131 4/079

REVISIONS

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	S.TRIMARCHI	DES/DFT	8-13-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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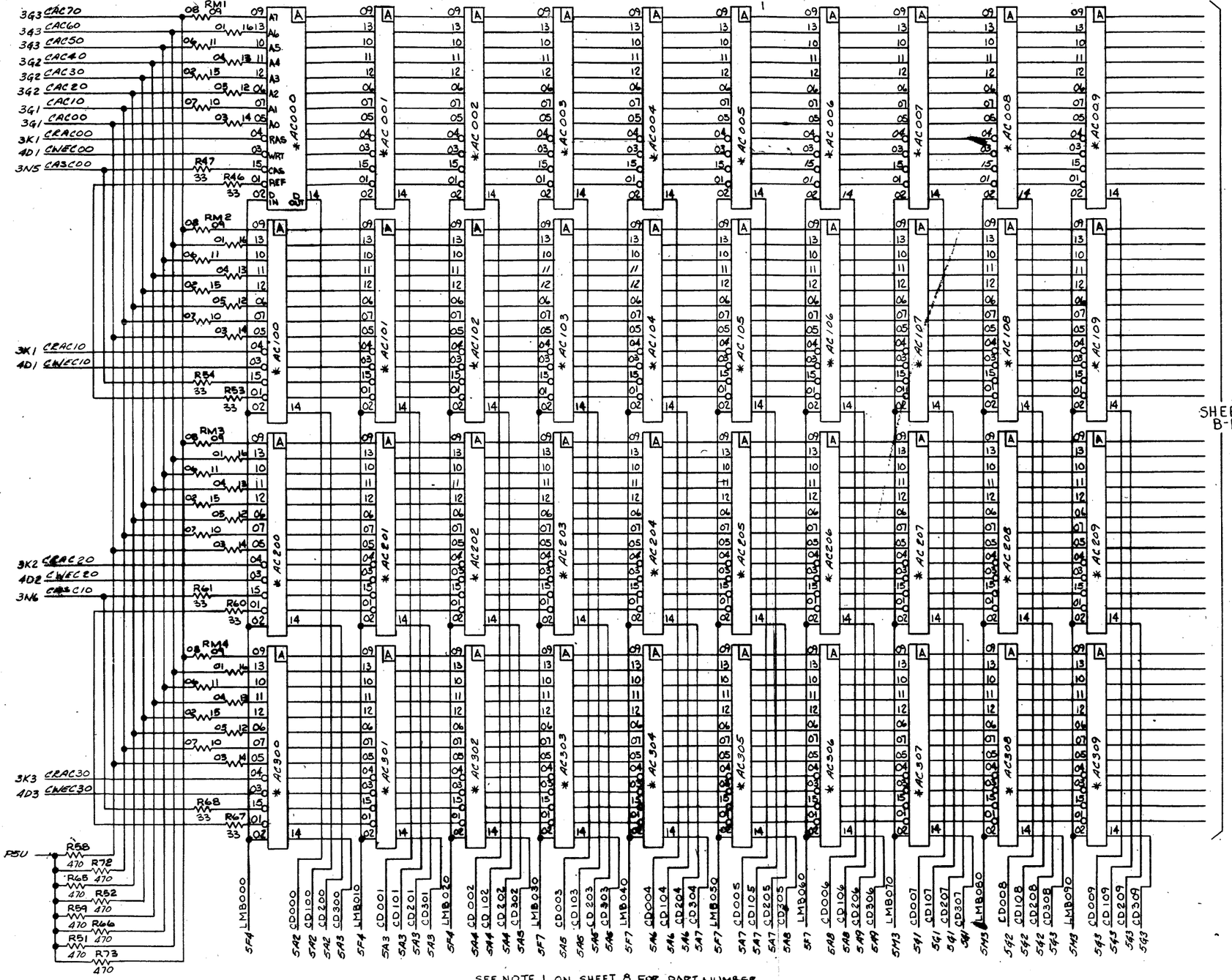
TITLE

STM 2.0 MB

TASK 03979

DWG 35-764 D08

SHT 9-16



NOTES
1. UNLESS OTHERWISE SPECIFIED ALL LOGIC IS POWERED BY PSU
2. ALL RESISTORS ARE 1/8 W ±5%
3. RESISTOR MODULES ARE 21-073, 33 Ω

PT. NO.	VARIATION
F02 & F04	AS SHOWN
F01 & F03	AS SHOWN LESS PARTS MARKED WITH AN ASTERISK (*)

REVISIONS

AREA	A2	FAG: REMOVED REFS TO A25 (Pg 4)			
JAT	AD	4733	MS	6-10-81	201

UNLESS OTHERWISE SPECIFIED

SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
	S.TRIMARCHI	DES / DFT	8-13-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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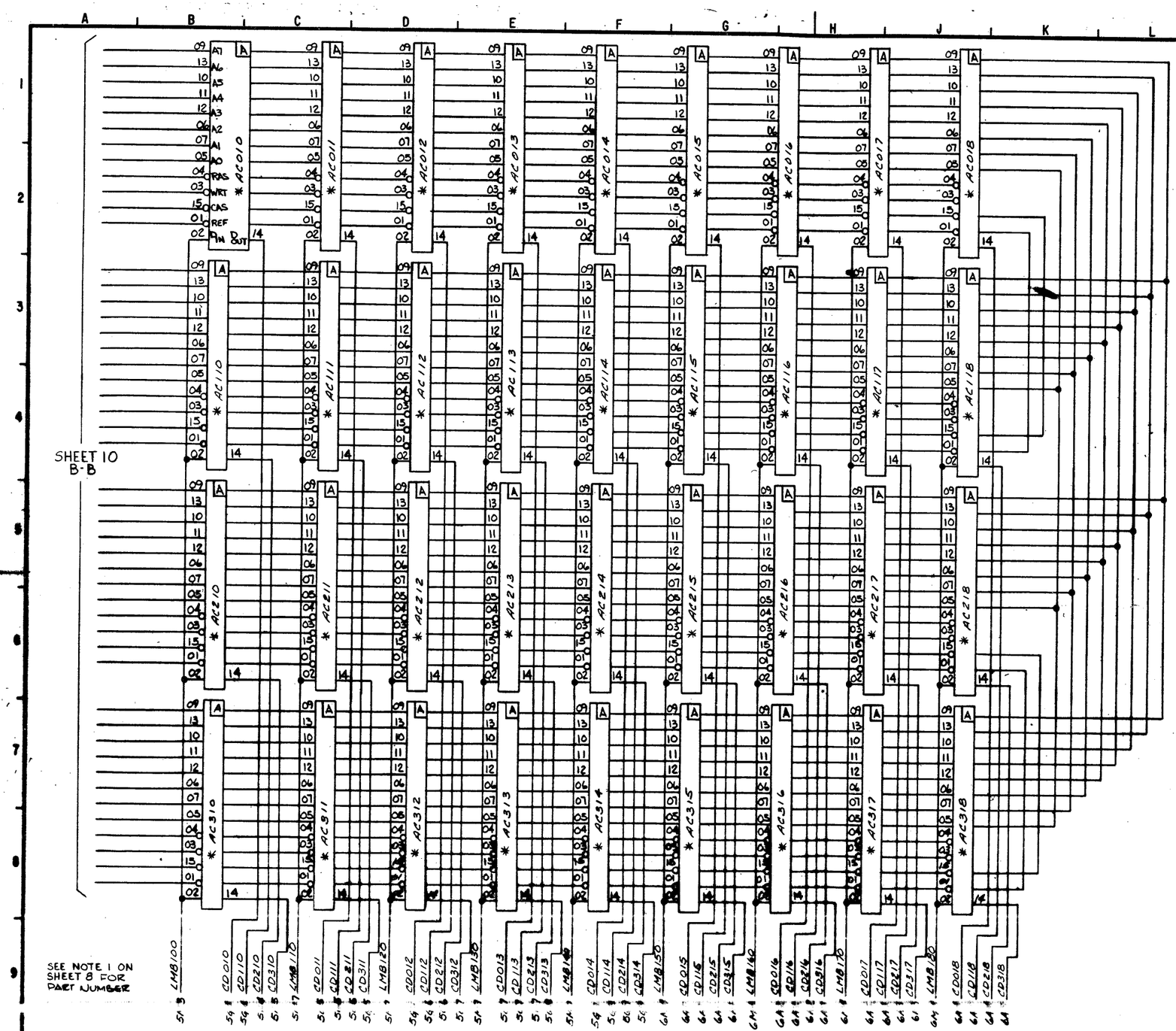
TITLE
STM 2.0MB

TASK 03979 | SHT 10-16
DWG 35-764 R01 D08

BRUNING 44-131 4579



SHEET 10
B-B

SEE NOTE 1 ON SHEET 8 FOR PART NUMBER

NOTES 1. UNLESS OTHERWISE SPECIFIED ALL LOGIC IS POWERED BY PSU.

PT. NO.	VARIATION
F02 & F04	AS SHOWN
F01 : F03	AS SHOWN LESS PARTS MARKED WITH AN ASTERISK (*)

REVISIONS

UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME	TITLE	DATE
S.TRIMARCHI	DES/DFT	8-13-79
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

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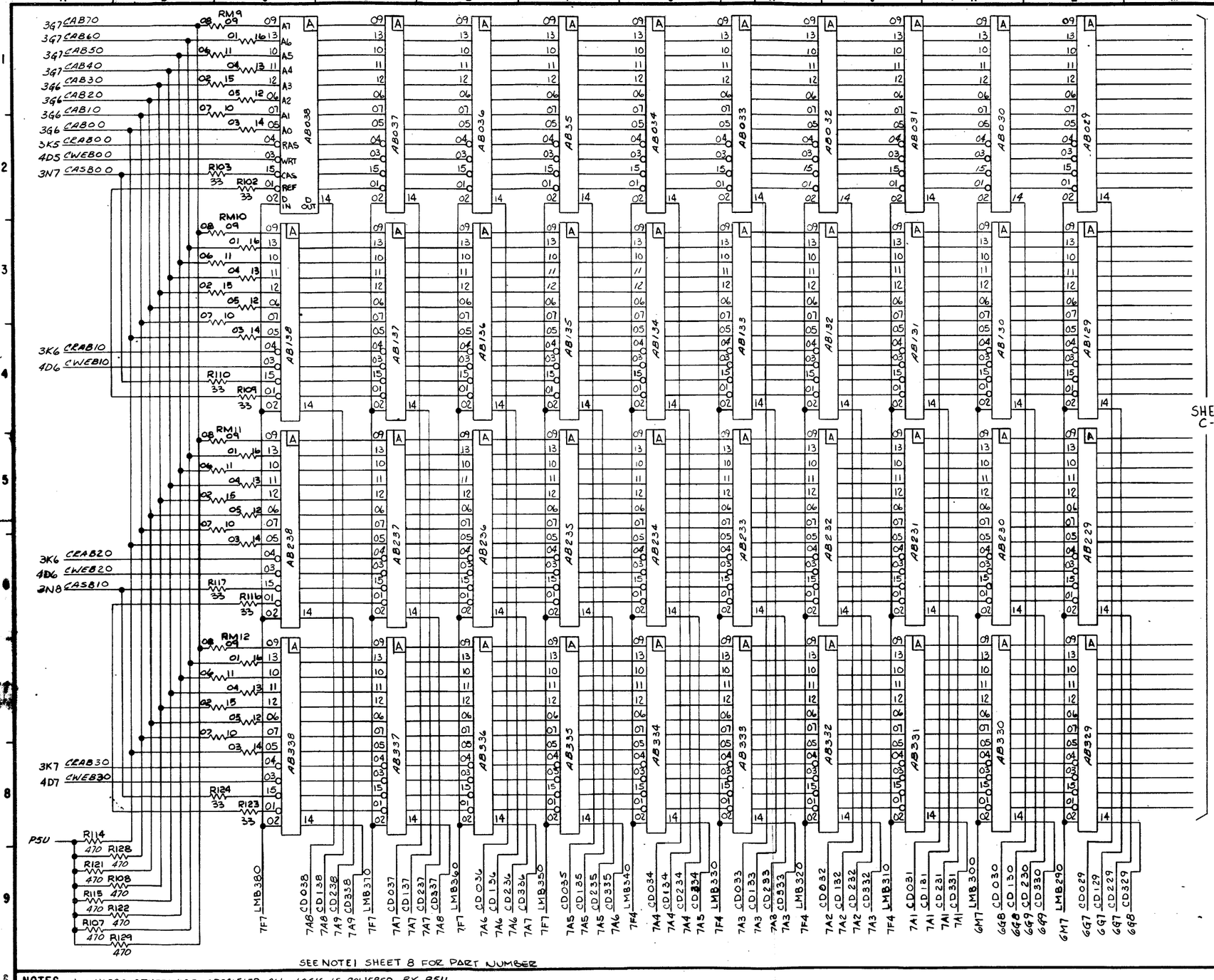
TITLE
STM 2.0 MB

TASK 03979
DWG 35-764 D08
SHT 11 - 16



NOTES
1. UNLESS OTHERWISE SPECIFIED ALL LOGIC IS POWERED BY PSU
2. ALL RESISTORS ARE 1/8 W, ± 5%
3. RESISTOR MODULES ARE 21-073, 33Ω.

REVISIONS

AREAS A2 & A6: REMOVED CROSS-REFS TO A37. (Pg 4)				
JAT	dv	4733	MS	6-10-81	R01

UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME	TITLE	DATE
S.TRIMARCHI	DES/DFT	8-13-79
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

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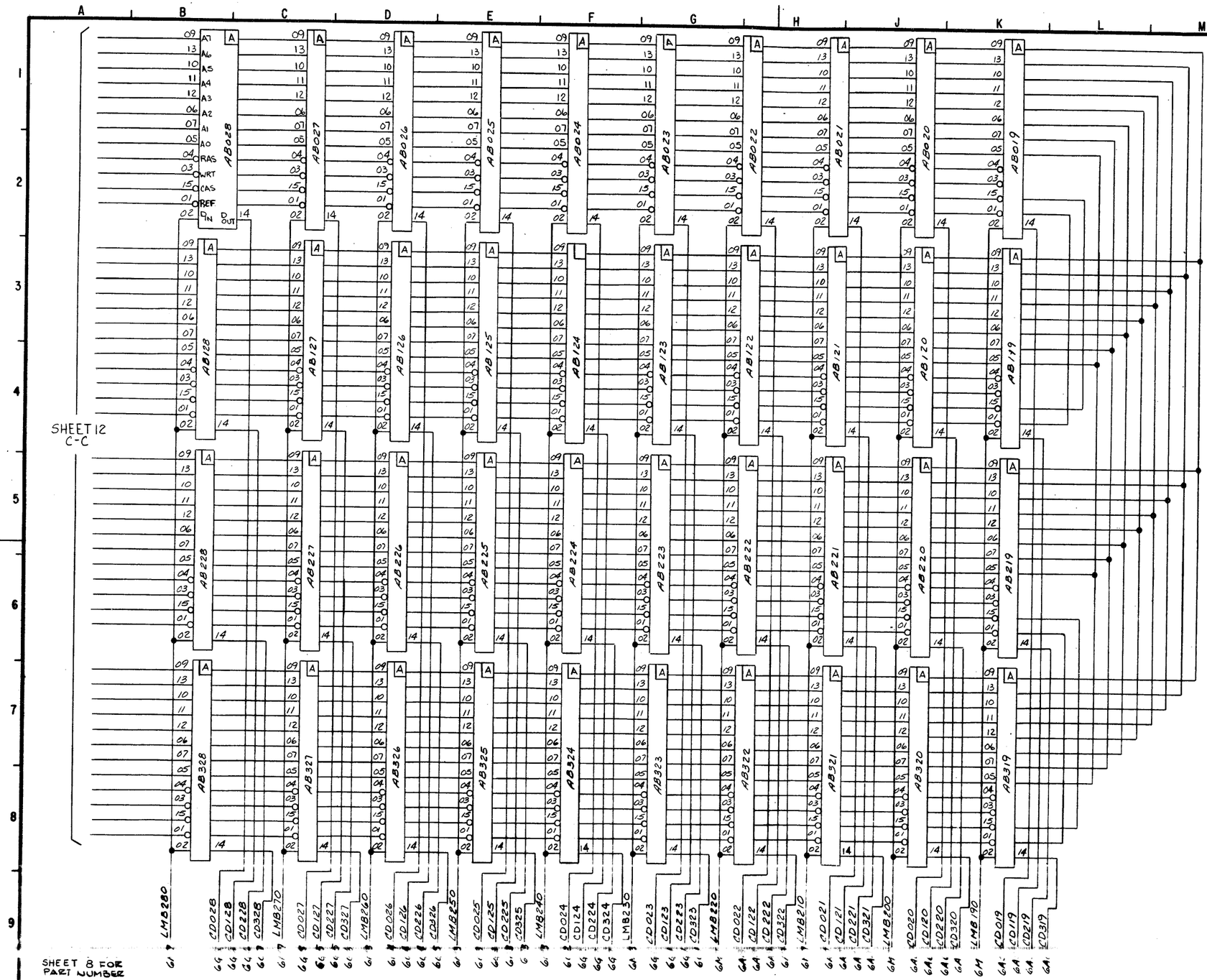
TITLE
STM 2.0 MB

TASK 03979	SHT
DWG 35-764 REV D08	12 - 16



REVISIONS

NOTES 1. UNLESS OTHERWISE SPECIFIED ALL LOGIC IS POWERED BY PSU

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	S.TRIMARCHI	DES/DFT	8-14-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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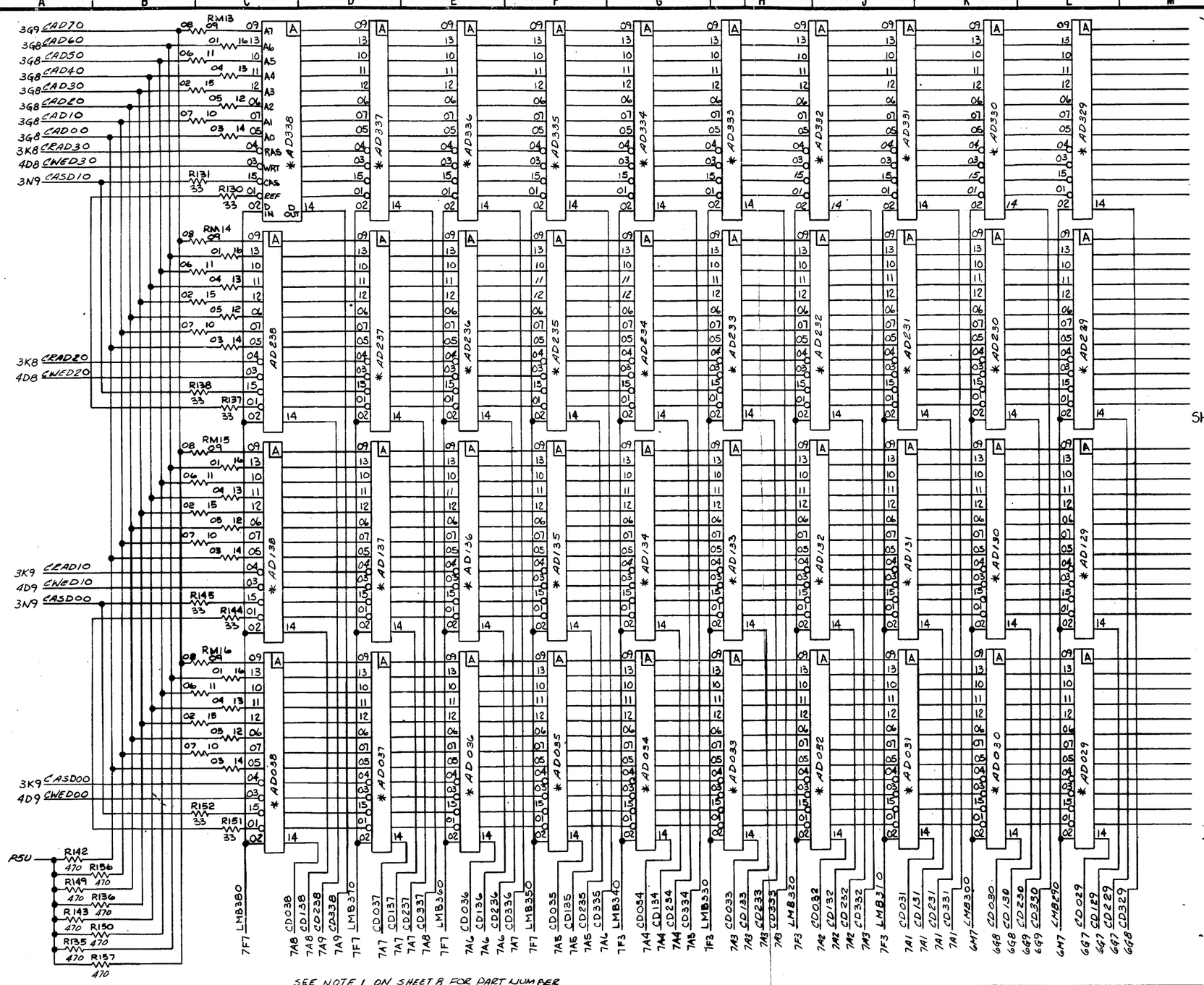
Oceanport, N.J. 07757

TITLE

STM 2.0MB

TASK 03979	SHT
DWG 35-764 D08	13 - 16

FRUNING 44-131 4/579



SHEET 15
D-D

SEE NOTE 1 ON SHEET 8 FOR PART NUMBER

NOTES 1. UNLESS OTHERWISE SPECIFIED ALL LOGIC IS POWERED BY P5U

2. ALL RESISTORS ARE 1/8 W, ±5%

3. RESISTOR MODULES ARE 21-073, 33Ω.

PART NO	VARIATION
F02 ± F04	AS SHOWN
F01 ± F03	AS SHOWN LESS PARTS MARKED WITH AN ASTERISK (*)

REVISIONS

ADDED A2 & A6. REMOVED CROSS REFS TO A37 (B4)				
JAT	GJ	4733	MS	6-10-81	R01

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	S. TRIMARCHI	DES/DFT	8-13-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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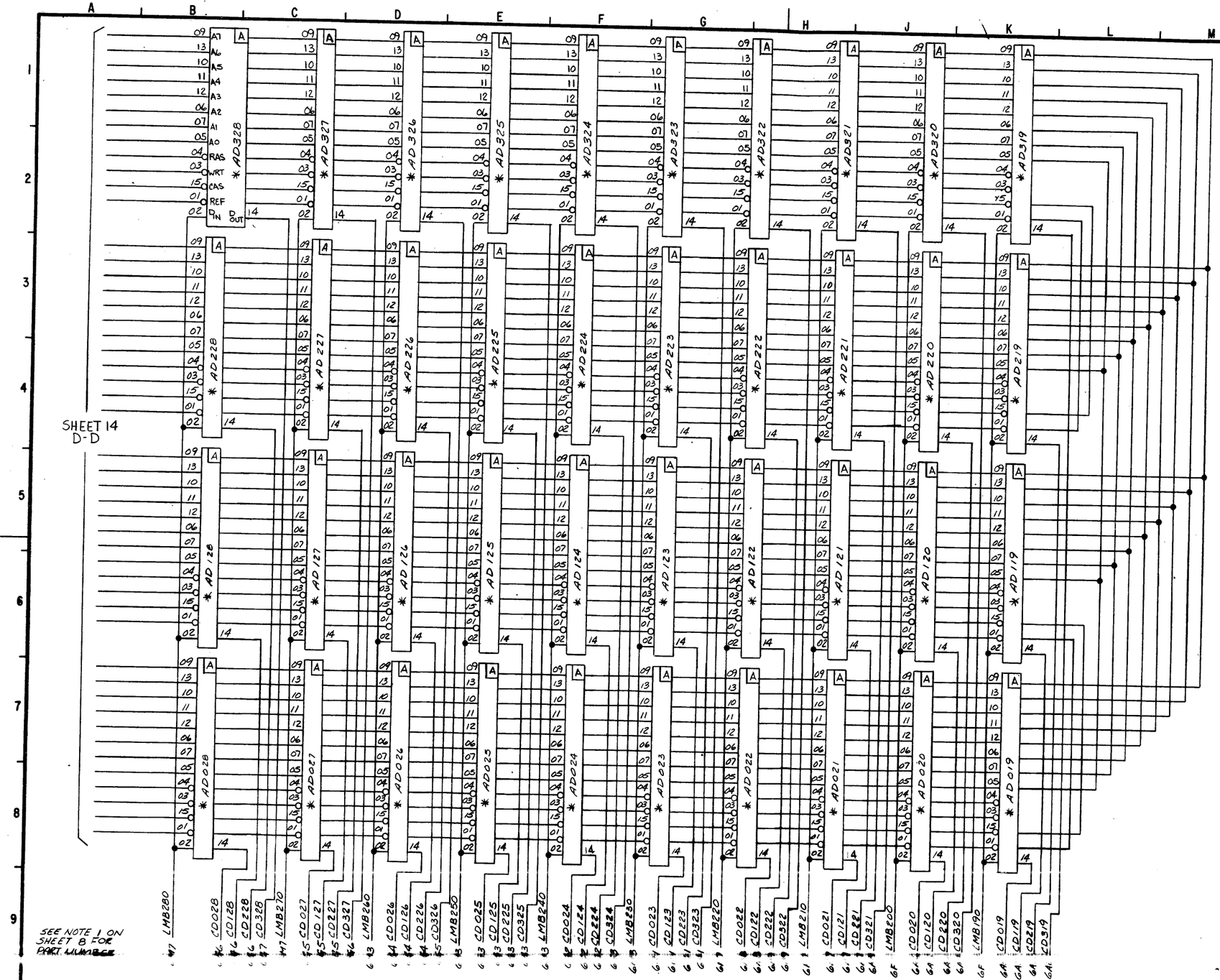
TITLE

STM 2.0 MB

TASK 03979

DWG 35-764 F01 D08

SHT 14 - 16



REVISIONS

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	S.TRIMARCHI	DES / DFT	8-14-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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TITLE

STM 2.0 MB

TASK 03979

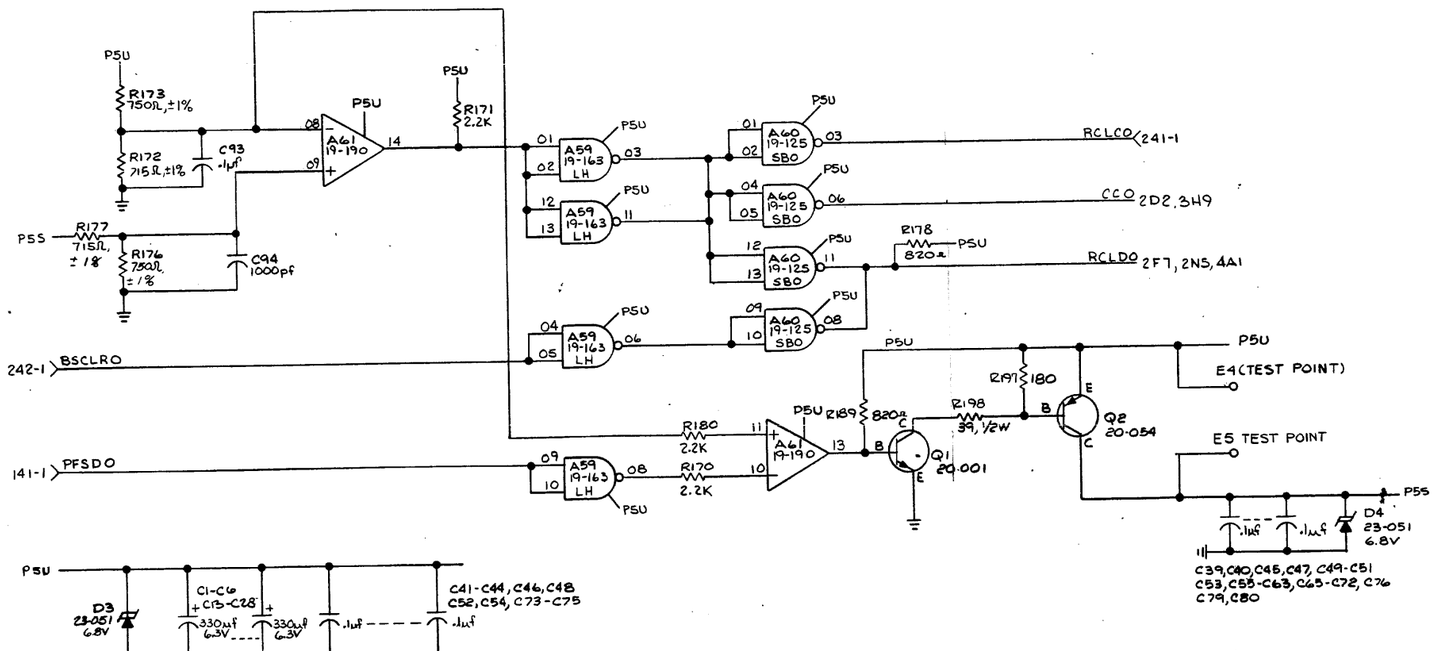
DWG 35-764 D08

SHT 15 - 16

NOTES 1. UNLESS OTHERWISE SPECIFIED ALL LOGIC IS POWER BY PSU

PT. NO.	VARIATION
F02 ; F04	AS SHOWN
F01 ; F03	AS SHOWN LESS PARTS MARKED WITH AN ASTERISK (*)

REVISIONS					
ADDED R178 AT G5					
GPS	[illegible]	4499	M	10-8-80	R01



NOTES 1. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE ¼ W, ± 5%

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	S. TRIMARCHI	DES / DFT	9-28-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

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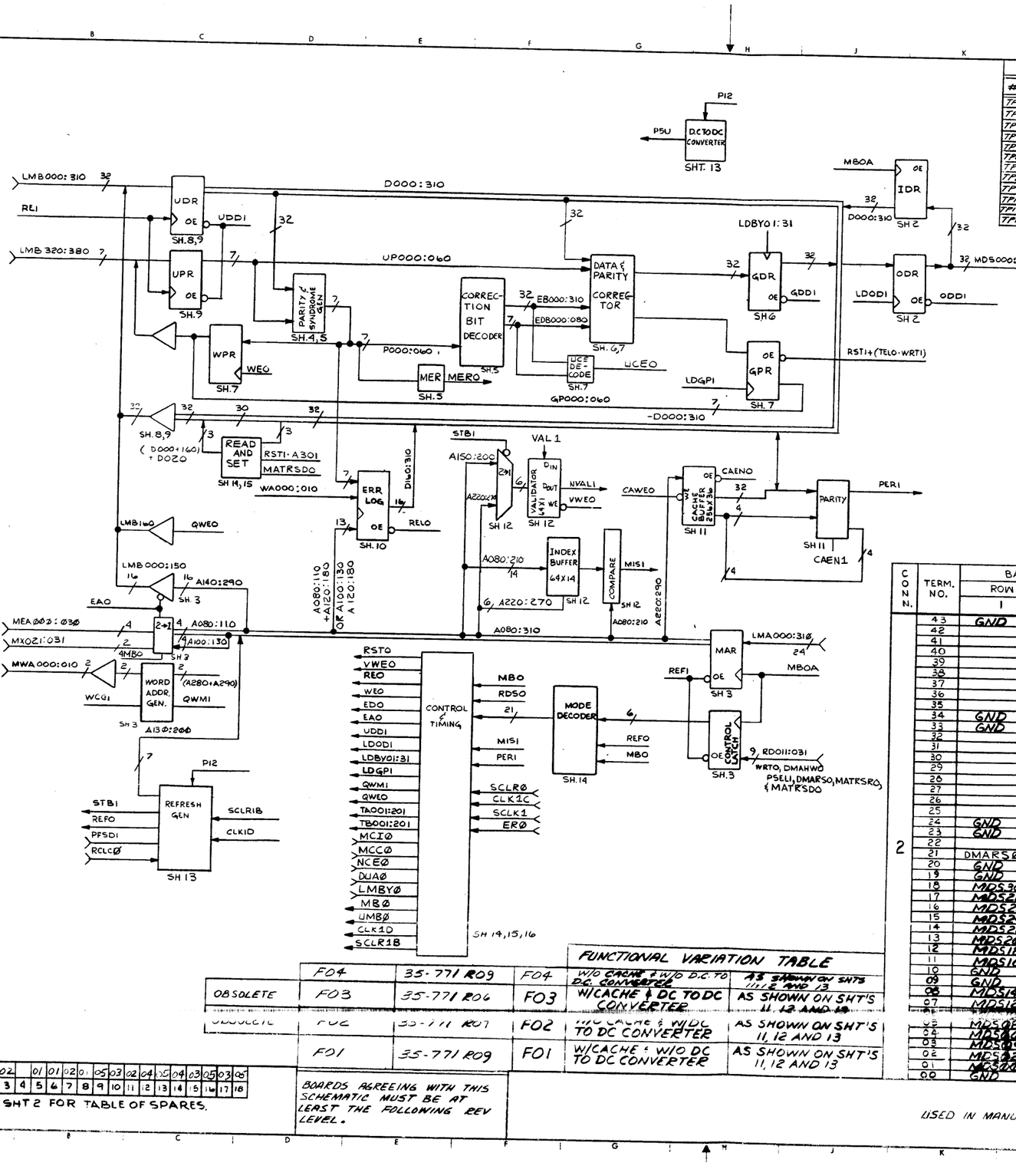
Oceanport, N.J. 07757

TITLE
STM 2.0MB

TASK 03979	SHT
DWG 35-764 R01 D08	16 - 16



TEST POINTS

#	MNEMONIC	SHT.
TP1	GND	5
TP2	DERRO	5
TP3	GND	12
TP4	TP4	12
TP5	MBIC	13
TP6	TP6	13
TP7	GND	16
TP8	BYPI	16
TP9	TP9	5
TP10	GND	5
TP11	DERRB	7
TP12	GND	7

BACK PANEL MAP

CONN.	TERM. NO.	ROW 1	ROW 2
	43	GND	GND
	42		ØSCLRØ
	41	PESDØ	RCLCØ
	40		
	39		
	38		MXØ21
	37	MXØ11	MXØ31
	36	LMB381	LMB371
	35	LMB361	LMB351
	34	GND	GND
	33	GND	GND
	32	LMB341	LMB331
	31	LMB321	LMB311
	30	LMB301	LMB291
	29	LMB281	LMB271
	28	LMB261	LMB251
	27	LMB241	LMB231
	26	LMB221	LMB211
	25	LMB201	LMB191
	24	GND	GND
	23	GND	GND
	22	RDØØ1	RDØ11
	21	RDØ21	RDØ31
	20	GND	GND
	19	GND	GND
	18	LMB181	LMB171
	17	LMB161	LMB151
	16	LMB141	LMB131
	15	LMB121	LMB111
	14	LMB101	LMB091
	13	LMB081	LMB071
	12	LMB061	LMB051
	11	LMB041	LMB031
	10	GND	GND
	09	GND	GND
	08	LMB021	LMB011
	07	LMB001	
	06	MEAØ2Ø	MEAØ3Ø
	05	MEAØØØ	MEAØ1Ø
	04	MWAØØ1	MWAØ11
	03	MCCØ	MREFØ
	02	MCIØ	MRDSØ
	01	MREØ	MWEØ
	00	GND	GND

CONN.	TERM. NO.	ROW 1	ROW 2
	43	GND	GND
	42		
	41		
	40		
	39		
	38		
	37		
	36		
	35		
	34	GND	GND
	33	GND	GND
	32		
	31		
	30		
	29		
	28		
	27		
	26		
	25		
	24	GND	GND
	23	GND	GND
	22		MATRSDØ
	21	DMARSØ	MATRSRØ
	20	GND	GND
	19	GND	GND
	18	MDS3ØØ	MDS31Ø
	17	MDS28Ø	MDS29Ø
	16	MDS26Ø	MDS27Ø
	15	MDS24Ø	MDS25Ø
	14	MDS22Ø	MDS23Ø
	13	MDS2ØØ	MDS21Ø
	12	MDS18Ø	MDS19Ø
	11	MDS16Ø	MDS17Ø
	10	GND	GND
	09	GND	GND
	08	MDS14Ø	MDS15Ø
	07	MDS12Ø	MDS13Ø
	06	MDS1ØØ	MDS11Ø
	05	MDS08Ø	MDS09Ø
	04	MDS06Ø	MDS07Ø
	03	MDS04Ø	MDS05Ø
	02	MDS02Ø	MDS03Ø
	01	MDS000	MDS01Ø
	00	GND	GND

CONN.	TERM. NO.	ROW 1	ROW 2
	43	GND	GND
	42	GND	SCLRØ
	41		
	40		
	39		
	38		
	37		
	36	GND	GND
	35		
	34	GND	GND
	33	GND	GND
	32		
	31		
	30		
	29		
	28		
	27		
	26		
	25		
	24	GND	GND
	23	GND	GND
	22	NVMØ	
	21	CLMC	SCLK1
	20	GND	GND
	19	GND	GND
	18	NCEØ	GMWEØ
	17	DUAØ	PSEL1
	16	DMAHWØ	LMBYØ
	15	ERØ	WRTØ
	14	LMA3ØØ	LMA31Ø
	13	LMA28Ø	LMA29Ø
	12	LMA26Ø	LMA27Ø
	11	LMA24Ø	LMA25Ø
	10	GND	GND
	09	GND	GND
	08	LMA22Ø	LMA23Ø
	07	LMA2ØØ	LMA21Ø
	06	LMA18Ø	LMA19Ø
	05	LMA16Ø	LMA17Ø
	04	LMA14Ø	LMA15Ø
	03	LMA12Ø	LMA13Ø
	02	LMA1ØØ	LMA11Ø
	01	LMA08Ø	LMA09Ø
	00	GND	GND

FUNCTIONAL VARIATION TABLE

	F04	35-771 R09	F04	W/O CACHE & W/O D.C. TO D.C. CONVERTER	AS SHOWN ON SHTS 11, 12 AND 13
OBSOLETE	F03	35-771 R06	F03	W/CACHE & DC TO DC CONVERTER	AS SHOWN ON SHT'S 11, 12 AND 13
OBSOLETE	F02	35-111 R07	F02	W/O CACHE & W/DC TO DC CONVERTER	AS SHOWN ON SHT'S 11, 12 AND 13
	F01	35-771 R09	F01	W/CACHE & W/O DC TO DC CONVERTER	AS SHOWN ON SHT'S 11, 12 AND 13

REVISIONS	08	05	02		01	01	02		05	03	02	04	05	04	03	05	03	05
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

NOTE - SEE SHT 2 FOR TABLE OF SPARES.

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REV LEVEL.

USED IN MANUAL 47-011 & 47-009

PERKIN ELMER

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Oceanport, N.J 07757

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
DEV PROD		

1) VARIATION TABLE FOR W/A: NOT SPEC. 35-771 WAS SPEC AS R00. SHEETS 2, 7, 8, 9, 10, 11, 12, 13, 14, 16, 17 & 18 WERE R00.

WW 4592 | M | 11-5-80 | R01

RELEASED FOR PRODUCTION
ENG. S. [illegible] DATE 11-

REVISED SHTS 1 & 12
VT 4597 | MS | 2-5-81 | R02

2 REVISED SHTS 23, 7, 10, 11, 13, 14.
JAT 4635 | MS | 6-9-81 | R03

REVISED SHTS 1, 9, 13 & 18:
WW 4793 | MS | 7-21-81 | R04

REV'D SHTS 1-3, 9, 13, 15-18: REV TABLE, 35-771 F01, F03 & F04 WAS R03: 35-111 F02 WAS R04;
WW 4764 | MS | 10-13-81 | R05

3 REV TABLE 35-771 F01, F03 & F04 WAS R05. 35-771 F02 WAS R06. F02 & F03 HAVE BEEN MADE OBSOLETE. REVISED SHTS 1, 2, 9, 12 & 14-18
WW 4891 | MS | 11-6-81 | R06

REVISE SHTS 1, 16 & 18 35-771 F01 & F04 WERE R06.
KR 4900 | E | 11-20-81 | R07

4 REV'D SHTS 1, 2, 5, 6, 9, 10, 12, 13-16; 35-771 F01 & F04 WERE R07.
WW 5089 | MS | 8-13-82 | R08

SCALE -			
	E. GREENSTEIN	TEST	11-14-80
	B. GRAY	DRAFT	11-14-80
	R. ACEO	CHK	11-14-80
	S. AGRAWAL	ENGR	11-14-80
	R. BERGER	QC	11-14-80
	D. FRANKENBERGER	M&R	11-14-80

TITLE SCHEMATIC
LOCAL BANK CONTROLLER

DWG NO 03976 | SHEET 1 OF 18
SIZE D | SCALE NONE | 35-771 R08

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J 07757

REVISIONS				
IN TABLE OF SPARES DELETED OGR11 AND 20H-03. ADDED 17A, 19-236, 08 & 11, 22D-12 & 19M10				
JAT	4542		11-5-80	R01
SPARE GATE CHART REMOVED 19M13 & ADDED 22D03, 12B04				
JAT	4635	MS	6-3-81	R02
IN SPARE GATE CHART, ADDED 19D: DELETED 18A, 19-234 SPARE 13:				
JAT	4769	MS	10-13-81	R03
ADDED OGM TO SPARE GATE TABLE				
JLV	4891	MS	11-6-81	R04
DELETED 05A, 19-063, OUTPUT 09 FROM SPARES TABLE.				
JAT	5089	MS	8-19-82	R05

PROCESSOR DATA BUS

01K 19-232 (ODR)

00K 19-232

03K 19-232

04K 19-232

OUTPUT DATA REGISTER

01R 19-232

00R 19-232

07R 19-232

08R 19-232

INPUT DATA REGISTER

INPUT OUTPUT DATA REGISTER

13C 19-126 5G

03J 19-236 5A

REF. DES.	PART NUMBER	SPARE OUTPUTS
23M	19-055	06
05M	19-234	04, 10, 13
20H	19-055	06

TABLE OF SPARES

REF. DESIGN	PART NUMBER	SPARE OUTPUTS
19H	19-058	12
17E	19-126	08
16E	19-055	11
15C	19-131	07, 06, 10, 11, 14, 15
01F	19-241	06
19M	19-234	, 10
07C	19-236	08,
06C	19-235	03, 08, 11
05H	19-234	04, 10, 13
05F	19-234	13
12R	19-163	06, 08 & 11
10A	19-163	03, 08
23D	19-154	08, 10, 12
05E	19-127	11
13H	19-126	06
13C	19-126	08
14D	19-234	04, 10, 13
25F	19-124	03, 06
09R	19-125	08, 11
09B	19-057	04
25H	19-059	12
19A	19-059	12
22F	19-058	06, 12
22D	19-057	08, 06, 10, 12
20B	19-057	06, 10, 12
20A	19-057	06
12B	19-057	04
03F	19-057	04, 10 & 12
17A	19-236	08, 11
06M	19-235	08, 11
10A	19-163	11
09A	19-160	11

TABLE OF SPARES

SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .01, X ± .1, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	B. GRAY	DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC
LBC
TASC NO. 03976
DWG NO. 35-771R05D08
SHEET OF 2–18

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J 07757

REVISIONS				
AREA K9: REMOVED CROSS REF TO/FROM 12B02				
JAT	4635	MS	6-8-81	R001
AREA H-7, ADDED NEW IC 19D: 23F05 DID GO TO NEI: 15L2				
JAH	4769	MS	10-13-81	R02

PROCESSOR ADDRESS BUS

4MB/16MB MODULE ID

QUAD WORD COUNTER

NOTES:
1. STRAP 215-5 (TP10) TO 216-5(TP9) FOR 4MB SYSTEM. FOR SYSTEMS LARGER THAN 4MB, REMOVE THE STRAP.

SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	B. GRAY	DRAFT	1-11-80
		CHK	
		ENGR	

TITLE SCHEMATIC
L8C
TASK NO. 03976
DWG NO. 35-771 R08D08
SHEET OF 3—18

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

15KØ DØØØA
6N1,G1 DØ1Ø
15N5,G5 DØ2ØA
6F3,G7 D21Ø
6N2,G1 DØ4Ø
6N2,G5 DØ5Ø
6N2,G2 DØ6Ø
15KØ D16ØA
6N6,G6 D13Ø

07J
19-223
9 BIT EVEN/ODD PARITY GEN/CHK
A

ODD → 06
EVEN → 05

6F6 D29Ø
6F6 D24Ø
6F7,G4 D3ØØ
6N6 DØ8Ø
9H5 UPØØ*

07K
19-223
9BIT EVEN/ODD PARITY GEN/CHK
A

06 → 02, 03
05 → 05, 04

07H
19-126
STTL

ODD/ODD
EVEN/EVEN
ODD

06 PØØØ 5H5, 7D6, 10B8

6N2,G1 DØ3Ø
6N2,G2 DØ7Ø
6F2 D17Ø
6N6 DØ9Ø
6N6,G3 D12Ø
6F2,G3 D2ØØ

08J
19-223
9BIT EVEN/ODD PARITY GEN/CHK
A

06 → 01, 13
03 → 10, 09

ODD/EVEN
ODD/EVEN
EVEN

08 PØ1Ø 5H5, 7D6, 10B8

6F3,G7 D22Ø
6N7,G6 D14Ø
6F6 D25Ø
9H8 UPØ1Ø

08K
19-223
9BIT EVEN/ODD PARITY GEN/CHK
A

06 → 06
05 → 05

A5 DØ3Ø
A1 DØ1Ø
A2 DØ4Ø
A6 DØ7Ø
A2 DØ6Ø
6F2 D18Ø
6N7 D15Ø
6N6 D1ØØ
A6 D2ØØ

09J
19-223
9BIT EVEN/ODD PARITY GEN/CHK
A

ODD → 06
EVEN → 05

6G3 D23Ø
A6 D12Ø
6F6 D26Ø
6F7 D31Ø
A3 D3ØØ
9H9 UPØ2Ø

09K
19-223
9BIT EVEN/ODD PARITY GEN/CHK
A

06 → 04, 05
05 → 03, 02

09H
19-126
STTL

ODD/ODD
EVEN/EVEN
ODD

06 PØ2Ø 5H5, 7D6, 10B8

A1 DØ2ØA
A2 DØ5Ø
6N6 D11Ø
A3 D13Ø
A7 D14Ø
6F2 D19Ø

10J
19-223
9BIT EVEN/ODD PARITY GEN/CHK
A

06 → 01, 13
05 → 10, 09

ODD/EVEN
ODD/EVEN
EVEN

08 PØ3Ø 5G8, 7D7, .08B

6F6 D27Ø
A2 D21Ø
A7 D22Ø
9H9 UPØ3Ø

10K
19-223
9BIT EVEN/ODD PARITY GEN/CHK
A

06 → 06
05 → 05

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PARITY GENERATOR

SCALE —	NAME	TITLE	DATE
		DRAFT	
		CHK	
		ENGR	

TITLE : SCHEMATIC
LBC

TASK NO 03976
DWG NO 35-771 D08
SHEET OF 4 - 18

DRAWING 44-131 24538

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS						
AREA L-3, 06J10 WAS 06J01 IN ERROR. CHG'D PER M102.						
4H	AV	5089	MS	8-18-82	R01	

11J 19-223 9 BIT EVEN/ODD PARITY GEN/CHK — ODD 06, EVEN 05
6N2 D03Ø 08 A
6N6 D08Ø 09 B
15K6 D000A 10 C
6N6 D07Ø 11 D
6N6 D10Ø 12 E
6N1 D01Ø 13 F
15N5 D02ØA 01 G
6F2,G1 D18Ø 02 H
6F1,G1 D17Ø 04 I

11K 19-223 9 BIT EVEN/ODD PARITY GEN/CHK — 06, 05
15K6,G1 DK6ØA 08
6N6 D11Ø 09
6F2,G2 D19Ø 10
6F7 D31Ø 11
9H8 UPØ4Ø 12
6F6,G3 D28Ø 13
01, 02, 04

12J 19-223 9 BIT EVEN/ODD PARITY GEN/CHK — 06, 05
6F6,G2 D24Ø 08
6F6,G2 D25Ø 09
10, 11, 12, 13
6N6 D12Ø 01
6N6 D13Ø 02
6N6 D14Ø 04

12K 19-223 9 BIT EVEN/ODD PARITY GEN/CHK — 06, 05
6N7 D15Ø 08
6F6,G3 D26Ø 09
6F6,G3 D27Ø 10
11
6F6 D29Ø 12
9H8 UPØ5Ø 13
6F7 D30Ø 01
02
04

11H 19-126 STTL
04 ODD/ODD 05
03 EVEN/EVEN 02
06

12J: 06 → 01, 13 ODD/EVEN; 05 → 10, 09 ODD/EVEN
EVEN: 08 → PØ5Ø 48, 7D7, 10B8

13J 19-223 9 BIT EVEN/ODD PARITY GEN/CHK — 06, 05
A3 D16ØA 08
A3 D17Ø 09
A2 D18Ø 10
A3 D19Ø 11
6F3 D22Ø 12
6F4 D23Ø 13
A5 D24Ø 01
A5 D25Ø 02
A7 D26Ø 04

13K 19-223 9 BIT EVEN/ODD PARITY GEN/CHK — 06, 05
A7 D27Ø 08
A4 D28Ø 09
6F3 D20Ø 10
6F3 D21Ø 11
12
9H9 UPØ6Ø 13
01
02
04

13H 19-126 STTL
01, 13 ODD/EVEN; 10, 09 ODD/EVEN → 08

PØ4Ø 48, 7D7, 10B8

4F4 PØØØ
4F6 PØ1Ø
4M4 PØ2Ø
15L2 MEØ
DERRO
7D7, 10B8 PØ6Ø

08H 19-129 3 TO 8 DECODER (SEL A, B, C; GEA, GEB, GE1; DVB)
01 → 15 DBØØ 6H7, 7A3
02 → 14 DB1Ø 6H2, 7A1
03 → 13 DB2Ø 6H6, 7A2
12 DB3Ø 6AB
11 DB4Ø 6A9, 7A3
10 DB5Ø 6A9
09 DB6Ø 6H2
07 DB7Ø 6H3

P5 — 75 03F 11 — 1K — 01 — 03F 19-057 SG — 02
TP1 224-5 — TP2 223-5 — SEE NOTE 1

10H 19-129 3 TO 8 DECODER
01 → 15 DAØØ 6A2, 7A5
02 → 14 DA1Ø 6A2
03 → 13 DA2Ø 6A1
12 DA3Ø 6A3
11 DA4Ø 6A1
10 DA5Ø NC
09 DA6Ø NC
07 DA7Ø NC

4M6 PØ3Ø
F4 PØ4Ø
F5 PØ5Ø

12H 19-129 3 TO 8 DECODER
01 → 15 DCØØ 6A3, 7A2
02 → 14 DC1Ø 6A4, 7A3
03 → 13 DC2Ø 6A1, 7A4
12 DC3Ø 6A3
11 DC4Ø 6A5, 7A5
10 DC5Ø 6A7
09 DC6Ø 6A8
07 DC7Ø 6H7

06J 19-082 SGO
04 PØ6Ø
NC, NC, NC
03 PØ5Ø
10 PØ4Ø
08 MERO → 15N2

06H 19-082 SGO
01 PØ3Ø
06 PØ2Ø
03 PØ1Ø
10 PØØØ
08

10 03F 76 470 P5

05 03F 19-057 SG 06 MERI → 15E8, 7N6

NOTES:
1. TO DISABLE ERROR CORRECTION CONNECT 224-5 TO 223-5.

MEMORY ERROR AND PARITY GENERATOR

SCALE – | NAME | DATE | TITLE: SCHEMATIC LEC | DRAFT | CHK | ENGR
SIZE 03976 | SHEET OF 5 — 18
DWG 35-771 R0/D08

BRUNING 44-231 24538

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
AREA N-2, 01E19, "7A6" WAS "7G6" IN ERROR. CHG'D PER M102.				
LTR	BY	SDB9	MS	8-18-82 R01

DATA LATCH

DATA LATCH

ERROR CORRECTOR

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SCALE –	NAME	TITLE	DATE
TOLERANCE .XXX ± .005, .XX ± .02, . ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

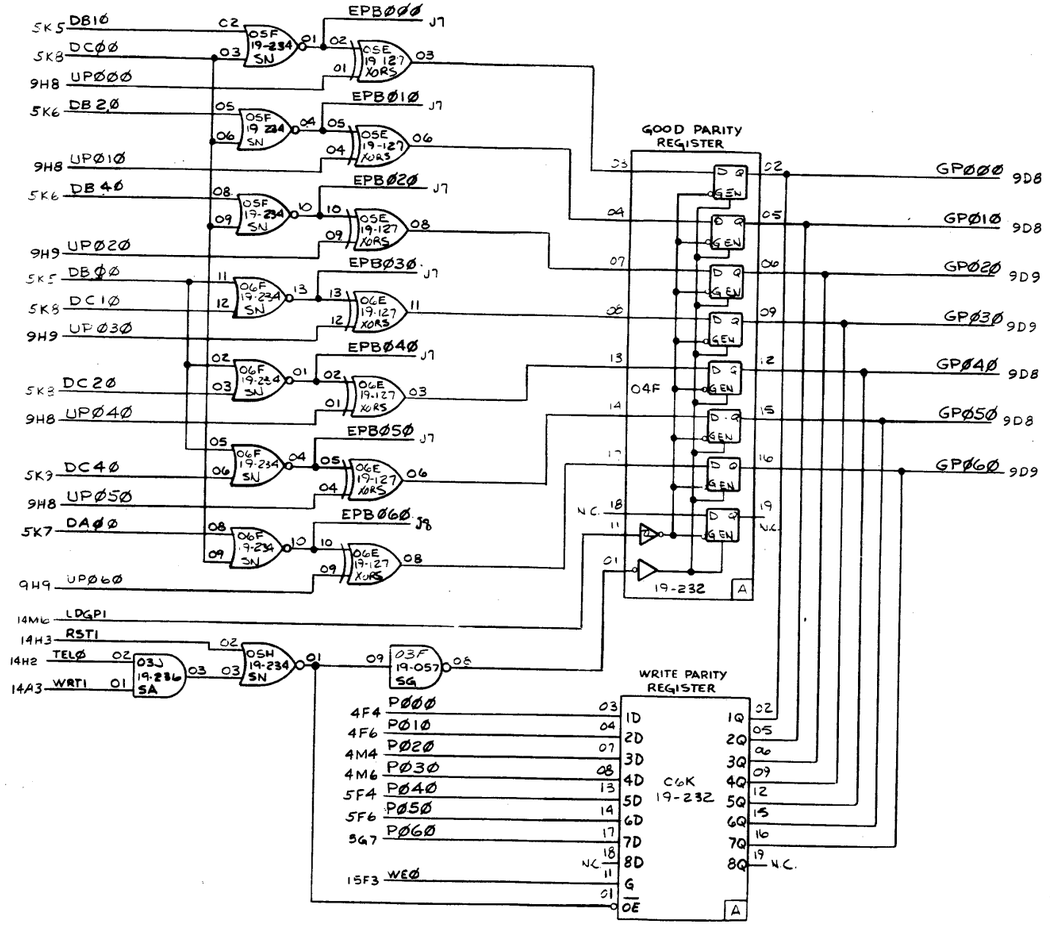
TITLE : SCHEMATIC
LBC

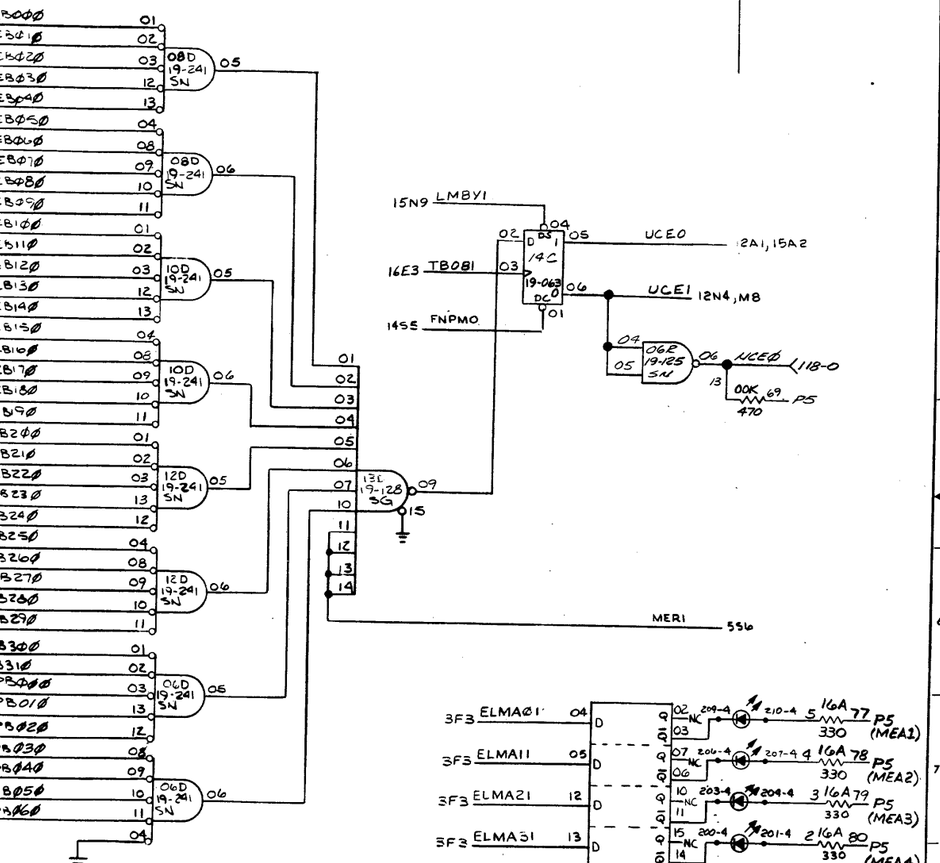
TABS NO. 03976 — SHEET OF 6 — 18
SYM NO. 35-771R01D08

DRAWING 44-231 24538

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS
IN AREA R3 UCE0 WAS SPEC AS CROSS REFERENCED TO 9N3, 12A1, 15A2. IN AREA R4 GATE 06R & RESISTOR 00K WERE NOT SPEC.
JAT 00 4542 1-4-80 ECO
IC 06R AREA K8: PIN 9 WAS TO 3K9, A191. PIN 10 WAS TO KMS BELI.
JAT 00 4635 MS 6-8-81 ECO





NOTES:
1. FOR CUSTOMER SERVICE ONLY:
TO TURN OFF UCE/NPM AND MODULE I.D. LAMPS;
CONNECT TP11 TO TP12 MOMENTARILY. DO NOT STRAP.
MAKE SURE TO REMOVE THE JUMPER.

PARITY CORRECTOR & UNCORRECTABLE ERROR

SCALE -	NAME	TITLE	DATE
	B. GRAY	DRAFT	
		CHK	
		ENGR	

TITLE : SCHEMATIC
LBC
03976
35-771 R02 D08
SHEET 7 OF 18

DRAWING 44231 24538

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
125, 127, 145, 147, 175 & 177 WERE 21-090F03, 330 & 470Ω.				
WP	4542	M	11-4-80	R01

LMB BUS
DRIVERS AND RECEIVERS

SCALE—	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	P MARCUS	DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC
LBC

TASK NO. 03976
DWG NO. 35-771R01D08
SHEET OF 8 — 18

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS			
12T 12S 9T 9S 17T & 17S WERE 21-090 F03, 330 & 470Ω. 21R03 WAS GMVFØ TO CONN 218-D.			
' IN AREA R8 21R11 WAS SPEC AS MNEMONIC "UCEO"; 21R09 WAS SPEC AS "NCEO" TO CONN 118-D. 21R17 WAS SPEC AS GOING TO 19M10, 19M & 22D GATES WERE DELETED. 20M & 06R & 00K WERE NOT SPEC.			
JJF	4542	11-4-80	R01
AREA 5B, CROSS REF. FOR BMVFØ WAS N7, L7:			
JWM	4793	MS 7-21-81	R02
AREA N8: RES. 00K WAS 09M, 1K TO P5; ADDED 13E8			
JWM	4769	MS 10-13-81	R03
AREA K7-K9: 15M17 WAS NC; 15M04 WAS MNEM. QWEØ, DEST. 16S7; 15M19 WAS NC; 15M01 WAS MNEM. EAØ, DEST. 16S4; 15M03 WAS NC; 15M16 WAS MNEM. LMB16I, DEST 8R6. ADDED 18K RESISTOR TO 15M16			
JWM	4891	MS 11-5-81	R04
AREA R-8: DELETED 13E9 FROM BMVFØ. CHG'D PER M102			
JWM	5089	MS 12-28-81	R05

LMB BUS
DRIVERS AND RECEIVERS

SCALE—

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

TITLE: SCHEMATIC
LBC

PART NO. 03976
DWG NO. 35-771R5008
SHEET 9 OF 18

PERKIN-ELMER

Oceanport, N.J.

WRITE/READ ERROR LOGGER ADDRESS MUX

ERROR LOGGER SHIFT REGISTER

ERROR LOGGER SHIFT REGISTER

ERROR LOGGER

REVISIONS				
IN AREA A8 07M11 WAS TO LDGP1 LOC. 14M6. ADDED 17A				
JAH	AV	9542	1-4-80	R01
AREA B8: ADDED 2/8 TO IC 21M PIN 06				
JAT	AV	4635	MS	6-8-81	R02
AREA N3, DELETED 09M 11K RES.), BETWEEN 06R03 & P5.				
JAH	AV	5089	MSB-18-82	R03

SCALE—	NAME	TITLE	DATE
TOLERANCE .xxx ± .000, .xx ± .02, .x ± .09, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC LBC

TASK NO. 03976 SHEET OF

DWG NO. 35-7717 R03 D08 10—18

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
IN NOTE 1, FO4 VARIATION WAS NOT SPEC.				
	9512		11-5-80	R01
AREAS K1-K8: ADDED 4 (02R/4SR) RESISTOR PACKAGES. ADDED NOTE 2.				
JAT	9635	WIS	6-9-81	R02

CACHE 256 x 36

16H7 TAA12Ø
14G4 SFW1
12S7 HIT1
16D1 TB061
14H3 SPW1
15L2 MEI
16S7 QWM1
16B4 TB061
16H2 TB12Ø
16E4 TB08Ø
FW WRITE
PW WRITE
QW ERR
QW NO ERR
03J 19-236 SA
Z0C 19-062
08 CAWE0
1656 CAEN0
1657 CAEN1

3E8 A22Ø
3E8 A23Ø
3E8 A24Ø
3E8 A25Ø
3E8 A26Ø
3E9 A27Ø
3K3 A28Ø
3K3 A29Ø

21K * 19-254 256X9 RAM
22K * 19-254 256X9 RAM
24K * 19-254 256X9 RAM
25K * 19-254 256X9 RAM

CACHE PARITY CHECK
21J 19-223 9BIT EVEN/ODD PARITY GEN/CHK
22J * 19-223 9BIT EVEN/ODD PARITY GEN/CHK
24J 19-223 9BIT EVEN/ODD PARITY GEN/CHK
25J 19-223 9BIT EVEN/ODD PARITY GEN/CHK
EVEN OUT 05 NC
ODD OUT 06
23K * 19-056 SGO
23J * 19-055 SG
21H 19-060 SG
06 PER1 16L8, 15A8
SEE NOTE 1
SEE NOTE 2
PS

XRP2 14J3
1256 CHIT1
16R9 CPER1
13A4 SCLR0C
12A 19-069 SF
09 NC
07
DS
DC
218-4
219-4
330
16A *
76
CACHE PARITY ERROR

NOTE 1. DEPOPULATE COMPONENTS MARKED WITH AN ASTERISK FOR F02 & F04 VARIATION.
2 DEPOPULATE COMPONENTS MARKED WITH A TRIANGLE (Δ) FOR F01 & F03 VARIATIONS.

CACHE & CACHE PARITY

SCALE–	NAME	TITLE	DATE
UNLESS OTHERWISE SPECIFIED	B. GRAY / D. STINE	DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC
LBC
TAB NO. 03976
DWG NO. 35-771 R02D08
SHEET OF 11—18

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
IN NOTE 2 FOR VARIATION WAS NOT SPEC.				
HF AW	1542	11-5-80	R01	
AREA D2, REMOVED ASTERISK FROM 21D				
VT AW	4597	MS 2-5-81	R02	
AREA N6; ADDED "MISB1" AND REF 15AB TO 18F09 ADDED "MISA1" & REF 15AB TO 18F10: ADDED "MISS1" & REF 15A7 TO 18F81				
CACHE VALIDATOR PER M102	JW 4891	MS 11-5-81	R03	
AREA R-6, DELETED "5A9" FROM M151.				
AH AJ	5089	MS 8-18-82	R04	

STB0
13H2 TELO
14H2 RSTO
14H2 UCEO
7S4

21H* 19-060 SG
21E 19-055 SG
VALØ
VALI N1
N3
25M* 19-065 2 TO 1 MUX
13H2 STB1
A220 A150 A230 A160 A240 A170 A250 A180
ENB 24M* 19-065 2 TO 1 MUX SEL
VALI H1
26R* 19-237 256X1 RAM
DATA IN
DATA OUT
NVALI 16L9, N7, 15AB

21D 19-259 (1/2) 2-TO-4 LINE DECODER/DEMULTIPLEXER
3D7, K1 A220
3D8, K1 A230
16S7 QWM1
16H7 TPAA121
19A 19-055 SG

ADBØ : A21Ø
TAG FIELD

25A* 25B* 25C* 25E* 19-075 16x4 REG STK
3D1 ADBØ
3D2 AD90
3D2 AD100
3D2 AD110

24A* 24B* 24C* 24E* 19-075 16x4 REG STK
3D3 A120
3D3 A130
3D3 A140
3D4, K1 A150

23A* 23B* 23C* 23E* 19-075 16x4 REG STK
ADRS A B C D
DATA IN
OUT PUTS S1 S2 S3 S4
K1, 3D5 A160
K1, 3D5 A170
K1, 3D5 A180
H1, 3D5 A190

22A* 22B* 22C* 22E* 19-075 16x4 REG STK
A220 : A270
INDEX ADDRESS
K1, 3D8 A240
K1, 3D8 A250
H1, 3D8 A260
H1, 3D8 A270
SEE NOTE 2

25D* 19-154
24D* 19-154
23D 19-154

21A* 21B* 21C* 21D* 21E* 19-279
EOUT
EIN
TAG COMPARE

F1 VALØ
16D5 TA061
S7 HITI
16E3 TBOB1
16A3 SPW1
7R4 UCE1
HIT
UCE NORM MEM OP
UCE (QWM)
QWM
21C* 19-062 SG

07C 19-234 SA
16S7 QWM1
REFI 13J3
UCECLRØ 14S4
15AB MISB1
15AB MISA1
18F 19-241 SN
22D 19-057
MISI 16L8
22Z-5 TP4
TP3 18F 1K
22Z-5
P5
15A7 MISS1
PSU
15A 19-234 SN
NVALI N3
CHITI 11N6
STBD 13H2
HITI N9, 11C2
16D8 TABB1
13N8 MBIA
N.C.

CACHE HIT DETECTOR

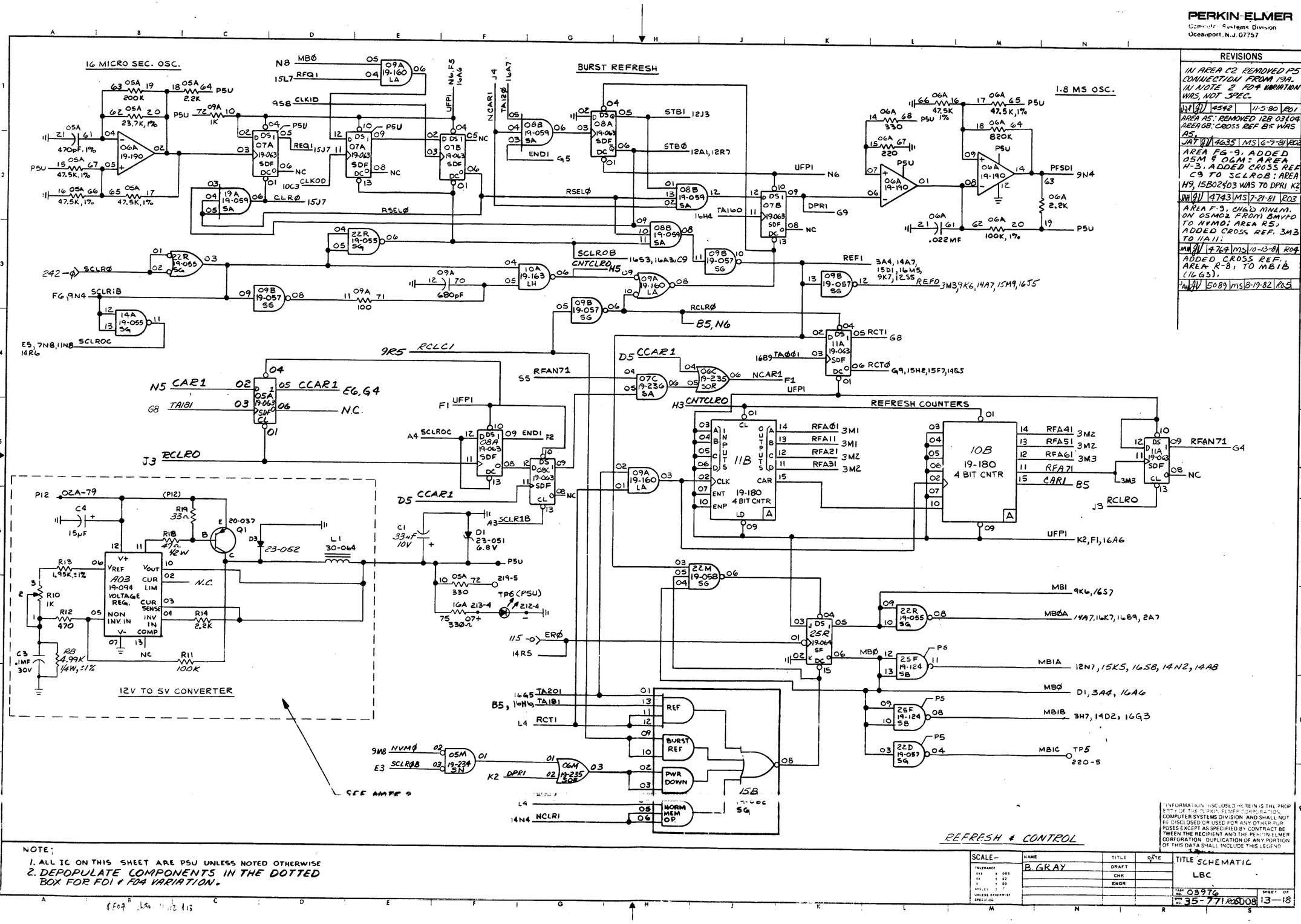
NOTES:
1. REMOVE JUMPER 22Z-5 TO 22Z-5 TO FORCE CACHE MISSES.
2. DEPOPULATE IC'S MARKED WITH AN ASTERISK FOR F02 & F04 VARIATION.

SCALE—
NAME
TITLE
DRAFT
CHK
ENGR
DATE

TITLE SCHEMATIC
LBC
TAG 03976
SIZE D 7771 R04
SHEET 12 OF 18

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS					
IN AREA C2 REMOVED P5 CONNECTION FROM 19A. IN NOTE 2 FD4 VARIATION WAS, NOT SPEC.					
JAT	GV	4542		11-5-80	R01
AREA A5: REMOVED 12B 03&04. AREA G8: CROSS REF B5 WAS A5.					
JAT	GV	4635	MS	6-9-81	R02
AREA F6-9, ADDED OSM & OLM: AREA H-3, ADDED CROSS REF C9 TO SCLR08: AREA H9, 15B02&03 WAS TO DPRI K2					
JAH	GV	4743	MS	7-21-81	R03
AREA F-9, CHGD MNEM. ON OSM02 FROM SMYF0 TO NYM0; AREA R5, ADDED CROSS REF. 3M3 TO 11A11:					
MH	GV	4764	MS	10-13-81	R04
ADDED CROSS REF. AREA R-8, TO MB1B (16G3).					
JAH	GV	5089	MS	8-19-82	R05

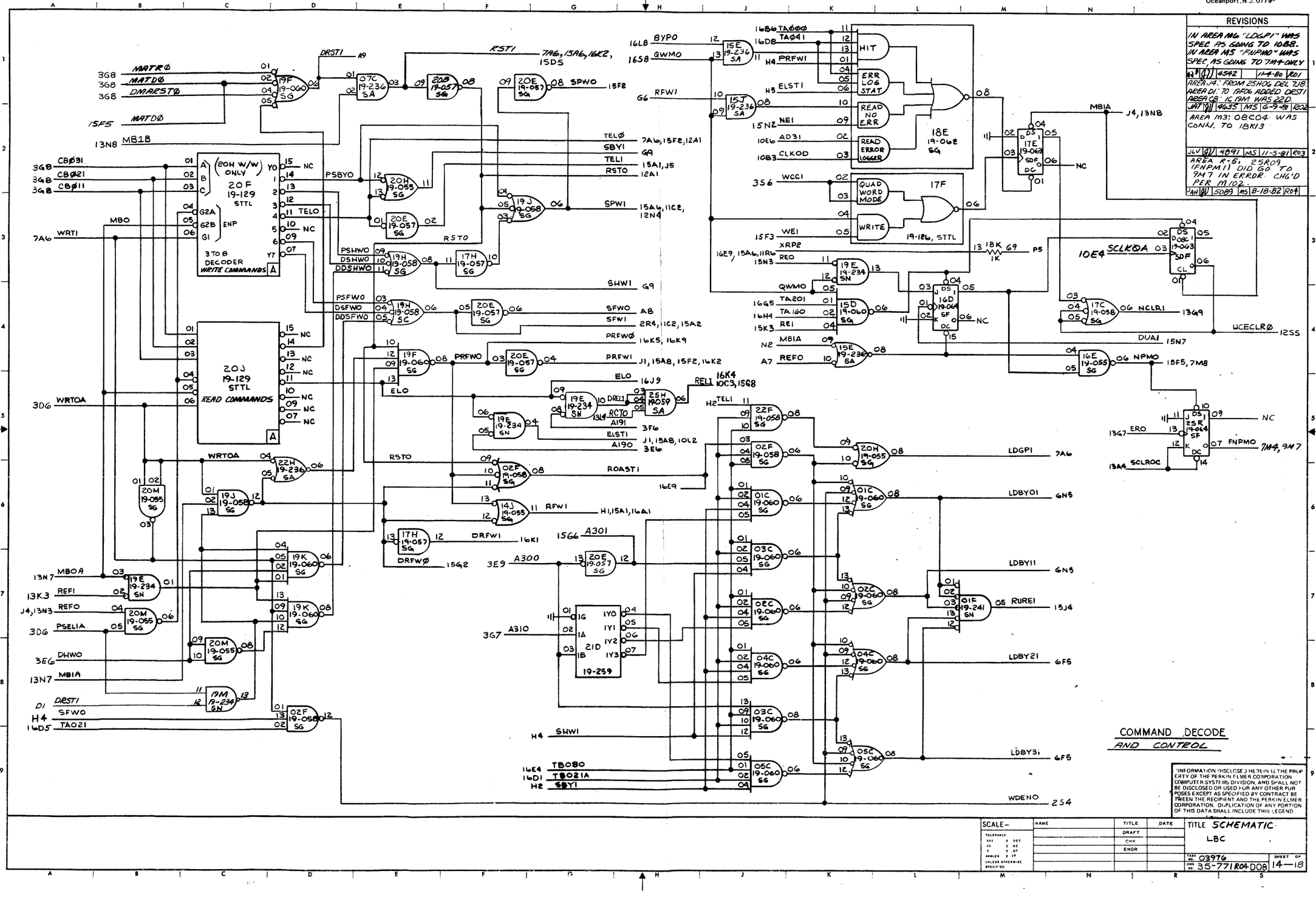


SCALE–	NAME	TITLE	DATE
TOLERANCE XX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	B. GRAY	DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC
LBC
TASK NO. 03976
SYS NO. 35-771 R05D08
SHEET OF 13–18

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
IN AREA M6 "LDGP1" WAS SPEC AS GOING TO 10BB. IN AREA M5 "FNPMO" WAS SPEC AS GOING TO 7M4 ONLY				
JAT	4542		11-4-80	R01
AREA I4: FROM 25H06 DEL 7J8. AREA D1: TO 3A06 ADDED DEST1 AREA C8: IC 15M WAS 22D				
JAT	4635	MS	12-9-81	R02
AREA M3: 08C04 WAS CONN. TO 18K13				
JLV	4891	MS	11-5-81	R03
AREA R-5, 25R09 (FNPM1) DID GO TO 7M7 IN ERROR. CHG'D PER M102.				
JAH	5089	MS	8-18-82	R04

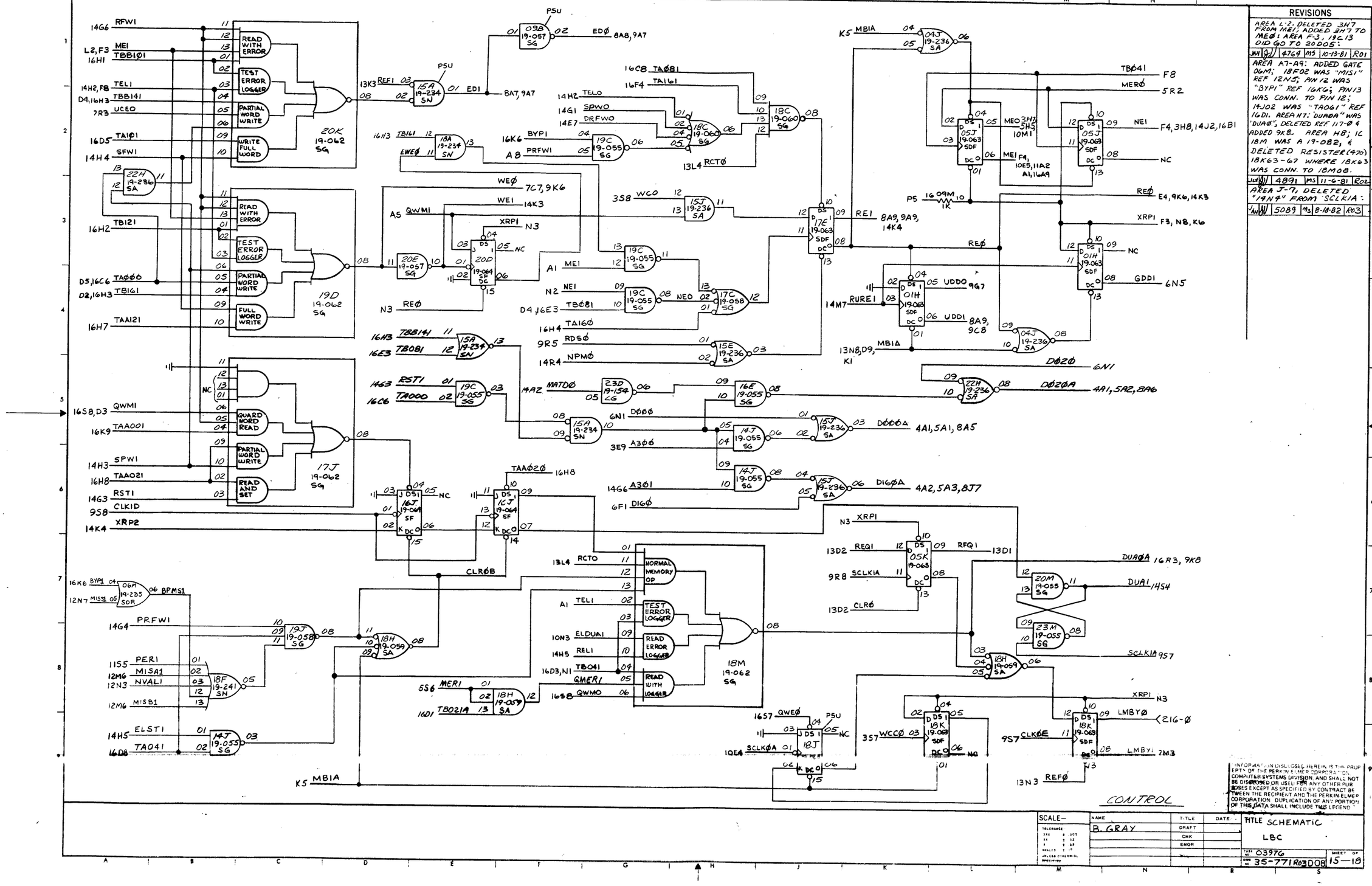


SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .07, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC
LBC
TASK NO. 03976
DWG NO. 35-771R04-D08
SHEET OF 14–18

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
AREA L-2; DELETED 3H7 FROM MEI; ADDED 2H7 TO MEØ; AREA F-3, 19C13 DID GO TO 20005:				
JWH	4769	MS	10-13-81	R01
AREA A7-A9: ADDED GATE 06M; 18F02 WAS "MISI" REF 12N5; PIN 12 WAS "BYPI" REF 16K6; PIN 13 WAS CONN. TO PIN 12; 14J02 WAS "TA06I" REF 16D1. AREA N7: "DUAØA" WAS "DUAØ", DELETED REF 11-7-0 & ADDED 9K8. AREA H8; IC 18M WAS A 19-082, & DELETED RESISTER (470) 18K63-67 WHERE 18K63 WAS CONN. TO 18M08.				
JWH	4891	MS	11-6-81	R02
AREA J-7, DELETED "19N9" FROM "SCLKIA":				
JWH	5089	MS	8-18-82	R03



	NAME	TITLE	DATE
SCALE—	B. GRAY	DRAFT	
TOLERANCE		CHK	
		ENGR	

HTLE SCHEMATIC
LBC

TASK NO 03976
DRWG NO 35-771R03D08
SHEET OF 15—18

PERKIN-ELMER
Computer Systems Division
Oceanport N.J. 07757

REVISIONS				
IN AREA D4 17A WAS NOT SPEC. 13A-12 WAS SPEC AS TA06J. IN AREA D1 ON TB021 CROSS REF 10A8 WAS NOT SPEC. IN AREA F4 ON TB080 CROSS REF 10A8 WAS NOT SPEC. IN AREA A6-TA06J1A" WAS SPEC AS"TA06J"				
JWP	JU	4542		11-4-80	R01
AREA H-3; ADDED CROSS REF SH7 TO TB191:				
JAH	JU	4764	MS	10-13-81	R02
AREA R3 "DUA0A" WAS "DUA0". AREA D8; ADDED REF 15A9 TO "TA041". AREA K6; REF 15A2 WAS 15A9. AREA R4; DELETED REF 9K8 TO "EA0". AREA R5; 18J07 WAS NC.				
JW	JU	4891	MS	11-6-81	R03
AREA D2, F2, D6 & F6, IC'S 17B, 18B, 13A & 13B WERE 19-249 F02. ADDED NOTE 2.				
KR	JU	4900	JC	11-20-81	R04
AREA K3, ADDED "05A". 18D 09 DID GO TO PRFW1 & 18D05 & 17D10				
AH	JU	5089	MS	8-18-82	R05

NOTES:
1. REMOVE STRAP FROM 217-5 (TP8) TO 218-5 (TP7) TO BYPASS CACHE.
2. IC PIN NUMBERS SHOWN IN PARENTHESIS REPRESENT ALTERNATE USE OF 19-249 F02.

TIMER & CONTROL

SCALE	NAME	TITLE	DATE
TOLERANCE XXX ± .005" .XX ± .02 .X ± .03 UNLESS OTHERWISE SPECIFIED	B. GRAY	DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC
LBC
PART NO 03976
DWG NO 35-771R05008
SHEET OF 16—18

CROSS REFERENCE NET#, MNEMONIC, SHEET#

NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.
0001	A080	3	0063	D090	11	0125			0187	ELMA31	3	0249	LMB111	8	0311	MDSI50	2	0373	RDO21	3	0435	TA161	16	0497	07J05	4	0559	05E06	7	0621	22E02	12	0683	20M08	14
0002	A090	3	0064	D100	11	0126	EB000	6	0188	FNPMO	14	0250	LMB121	8	0312	MDSI60	2	0374	RDO31	3	0436	TA181	16	0498	07K06	4	0560	05E08	7	0622	25A05	12	0684	22H06	14
0003	A100	3	0065	D110	11	0127	EB010	6	0189			0251	LMB131	8	0313	MDS170	2	0375	RDSO	9	0437	TA201	16	0499	07K05	4	0561	05E11	7	0623	25A07	12	0685	20J14	14
0004	A110	3	0066	D120	11	0128	EB020	6	0190	TP9	3	0252	LMB141	8	0314	MDS180	2	0376	RDSI	9	0438	TB001	16	0500	08J06	4	0562	06E03	7	0624	25A09	12	0686	17H10	14
0005	A120	3	0067	D130	11	0129	EB030	6	0191	LD01	10	0253	LMB151	8	0315	MDS190	2	0377	REO	15	0439	TB021	16	0501	08J05	4	0563	06E06	7	0625	25A11	12	0687	21D04	14
0006	A130	3	0068	D140	11	0130	EB040	6	0192	LD02	10	0254	LMB161	8	0316	MDS200	2	0378	REI	15	0440	TB041	16	0502	08K06	4	0564	06E08	7	0626	24A05	12	0688	21D05	14
0007	A140	3	0069	D150	11	0131	EB050	6	0193	LDBY01	14	0255	LMB171	8	0317	MDS210	2	0379	REFO	13	0441	TB061	16	0503	08K05	4	0565	08D05	7	0627	24A07	12	0689	21D06	14
0008	A150	3	0070	D160	11	0132	EB060	6	0194	LDBY11	14	0256	LMB181	8	0318	MDS220	2	0380	REFOA	13	0442	TB081	16	0504	09J06	4	0566	08D06	7	0628	24A09	12	0690	21D07	14
0009	A160	3	0071	D170	11	0133	EB070	6	0195	LDBY21	14	0257	LMB191	8	0319	MDS230	2	0381	REFI	13	0443	TB101	16	0505	09J05	4	0567	10D05	7	0629	24A11	12	0691	16D05	14
0010	A170	3	0072	D180	11	0134	EB080	6	0196	LDBY31	14	0258	LMB201	8	0320	MDS240	2	0382	RELI	14	0444	TB121	16	0506	09K06	4	0568	10D06	7	0630	23A05	12	0692	22F08	14
0011	A180	3	0073	D190	11	0135	EB090	6	0197	LDGPI	14	0259	LMB211	8	0321	MDS250	2	0383	REQI	13	0445	TB141	16	0507	09K05	4	0569	12D05	7	0631	23A07	12	0693	02F06	14
0012	A190	3	0074	D200	11	0136	EB100	6	0198	LDODI	16	0260	LMB221	8	0322	MDS260	2	0384	RFA01	13	0446	TB161	16	0508	10J06	4	0570	12D06	7	0632	23A09	12	0694	01C06	14
0013	A200	3	0075	D210	11	0137	EB110	6	0199	LMBY0	15	0261	LMB231	8	0323	MDS270	2	0385	RFA11	13	0447	TB080	16	0509	10J05	4	0571	06D05	7	0633	23A11	12	0695	03C06	14
0014	A210	3	0076	D220	11	0138			0200	LMBY1	15	0262	LMB241	9	0324	MDS280	2	0386	RFA21	13	0448	TAA020	16	0510	10K06	4	0572	06D06	7	0634	22A05	12	0696	02C06	14
0015	A220	3	0077	D230	11	0139	EB120	6	0201	LOE1	16	0263	LMB251	9	0325	MDS290	2	0387	RFA31	13	0449	TAA001	16	0511	10K05	4	0573	05H01	7	0635	22A07	12	0697	04C06	14
0016	A230	3	0078	D240	11	0140	EB130	6	0202	GP000	7	0264	LMB261	9	0326	MDS300	2	0388	RFA41	13	0450	TAA121	16	0512	11J06	5	0574	03J03	7	0636	25M04	12	0698	03C08	14
0017	A240	3	0079	D250	11	0141	EB140	6	0203	GP010	7	0265	LMB271	9	0327	MDS310	2	0389	RFA51	13	0451	TBB040	16	0513	11J05	5	0575	03F08	7	0637	25M07	12	0699	19C06	15
0018	A250	3	0080	D260	11	0142	EB150	6	0204	GP020	7	0266	LMB281	9	0328	MREO	9	0390	RFA61	13	0452	TBB101	16	0514	11K06	5	0576	13D09	7	0638	24M04	12	0700	18C06	15
0019	A260	3	0081	D270	11	0143	EB160	6	0205	GP030	7	0267	LMB291	9	0329	MREFO	9	0391	RFA71	13	0453	TBB141	16	0515	11K05	5	0577	16C02	7	0639	24M07	12	0701	15J11	15
0020	A270	3	0082	D280	11	0144	EB170	6	0206	GP040	7	0268	LMB301	9	0330	MWA001	9	0392	RFQ1	15	0454	TAA021	16	0516	12J06	5	0578	42X10	7	0640	24M09	12	0702	19C11	15
0021	A280	3	0083	D290	11	0145	EB180	6	0207	GP050	7	0269	LMB311	9	0331	MWA011	9	0393	RFWI	14	0455	TELO	14	0517	12J05	5	0579	16C07	7	0641	24M12	12	0703	17C12	15
0022	A290	3	0084	D300	11	0146	EB190	6	0208	GP060	7	0270	LMB321	9	0332	MWEO	9	0394	RDSTI	14	0456	TELI	14	0518	12K06	5	0580	42X07	7	0642	21C08	12	0704	15E03	15
0023	A300	3	0085	D310	11	0147	EB200	6	0209	GDDI	15	0271	LMB331	9	0333	MXO21	3	0395	RSELO	13	0457	UP000	9	0519	12K05	5	0581	16C10	7	0643	18F06	12	0705	18C08	15
0024	A310	3	0086	DO00A	15	0148	EB210	6	0210	GMERI	15	0272	LMB341	9	0334	MXO31	3	0396	RSTO	14	0458	UP010	9	0520	13J06	5	0582	42X04	7	0644	MISS1	12	0706	15A10	15
0025	A161	10	0087	DO20A	15	0149	EB220	6	0211	GMVFO	9	0273	LMB351	9	0335	NCEO	9	0397	RSTI	14	0459	UP020	9	0521	13J05	5	0583	42X00	7	0645	25D02	12	0707	14J06	15
0026	A171	10	0088	D160A	15	0150	EB230	6	0212	HITI	12	0274	LMB361	9	0336	NCLRI	14	0398	RUREI	14	0460	UP030	9	0522	13K06	5	0584	42X01	7	0646	25D04	12	0708	14J08	15
0027	A181	10	0089	DA00	5	0151	EB240	6	0213	LMA080	3	0275	LMB371	9	0337	NEO	15	0399	SO01	10	0461	UP040	9	0523	13K05	5	0585	15C03	7	0647	25D06	12	0709	05K08	15
0028	A191	3	0090	DA10	5	0152	EB250	6	0214	LMA090	3	0276	LMB381	9	0338	NEI	15	0400	SO11	10	0462	UP050	9	0524	03F02	5	0586	42X16	7	0648	25D08	12	0710	18J06	15
0029	A301	14	0091	DA20	5	0153	EB260	6	0215	LMA100	3	0277	MBO	13	0339	NPMO	14	0401	SO21	10	0463	UP060	9	0525			0587	09M14	7	0649	MISB1	12	0711	23M08	15
0030	AD01	10	0092	DA30	5	0154	EB270	6	0216	LMA110	3	0278	MBOA	13	0340	NBALI	12	0402	SO31	10	0464	UCEO	7	0526	11E03	6	0588	09K10	9	0650	MISA1	12	0712	18H06	15
0031	AD11	10	0093	DA40	5	0155	EB280	6	0217	LMA120	3	0279	MBI	13	0341	NVMO	9	0403	SO41	10	0465	UCEI	7	0527	11E06	6	0589	PSU		0651	25D10	12	0713	18K05	15
0032	AD21	10	0094	DB00	5	0156	EB290	6	0218	LMA130	3	0280	MBIA	13	0342	ODDI	16	0404	SO51	10	0466	UDDO	15	0528	11E08	6	0590	19M10	9	0652	25D12	12	0714	04J08	15
0033	AD31	10	0095	DB10	5	0157	EB300	6	0219	LMA140	3	0281	MBIB	13	0343	MATFO	14	0405	SO61	10	0467	UDDI	15	0529	11E11	6	0591	17H02	10	0653	24D02	12	0715	04J06	15
0034	BMCI0	9	0096	DB20	5	0158	EB310	6	0220	LMA150	3	0282	MBIC	13	0344	MATDO	14	0406	SDYI	14	0468	UFPI	16	0530	12E03	6	0592	15H06	10	0654	24D04	12	0716	17J08	15
0035	BMVFO	9	0097	DB30	5	0159	EPB000	7	0221	LMA160	3	0283	MCI0	16	0345	PSFWO	14	0407	SCLKI	9	0469	VALO	12	0531	12E06	6	0593	05K05	10	0655	24D06	12	0717	23D06	15
0036	BSCLRO	9	0098	DB40	5	0160	EPB010	7	0222			0284	MCCO	9	0346	PSHWO	14	0408	SCLKIA	9	0470	VALI	12	0532	12E08	6	0594	15E06	10	0656	24D08	12	0718	16E08	15
0037	BYPO	16	0099	DB50	5	0161	EPB020	7	0223	LMA170	3	0285	MEO	10	0347	POOO	4	0409	SCLKOA	10	0471	WA000	3	0533	12E11	6	0595	23M06	10	0657	24D10	12	0719	05C06	14
0038	BYPI	16	0100	DB60	5	0162	EPB030	7	0224	LMA180	3	0286	MEI	15	0348	PO10	4	0410	SCLRIB	13	0472	WA001	3	0534	13E03	6	0596	16H06	10	0658	24D12	12	0720	15E11	14
0039	CAENO	16	0101	DB70	5	0163	EPB040	7	0225	LMA190	3	0287	MEA000	9	0349	PO20	4	0411	SCLRO	13	0473	WA010	3	0535	13E06	6	0597	19M04	10	0659	23D02	12	0721	19E13	14
0040	CAENI	16	0102	DC00	5	0164	EPB050	7	0226	LMA200	3	0288	MEA010	9	0350	PO30	4	0412	SCLROB	13	0474	WA011	3	0536	13E08	6	0598	16H08	10	0660	23D04	12	0722	15J08	14
0041	CARI	13	0103	DC10	5	0165	EPB060	7	0227	LMA210	3	0289	MEA020	9	0351	PO40	5	0413	SCLROC	13	0475	WCO	3	0537	13E11	6	0599	17H04	10	0661	05A67	13	0723	15D06	14
0042	CAWEO	11	0104	DC20	5	0166	EAO	16	0228	LMA220	3	0290	MEA030	9	0352	PO50	5	0414	SFWO	14	0476	WCCO	3	0538	14E03	6	0600	18K12	10	0662	05A63	13	0724	15E08	14
0043	CBO11	3	0105	DC30	5	0167	EDO	15	0229	LMA230	3	0291	MERO	5	0353	PO60	5	0415	SFWI	14	0477	WCCI	3	0539	14E06	6	0601	23K03	11	0663	06A02	13	0725	16D06	14
0044	CB021	3	0106	DC40	5	0168	EDI	15	0230	LMA240	3	0292	MERI	5	0354	PERI	11	0416	SHIFTI	10	0478	WDENO	3	0540	14E08	6	0602	23K06	11	0664	09A06	13	0726	18E08	14
0045	CB031	3	0107	DC50	5	0169	ELO	14	0231	LMA250	3	0293	MISI	12	0355	PFSDO	9	0417	SHWI	14	0479	WEO	15	0541	14E11	6	0603	23K08	11	0665	07A09	13	0727	17F06	14
0046	CHI21	12	0108	DC60	5	0170	ELDUAO	10	0232	LMA260	3	0294	MRDSO	9	0356	PFSDI	13	0418	SPWO	14	0480	WEI	15	0542	07E03	6	0604	23K11	11	0666	09B08	13	0728	17E05	14
0047	CLKOD	10	0109	DC70	5	0171	ELDUAI	10	0233	LMA270	3	0295	MDS000	2	0357	PRFWO	14	0419	SPWI	14	0481	WRTO	3	0543	07E06	6	0605	23J03	11	0667	09A71	13	0729	22H05	14
0048	CLKIC	9	0110	DERRQ	5	0172	ELSTI	14	0234	LMA280	3	0296	MDS010	2	0358	PRFWI	14	0420	STBO	13	0482	WRTOA	3	0544	07E08	6	0606	23J06	11	0668	10A06	13	0730	18F05	15
0049	CLKID	9	0111	DHWO	3	0173	ENDI	13	0235	LMA290	3	0297	MDS020	2	0359	PSBYO	14	0421	STBI	13	0483	WRTI	14	0545	07E11	6	0607	23J08	11	0669	09A08	13	0731	14J03	15
0050	CLRO	13	0112	DMHWO	3	0174	ERO	13	0236	LMA300	3	0298	MDS030	2	0360	PSELI	14	0422	TA000	16	0484	XRPI	15	0546	08E03	6	0608	23J11	11	0670	08B12	13	0732	19J08	15
0051	CLROB	15	0113	DPRI	13	0175			0237	LMA310	8	0299	MDS040	2	0361	PSELIA	3	0423	TA080	16	0485	XRP2	16	0547	08E06	6	0609	23K01	11	0671	06A14	13	0733	16J06	15
0052	CLTBI	16	0114	DRELI	14	0176	ELA040	10	0238	LMB001	8	0300	MDS050	2	0362	QWEO	16	0424	TA120	16	0486	21R19	9	0548	08E08	6	0610	22J06	11	0672	06A01	13	0734	20K08	15
0053	CPERI	16	0115	DRFWO	14	0177	ELA050	10	0239	LMB011	8	0301	MDS060	2	0363	QWMO	16	0425			0487	03J06	2	0549	08E11	6	0611	24J06	11	0673	06A14	13	0735	16J07	15
0054	DOOO	11	0116	DRFWI	14	0178	ELA060	10	0240	LMB021	8	0302	MDS070	2	0364	QWMI	16	0426	TA160	16	0488	18R03	3	0550	09E03	6	0612	25J06	11	0674	11B15	13	0736	16J09	15
0055	DO10	11	0117	DDSFWO	14	0179	ELA070	10	0241	LMB031	8	0303			0365	RCARO	10	0427	TA001	16	0489	18R06	3	0551	09E06	6	0613	12A07	11	0675	09A03	13	0737	19C03	15
0056	DO20	11	0118	DDSHWO	14	0180	ELA080	10	0242	LMB041	8	0304	MDS080	2	0366	RCLCO	9	0428	TA021	16	0490	23F08	3	0552	09E08	6	0614	42X19	11	0676	22M06	13	0738	15A13	15
0057	DO30	11	0119	DUAO	15	0181	ELA090	10	0243	LMB051	8	0305	MDS090	2	0367	RCLCI	9	0429	TA041	16	0491	22H03	3	0553	09E11	6	0615	03J11	11	0677			0739	19A08	16
0058	DO40	11	0120	DUAI	15	0182	ELA100	10	0244	LMB061	8	0306	MDS100	2	0368	RCLRO	13	0430	TA061	16	0492	18R11	3	0554	10E03	6	0616	03J08	11	0678	15B08	13	0740	14A03	16
0059	DO50	11	0121	DSHWO	14	0183	ELA110	10	0245	LMB071	8	0307	SPWI10	2	0369	RCLRO	13	0431	TA101	16	0493	18R12	3	0555	10E06	6	0617	11A06	12	0679	08B06	13	0741	17C08	16
0060	DO60	11	0122	DSFWO	14	0184	ELMA01	3	0246	LMB081	8	0308	MDS120	2	0370	RCTO	13	0432	TA101	16	0494	25H08	3	0556	10E08	6	0618	22A02	12	0680	20M06	14	0742	15H08	16
0061	DO70	11	0123	20J14	14	0185	ELMA11	3	0247	LMB091	8	0309	MDS130	2	0371	RCTI	13	0433	TA121	16	0495	21E11	3	0557	10E11	6	0619	22B02	12	0681	19E01	14	0743	12B10	16
0062	DO80	11	0124	MARSTO	14	0186	ELMA21	3	0248	LMB101	8	0310	MDS140	2	0372	RDO11	3	0434	TA141	16	0496	07J06	4	0558	05E03	7	0620	22C02	12	0682	22D08	14	0744	16D07	16

NOTES

REVISIONS				
NET #189 WAS SPEC AS FNPMI SHT 14. NET #589 WAS SPEC AS 22D12 SHT 9.				
D.A.P.	4592		11-5-80	R01
DELETED EWEI (NET 175) SHT. 15;				
JAH	4764	MS	10-13-81	R02
NET 119 WAS DAO. NET 644 WAS 52X21. NET 649 WAS 21A19. NET 650 WAS 21B19.				
JLV	4891	MS	11-6-81	R03

UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME	TITLE	DATE
V. PERRI / E. JOHNSON	DES/DFT	4-24-80
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE

LBC

TASK 03976 | SHT

DWG 35-771 R03 D08 | 17-18

CROSS REFERENCE NET#, MNEMONIC, SHEET#

NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.
0745	16E03	16	0807	GND16J		0869			0931			0993			1055			1117			1179			1241			1303			1365			1427		
0746	14B11	16	0808	GND20D		0870			0932			0994			1056			1118			1180			1242			1304			1366			1428		
0747	14B08	16	0809	GND08A		0871			0933			0995			1057			1119			1181			1243			1305			1367			1429		
0748	19B08	16	0810	13C06	2	0872			0934			0996			1058			1120			1182			1244			1306			1368			1430		
0749	18A10	16	0811	GND10C		0873			0935			0997			1059			1121			1183			1245			1307			1369			1431		
0750	12C08	16	0812	06R08	7	0874			0936			0998			1060			1122			1184			1246			1308			1370			1432		
0751	12C06	16	0813	04J11	7	0875			0937			0999			1061			1123			1185			1247			1309			1371			1433		
0752	21F06	16	0814	TB02IA	15	0876			0938			1000			1062			1124			1186			1248			1310			1372			1434		
0753	23M11	16	0815	42X13	13	0877			0939			1001			1063			1125			1187			1249			1311			1373			1435		
0754	18K71	16	0816	52X19	13	0878			0940			1002			1064			1126			1188			1250			1312			1374			1436		
0755	16B08	16	0817			0879			0941			1003			1065			1127			1189			1251			1313			1375			1437		
0756	19M01	16	0818	MATRSR0	3	0880			0942			1004			1066			1128			1190			1252			1314			1376			1438		
0757	18D08	16	0819	MATRSD0	3	0881			0943			1005			1067			1129			1191			1253			1315			1377			1439		
0758	P5U09A		0820	DMARS0	3	0882			0944			1006			1068			1130			1192			1254			1316			1378			1440		
0759	P5U07A		0821	RDSD0	9	0883			0945			1007			1069			1131			1193			1255			1317			1379			1441		
0760	P5U07B		0822	CLK0E	9	0884			0946			1008			1070			1132			1194			1256			1318			1380			1442		
0761	P5U09B		0823	07C11	12	0885			0947			1009			1071			1133			1195			1257			1319			1381			1443		
0762			0824	UCECLR0	14	0886			0948			1010			1072			1134			1196			1258			1320			1382			1444		
0763	GND20R		0825	NCAR1	13	0887			0949			1011			1073			1135			1197			1259			1321			1383			1445		
0764	GND19R		0826	07C06	13	0888			0950			1012			1074			1136			1198			1260			1322			1384			1446		
0765	GND23F		0827	08C01	13	0889			0951			1013			1075			1137			1199			1261			1323			1385			1447		
0766	GND07K		0828	08A08	13	0890			0952			1014			1076			1138			1200			1262			1324			1386			1448		
0767	GND08K		0829	RFANT1	13	0891			0953			1015			1077			1139			1201			1263			1325			1387			1449		
0768	GND09K		0830	09R08	13	0892			0954			1016			1078			1140			1202			1264			1326			1388			1450		
0769	GND10K		0831	19F06	14	0893			0955			1017			1079			1141			1203			1265			1327			1389			1451		
0770	GND11K		0832	CCARE1	13	0894			0956			1018			1080			1142			1204			1266			1328			1390			1452		
0771	GND12K		0833	TA06IA	14	0895			0957			1019			1081			1143			1205			1267			1329			1391			1453		
0772	GND13K		0834	07M11	10	0896			0958			1020			1082			1144			1206			1268			1330			1392			1454		
0773	GND06D		0835	05M01	13	0897			0959			1021			1083			1145			1207			1269			1331			1393			1455		
0774	GND21R		0836	06M03	13	0898			0960			1022			1084			1146			1208			1270			1332			1394			1456		
0775	GND07M		0837	MERR1	3	0899			0961			1023			1085			1147			1209			1271			1333			1395			1457		
0776	GND15F		0838	EWE0	15	0900			0962			1024			1086			1148			1210			1272			1334			1396			1458		
0777	GND16F		0839	14CP5	3	0901			0963			1025			1087			1149			1211			1273			1335			1397			1459		
0778	GND05K		0840	14CGND	3	0902			0964			1026			1088			1150			1212			1274			1336			1398			1460		
0779	GND21K		0841	18A13	15	0903			0965			1027			1089			1151			1213			1275			1337			1399			1461		
0780	GND22K		0842	DUA0A	9	0904			0966			1028			1090			1152			1214			1276			1338			1400			1462		
0781	GND24K		0843	BPMS1	15	0905			0967			1029			1091			1153			1215			1277			1339			1401			1463		
0782	GND06J		0844	EA1	9	0906			0968			1030			1092			1154			1216			1278			1340			1402			1464		
0783	GND17J		0845	17B6ND	16	0907			0969			1031			1093			1155			1217			1279			1341			1403			1465		
0784	GND18J		0846	18B6ND	16	0908			0970			1032			1094			1156			1218			1280			1342			1404			1466		
0785	GND01H		0847	13A6ND	16	0909			0971			1033			1095			1157			1219			1281			1343			1405			1467		
0786	GND12H		0848	13B6ND	16	0910			0972			1034			1096			1158			1220			1282			1344			1406			1468		
0787	GND18D		0849			0911			0973			1035			1097			1159			1221			1283			1345			1407			1469		
0788	GND17D		0850			0912			0974			1036			1098			1160			1222			1284			1346			1408			1470		
0789	GND16B		0851			0913			0975			1037			1099			1161			1223			1285			1347			1409			1471		
0790	GND12A		0852			0914			0976			1038			1100			1162			1224			1286			1348			1410			1472		
0791	GND16D		0853			0915			0977			1039			1101			1163			1225			1287			1349			1411			1473		
0792	GND13D		0854			0916			0978			1040			1102			1164			1226			1288			1350			1412			1474		
0793	GND22A		0855			0917			0979			1041			1103			1165			1227			1289			1351			1413			1475		
0794	GND22B		0856			0918			0980			1042			1104			1166			1228			1290			1352			1414			1476		
0795	GND22C		0857			0919			0981			1043			1105			1167			1229			1291			1353			1415			1477		
0796	GND22E		0858			0920			0982			1044			1106			1168			1230			1292			1354			1416			1478		
0797	GND25K		0859			0921			0983			1045			1107			1169			1231			1293			1355			1417			1479		
0798	GND25R		0860			0922			0984			1046			1108			1170			1232			1294			1356			1418			1480		
0799	GND17E		0861			0923			0985			1047			1109			1171			1233			1295			1357			1419			1481		
0800	GND21D		0862			0924			0986			1048			1110			1172			1234			1296			1358			1420			1482		
0801	GND21A		0863			0925			0987			1049			1111			1173			1235			1297			1359			1421			1483		
0802	GND21B		0864			0926			0988			1050			1112			1174			1236			1298			1360			1422			1484		
0803			0865			0927			0989			1051			1113			1175			1237			1299			1361			1423			1485		
0804	GND24M		0866			0928			0990			1052			1114			1176			1238			1300			1362			1424			1486		
0805	GND25M		0867			0929			0991			1053			1115			1177			1239			1301			1363			1425			1487		
0806	GND26R		0868			0930			0992			1054			1116			1178			1240			1302			1364			1426			1488		

NOTES

REVISIONS

NETS #833 & 834 WERE NOT SPEC.					
V.P.	JV	4542		11-5-80	R01
ADDED NETS 835 & 836:					
JAH	JV	4743	MS	7-21-81	R02
ADDED NEW NETS 836-841					
JAH	JV	4764	MS	10-13-81	R03
ADDED NEW NETS 842-844.					
JLV	JV	4891	MS	11-6-81	R04
ADDED NEW NETS 845-848.					
KR	JV	4900	R	11-20-81	R05

UNLESS OTHERWISE SPECIFIED

SCALE: NONE

TOLERANCE:

DIMENSIONS ARE IN INCHES

.XXX ±.005 .X ±.03
.XX ±.02 ANGLES ±1°

NAME DES/DFT		TITLE	DATE
V. PERRI	B. LUSK	DES/DFT	4-22-80
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

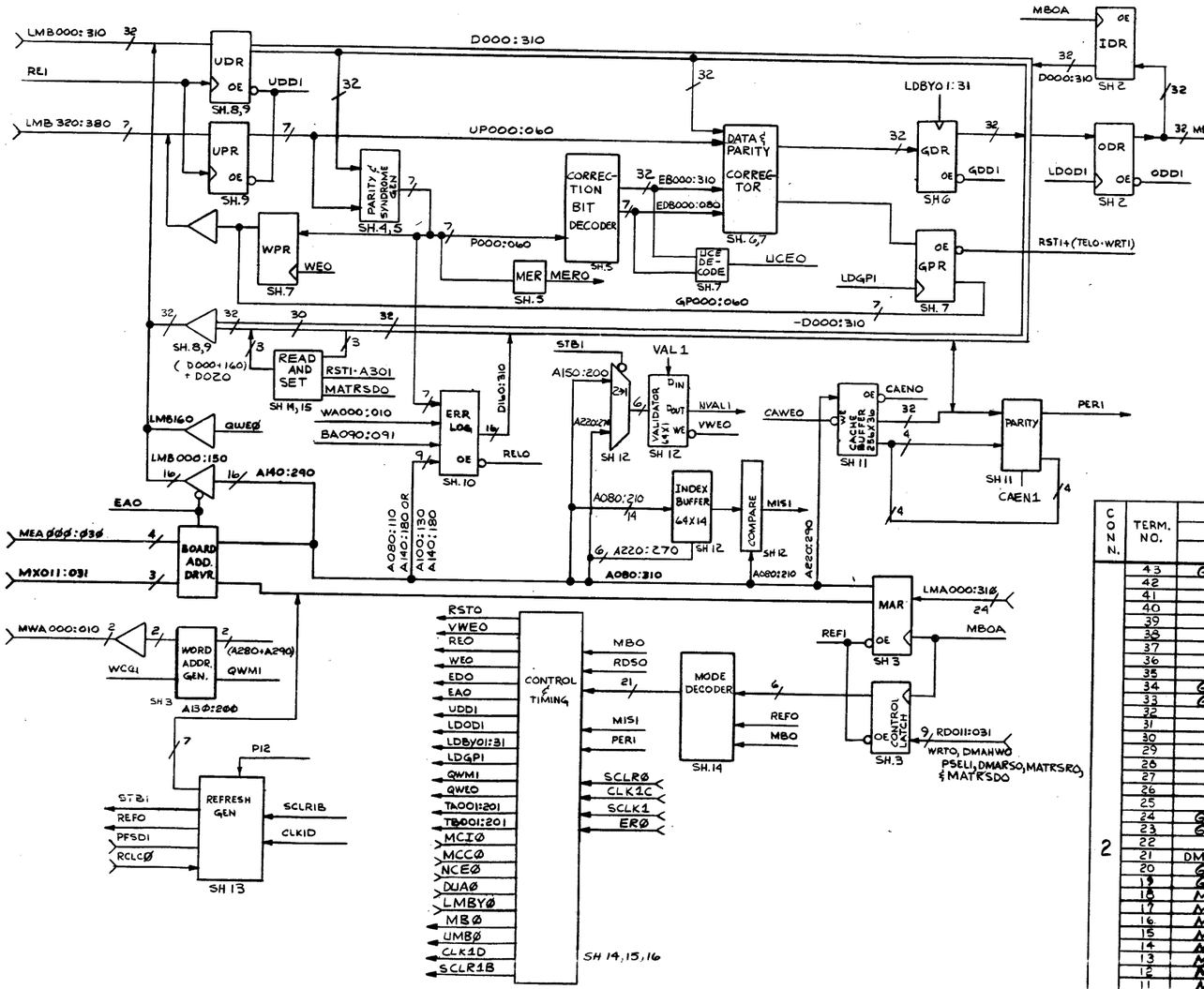
Computer Systems Division
Oceanport, N.J. 07757

TITLE

LBC

TASK 03976 SHT

DWG 35-771 R05 D08 18-18



TEST POINTS

#	MNEMONIC	SHT.
TP1	GND	5
TP2	DERRO	5
TP3	GND	12
TP4	TP4	12
TP5	MBIC	13
TP6	TP6	13
TP7	GND	16
TP8	BYP1	16
TP9	TP9	3
TP10	GND	3
TP11	DERO8	7
TP12	GND	7

TEST POINTS (CONT)

#	MNEMONIC	SHT
TP13	CSTRIN00	13
TP14	CSTRIN10	13
TP15	RPCTLD0	13
TP16	TAST0	16
TPA	PFSD1	13
TPB	PFSDIR	13
TPC	TGA211	12
TPD	TGA201	12
TPE	TGA191	12
TPF	TGA181	12
TPG	TGA171	12
TPH	TGA161	12
TPJ	TGA151	12
TPJ	TGA141	12
TPK	TGA131	12
TPL	TGA121	12
TPM	TGA111	12
TPN	TGA101	12
TPO	TGA091	12
TPP	TGA081	12

BACK PANEL MAP

CONN.	TERM. NO.	ROW 1	ROW 2	ROW 1	ROW 2	TERM. NO.	CONN.
	43	GND	GND	GND	GND	43	
	42				SCLR0	42	
	41					41	
	40					40	
	39					39	
	38					38	
	37					37	
	36			GND	GND	36	
	35					35	
	34	GND	GND	GND	GND	34	
	33	GND	GND	GND	GND	33	
	32					32	
	31					31	
	30					30	
	29					29	
	28					28	
	27					27	
	26					26	
	25					25	
	24	GND	GND	GND	GND	24	
	23	GND	GND	GND	GND	23	
	22		MATRSDØ	NVMØ		22	
	21	DMARSØ	MATRSRØ	CLK1C	SCLK1	21	
	20	GND	GND	GND	GND	20	
	19	GND	GND	GND	GND	19	
	18	MDS30Ø	MDS31Ø	NCEØ	GMVFØ	18	
	17	MDS28Ø	MDS29Ø	DUAØ	PSELI	17	
	16	MDS26Ø	MDS27Ø	DMAHWØ	LMBYØ	16	
	15	MDS24Ø	MDS25Ø	ERØ	WRTØ	15	
	14	MDS22Ø	MDS23Ø	LMA30Ø	LMA31Ø	14	
	13	MDS20Ø	MDS21Ø	LMA28Ø	LMA29Ø	13	
	12	MDS18Ø	MDS19Ø	LMA26Ø	LMA27Ø	12	
	11	MDS16Ø	MDS17Ø	LMA24Ø	LMA25Ø	11	
	10	GND	GND	GND	GND	10	
	09	GND	GND	GND	GND	09	
	08	MDS14Ø	MDS15Ø	LMA22Ø	LMA23Ø	08	
	07	MDS12Ø	MDS13Ø	LMA20Ø	LMA21Ø	07	
	06	MDS10Ø	MDS11Ø	LMA18Ø	LMA19Ø	06	
	05	MDS08Ø	MDS09Ø	LMA16Ø	LMA17Ø	05	
	04	MDS06Ø	MDS07Ø	LMA14Ø	LMA15Ø	04	
	03	MDS04Ø	MDS05Ø	LMA12Ø	LMA13Ø	03	
	02	MDS02Ø	MDS03Ø	LMA10Ø	LMA11Ø	02	
	01	MDS00Ø	MDS01Ø	LMA08Ø	LMA09Ø	01	
	00	GND	GND	GND	GND	00	

FUNCTIONAL VARIATION TABLE

F02	35-806 R05	F02	W/O CACHE	AS SHOWN ON SHT'S 2,11,12
F01	35-806 R05	F01	W/CACHE	AS SHOWN ON SHT'S 2,11,12

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REV LEVEL.

USED IN MANUAL 47-022

REVISIONS	5	4	1	0	0	0	0	0	2	1	0	1	2	1	2	3	2	5
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

NOTE - SEE SHT 2 FOR TABLE OF SPARES.

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

PRE PRODUCTION APPROVAL	DEV	INIT	DATE

SHT 2,3,9,13,15,17,18 WERE SPEC. AS REV R00. REV LEVEL OF BOARDS IN VARIATION TABLE WERE R00.

RS | WB | 4763 | 8-18-81 | R01

RELEASED FOR PRODUCTION
ENG. | DATE

REVISED SHTS 1, 2 & 18
JW | 4855 | R | 11-11-81 | R02

REVISED SHTS 1, 16, 18.
KB | 4900 | R | 12-2-81 | R03
AREA K9 47-022 WAS 47-004. AREA E9 35-806 F01 & F02 WERE R02. REVISED SHTS 1, 2, 9, 12, 14, 15, 16, 17 & 18
KB | 4909 | R | 1-19-82 | R04

REV'D SHTS 1, 2, 10, 13, 16 & 18 · 35-806 F01 & F02 WERE R03.
SDB9 | ms | 8-20-82 | R05

(207-6) A	(206-6) B	13
(216-5) TP9	(215-5) TP10	3
FROM	TO	SHT LOC.
STRAPPING, INFO		

SCALE —	E GREENSTEIN	TEST	
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	D STINE	DRAFT	12-10-80
	R. CERO	CHK	9-11-81
	M. MANGIONE	ENGR	9-11-81
	R. BARKER	QC	9-11-81
	ROBADA	MGR.	9-11-81

TITLE SCHEMATIC
LOCAL BANK CONTROLLER (BMB CAPABILITY)
TASK no. 03183
DWG no. 35-806RC5 D08
SHEET OF 1 — 18

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
TABLE OF SPARES; 01M WAS NOT SPEC., 18A-13, A 19-236 WAS DELETED, 17F-08 A 19-126 WAS DELETED, 06C SPARE OUTPUT 03,08 WERE DELETED.				
MS	WAP	4743	8-18-81	R01
DELETED 10A, 08 & 11 FROM SPARE GATES TABLE				
JW	AP	4855	R VI-11-81	R02
DELETED 06C11, 19-235 FROM SPARE GATE LIST.				
KA	AP	14909	MS 1-19-82	203
DELETED 05A 8/9, 19-063 FROM SPARE LIST.				
JW	AP	5089	MS 8-20-82	R04

PROCESSOR DATA BUS

01K 19-232 ODR

00K 19-232 OCT F/F

03K 19-232 OCT F/F

04K 19-232 OCT F/F

ODD1 16N4
LDD01 16K9

OUTPUT DATA REGISTER

02R 21-025 R01 15 PIN DIP 1K TO COM.

13C 19-126 SG

03J 19-236 SA

TA061 16D5
SFW1 14H4
TA101 16D5
WDENO 14M9
MDS160 10N5

MDS000 101-2
MDS010 201-2
MDS020 102-2
MDS030 202-2
MDS040 103-2
MDS050 203-2
MDS060 104-2
MDS070 204-2
MDS080 105-2
MDS090 205-2
MDS100 106-2
MDS110 206-2
MDS120 107-2
MDS130 207-2
MDS140 108-2
MDS150 208-2
MDS160 111-2
MDS170 211-2
MDS180 112-2
MDS190 212-2
MDS200 113-2
MDS210 213-2
MDS220 114-2
MDS230 214-2
MDS240 115-2
MDS250 215-2
MDS260 116-2
MDS270 216-2
MDS280 117-2
MDS290 217-2
MDS300 118-2
MDS310 218-2
MB0A 13N7

05R 21-025 R01 15 PIN DIP 1K TO COM.

F9 D150 17 00K 1K 6S P5
J9 D230 16 00K 1K 6G P5

INPUT DATA REGISTER

01R 19-232 OCT F/F

00R 19-232 OCT F/F

07R 19-232 OCT F/F

08R 19-232 OCT F/F

INPUT OUTPUT DATA REGISTER

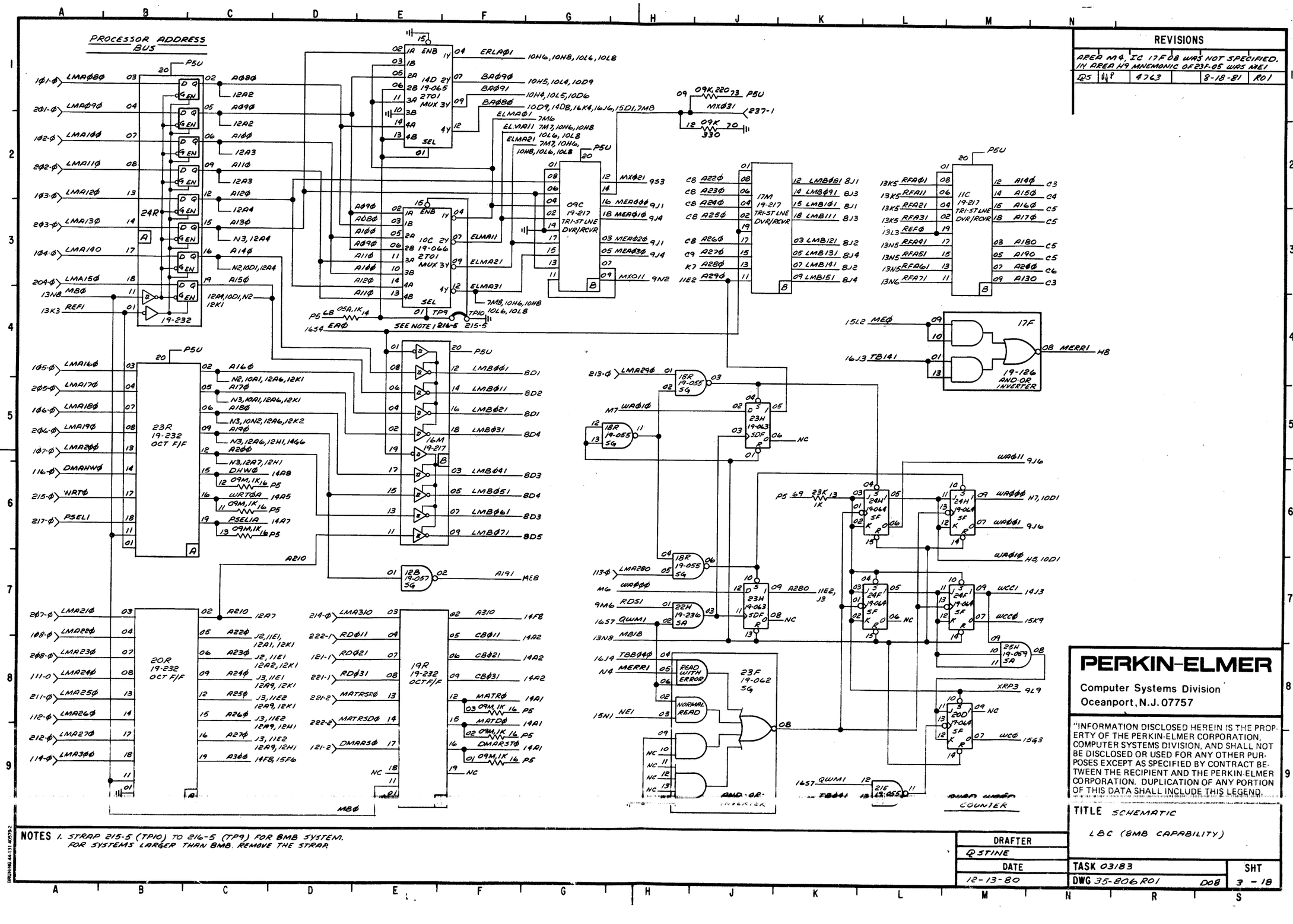
25F	19-124	03,06
23M	19-055	06
23D	19-154	08,10,12
22D	19-057	06,08,10,12
20H	19-055	06
20B	19-057	06,10,12
20A	19-057	06
19M	19-234	10,
19H	19-058	12
19A	19-059	12
17A	19-236	11
01M	19-234	04,10,13
15C	19-131	7/16, 10/11, 15/14
12R	19-163	06,08,11
10A	19-163	03
09R	19-055	08,11
12B	19-057	04
09A	19-160	11
06A	19-190	13
05H	19-234	04,10,13
05F	19-234	13
05E	19-127	11
03F	19-057	04,10,12
02M	19-063	8/9
17H	19-057	04
01F	19-241	06
REF. DESIGN.	PART NUMBER	SPARE OUTPUTS

TABLE OF SPARES

NOTES 1. DEPOPULATE ICS & DISCRETES MARKED WITH AN ASTERISK (*) FOR F01 VARIATION.

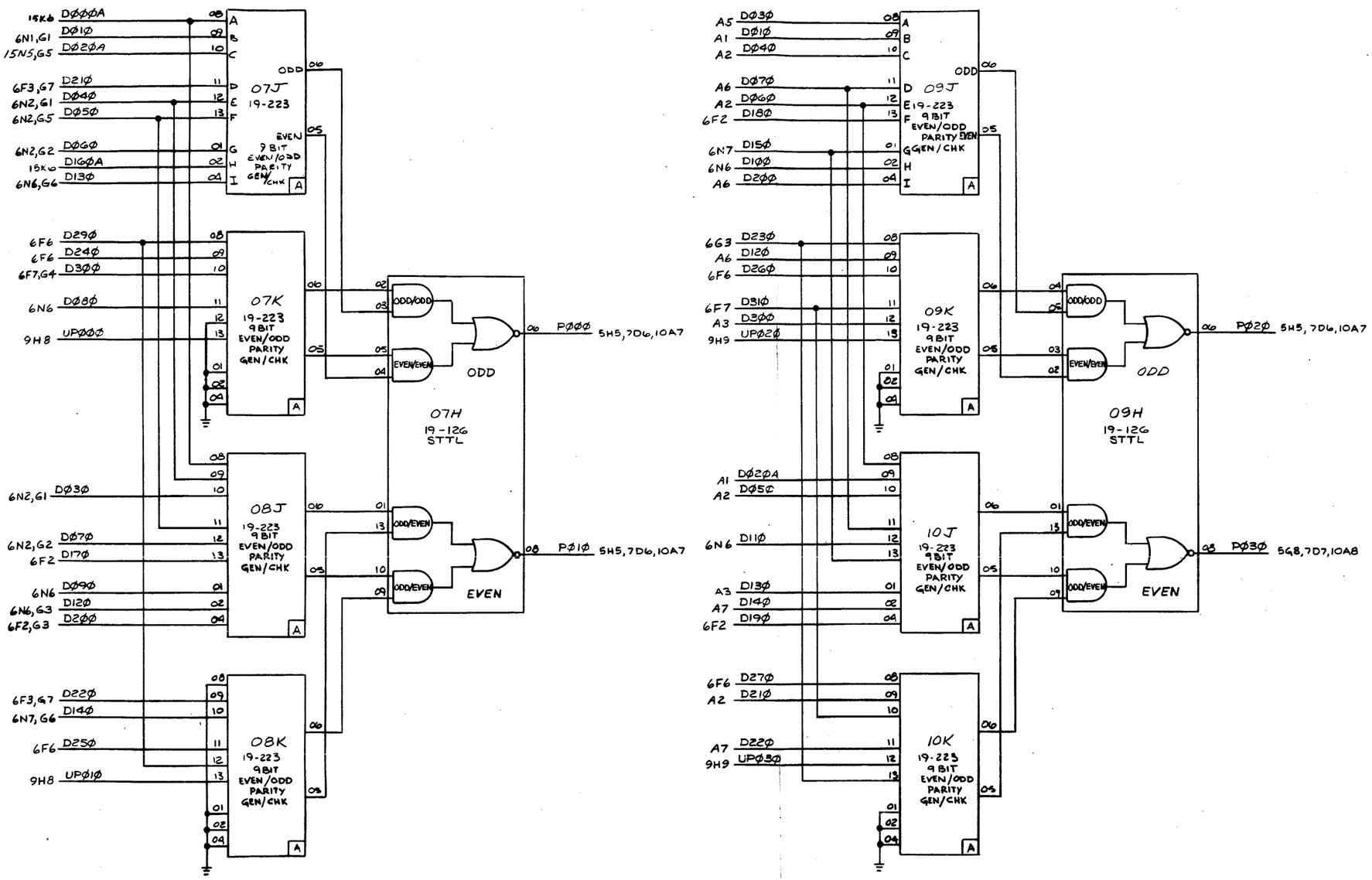
	NAME	TITLE	DATE
SCALE–	QSTINE	DRAFT	12-10-80
TOLERANCE XX ± .005, X ± .01, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		CHK	
		ENGR	

TITLE SCHEMATIC
LBC
8MB CAPABILITY
TASK NO. 03183
SYS NO. 35-806 P04 D08
SHEET OF 2–18


PROCESSOR ADDRESS BUS
REVISIONS
AREA M4, IC 17F08 WAS NOT SPECIFIED. IN AREA H9 MNEMONIC OF 23F-05 WAS ME1
ID5 | W8 | 4763 | | 8-18-81 | R01
24R
19-232
A
23R
19-232
OCT F/F
20R
19-232
OCT F/F
19R
19-232
OCT F/F/F
09C
19-217
TRI-ST LINE DVR/RCVR
17M
19-217
TRI-ST LINE DVR/RCVR
11C
19-217
TRI-ST LINE DVR/RCVR
14D 2Y
19-065
2 TO 1 MUX 3Y
10C 2Y
19-066
2 TO 1 MUX 3Y
16M
19-217
17F
19-126
AND-OR INVERTER
23F
19-062
SG
AND-OR-INVERTER
23H
19-063
SDF
24H
19-064
SF
24F
19-064
SF
20D
19-064
SF
25H
19-059
SA
18R
19-055
SG
22H
19-236
SA
12B
19-057
SG
21F
19-455
COUNTER
PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757
"INFORMATION DISCLOSED HEREIN IS THE PROPERTY OF THE PERKIN-ELMER CORPORATION, COMPUTER SYSTEMS DIVISION, AND SHALL NOT BE DISCLOSED OR USED FOR ANY OTHER PURPOSES EXCEPT AS SPECIFIED BY CONTRACT BETWEEN THE RECIPIENT AND THE PERKIN-ELMER CORPORATION. DUPLICATION OF ANY PORTION OF THIS DATA SHALL INCLUDE THIS LEGEND.
NOTES 1. STRAP 215-5 (TP10) TO 216-5 (TP9) FOR 8MB SYSTEM. FOR SYSTEMS LARGER THAN 8MB, REMOVE THE STRAP.
DRAFTER Q STINE
DATE 12-13-80
TITLE SCHEMATIC
LBC (8MB CAPABILITY)
TASK 03183
DWG 35-806 R01
D08
SHT 3 - 18
BRUNING 44-131 40579-2

PERKIN-ELMER
Computer Systems Division
Oceanport, N J. 07757

REVISIONS



PARITY GENERATOR

SCALE –	NAME	TITLE	DATE
	RSTINE	DRAFT	
		CHK	
		ENGR	

TITLE : SCHEMATIC
LBC (BMB CAPABILITY)

DWG NO 03183
REV 3F-806 D08
SHEET 4 OF 18

DRAWING 44-231 24538

PERKIN-ELMER
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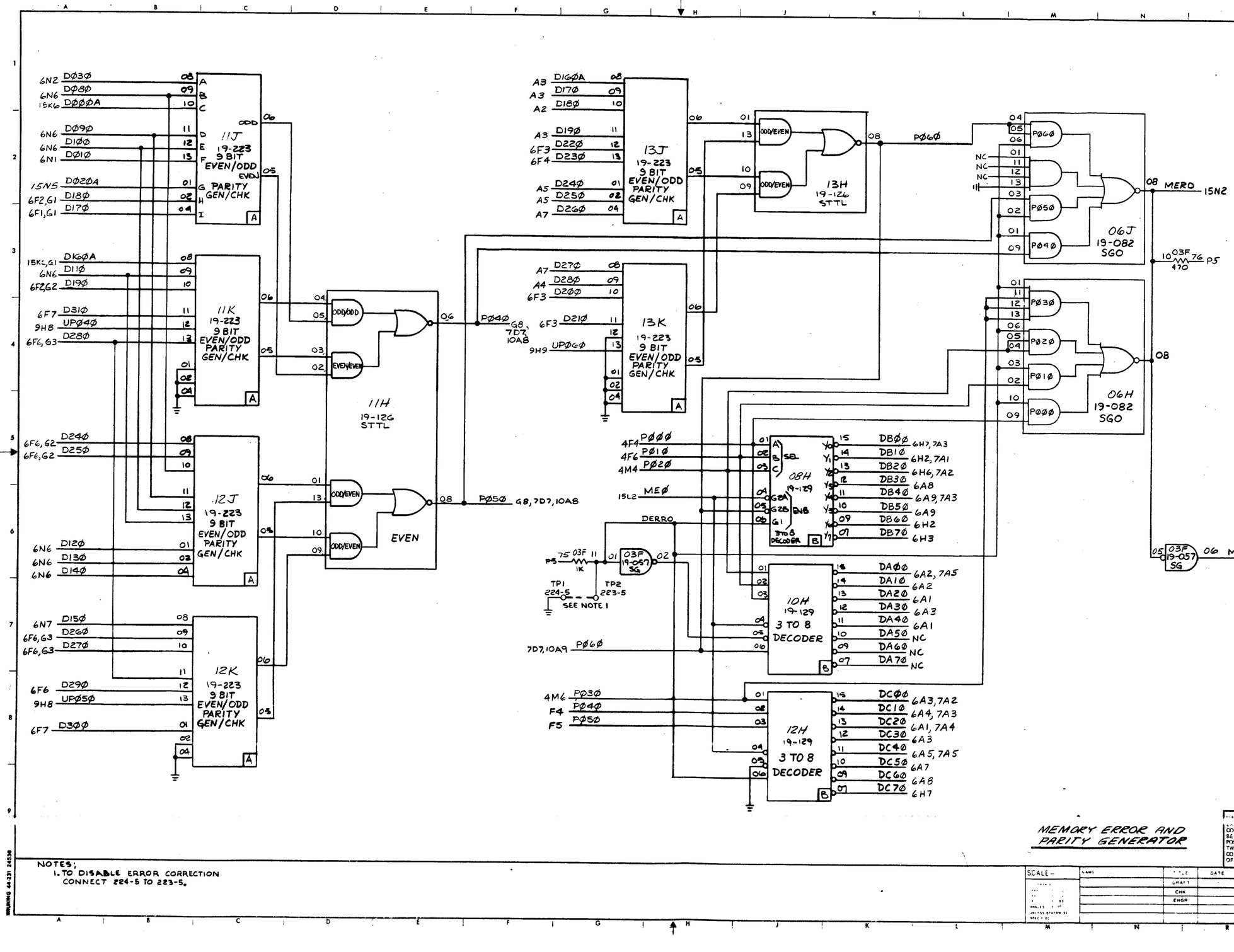
REVISIONS



NOTES;
1. TO DISABLE ERROR CORRECTION CONNECT 224-5 TO 223-5.

MEMORY ERROR AND PARITY GENERATOR

SCALE –
DRAWN
CHK
ENGR
DATE
TITLE: SCHEMATIC
LBC (8MB CAPABILITY)
TASK NO 03183
DWG NO 35 806 D08
SHEET OF 5 – 18

DRAWING 44-231 24538

PERKIN-ELMER
Computer ~~System~~ Division
Oceanport, N.J. 07757

REVISIONS

DATA LATCH

DATA LATCH

ERROR CORRECTOR

SCALE –

	NAME	TITLE	DATE
		DRAFT	
		CHK	
		ENGR	

TITLE: SCHEMATIC
LBC (8MB CAPABILITY)

TASK NO. 03183
DWG NO. 35-806 DOB
SHEET OF 6 — 18

PERKIN ELMER
Computer Systems Division
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REVISIONS

5K5 DB1Ø
5K8 DCØØ
9H8 UPØØØ
5K6 DB2Ø
9H8 UPØ1Ø
5K6 DB4Ø
9H9 UPØ2Ø
5K5 DBØØ
5K8 DC1Ø
9H9 UPØ3Ø
5K8 DC2Ø
9H8 UPØ4Ø
5K9 DC4Ø
9H8 UPØ5Ø
5K7 DAØØ
9H9 UPØ6Ø

05F 19-234 SN
06F 19-234 SN
05E 19-127 XORS
06E 19-127 XORS

EPBØØØ J7
EPBØ1Ø J7
EPBØ2Ø J7
EPBØ3Ø J7
EPBØ4Ø J7
EPBØ5Ø J7
EPBØ6Ø J8

GOOD PARITY REGISTER
04F
19-232 A
GPØØØ 9D8
GPØ1Ø 9D8
GPØ2Ø 9D9
GPØ3Ø 9D9
GPØ4Ø 9D8
GPØ5Ø 9D8
GPØ6Ø 9D9

14M6 LDGP1
14H3 RSTI
14H2 TELØ
14A3 WRTI
03J 19-236 5A
05H 19-234 SN
03F 19-057 5G

WRITE PARITY REGISTER
4F4 PØØØ
4F6 PØ1Ø
4M4 PØ2Ø
4M6 PØ3Ø
5F4 PØ4Ø
5F6 PØ5Ø
5G7 PØ6Ø
15F3 WEØ
06K 19-232

6K1 EBØØØ
6K1 EBØ1Ø
6K2 EBØ2Ø
6K2 EBØ3Ø
6K3 EBØ4Ø
6K3 EBØ5Ø
6K4 EBØ6Ø
6K4 EBØ7Ø
6K5 EBØ8Ø
6K6 EBØ9Ø
6K6 EB1ØØ
6K7 EB11Ø
6K7 EB12Ø
6K8 EB13Ø
6K8 EB14Ø
6K9 EB15Ø
6C1 EB16Ø
6C1 EB17Ø
6C2 EB18Ø
6C2 EB19Ø
6C3 EB2ØØ
6C3 EB21Ø
6C4 EB22Ø
6C4 EB23Ø
6C5 EB24Ø
6C6 EB25Ø
6C6 EB26Ø
6C7 EB27Ø
6C7 EB28Ø
6C8 EB29Ø
6C8 EB3ØØ
6C9 EB31Ø
C1 EPBØØØ
C2 EPBØ1Ø
C3 EPBØ2Ø
C4 EPBØ3Ø
C5 EPBØ4Ø
C6 EPBØ5Ø
C7 EPBØ6Ø

08D 19-241 SN
10D 19-241 SN
12D 19-241 SN
06D 19-241 SN

13D 19-128 5G

15N9 LMBYI
16E3 TB08I
1455 FNPMO
05F 14C 19-063 DC
06Z 19-125 SN
UCE0 12A1, 15A2
UCE1 12N4, M9
UCEØ 118-0
00K 69 Ω 470 P5

MERI 556

3F2 ELMAØ1
3F2 ELMA11
3F2 ELMA21
3F4 ELMA31
3F2 BAØØØ
07D 19-160 LA
16C 19-131 QDFF

209-4 210-4 05 16A 77 330 P5 (MEA1)
206-4 207-4 04 16A 78 330 P5 (MEA2)
203-4 204-4 03 16A 79 330 P5 (MEA3)
200-4 201-4 02 16A 80 330 P5 (MEA4)

UNCORRECTED ERROR LEDS

13E4 3CLROC
09J 19-236 5A
10G4 ELDUAØ
06R 19-125 5BD
09M 1K
TP11 214-5
TP12 213-5
SEE NOTES
16 P5
14N4 NPMØ
N4 UCE1
216-4 01 16A 81 330 P5(UCE)
NON PRESENT MEMORY - LAMP-OFF
INCORRECTABLE ERROR - LAMP-ON
CLR
CLK
CLR 19-131 QDFF

NOTES:
1. FOR CUSTOMER SERVICE ONLY:
TO TURN OFF UCE/NPM AND MODULE I.D. LAMPS;
CONNECT TP11 TO TP12 MOMENTARILY. DO NOT STRAP.
MAKE SURE TO REMOVE THE JUMPER.

PARITY CORRECTOR & UNCORRECTABLE ERROR

SCALE -
NAME | TITLE | DATE
DRAFT
CHK
ENGR

TITLE : SCHEMATIC
LBC (8MB CAPABILTY)
TAB NO 03183
DWG NO 35-806 D08
SHEET OF 7 - 18

DRAWING 44-231 24830

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

LMB BUS
DRIVERS AND RECEIVERS

SCALE–	NAME	TITLE	DATE
TOLERANCE .XXX ± .005, .XX ± .02, .X ± .09, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC
LBC (8MB CAPABILITY)

TASK NO. 03183
DWG NO. 33-806 D08
SHEET OF 8 — 18

REVISIONS					
AREA L9 RES. OOK WAS 09M W/ PIN 16 TO P5 & PIN 09 TO NVMØ, VALUE 1K					
RS	U.P.	4763		8-18-81	R01
AREA K9, EXTENSIVE CHANGES MADE TO IC 15M, FOR PREVIOUS REV LEVEL SEE R01 MICRO-FILM COPY.					
KR		4909	MS	1-15-82	R02

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Oceanport, N.J. 07757

TITLE SCHEMATIC

LBC (8MB CAPABILITY)

DRAFTER	TASK 03183	SHT
D STINE	DWG 35-806 R02 D08	9 - 18
DATE 12-11-80		

NOTES

WRITE/READ ERROR LOGGER
ADDRESS MUX

ERROR LOGGER
SHIFT REGISTER

REVISIONS					
AREA N-5, DELETED 1K RESISTOR 09M BETWEEN OGR03 & P5.					
JAH	JJ	5089	MS	8-19-82	R01

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
LBC (8MB CAPABILITY)

ERROR LOGGER

NOTES

DRAFTER		
DSTINE		
DATE	TASK 03183	SHT
12-15-80	DWG 35-806 R01 D08	10 - 18

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

CACHE 256 x 36

CACHE PARITY CHECK

16H7 TAA121 — FW WRITE
14G4 SFW1
12J7 HIT1
16D1 TB061 — PW WRITE
14H3 SPW1
15L2 MEI — 03J 19-236 SA
16J7 QWM1
16H2 TB121 — QW ERR
16B4 TB061 — 03J 19-236 SA
16E4 TB080 — QW NO ERR
20C 19-062
08 CAWE0
16J6 CAEN0

3C8 A22Ø
3C8 A23Ø
3C8 A24Ø
3C8 A25Ø
3C8 A26Ø
3C9 A27Ø
3K7 A28Ø
3J3 A29Ø

21K * 19-254 256x9 RAM — A
22K * 19-254 256x9 RAM — A
24K * 19-254 256x9 RAM — A
25K * 19-254 256x9 RAM — A

23K * 70 470 P5
23K * 71 470 P5
23K * 72 470 P5
23K * T3 470 P5

23J * 19-055 SG

21J * 19-223 9BIT EVEN/ODD PARITY GEN/CHK — B — EVEN OUT 05 NC; ODD OUT 06
22J * 19-223 9BIT EVEN/ODD PARITY GEN/CHK — B — 05 NC
24J 19-223 9BIT EVEN/ODD PARITY GEN/CHK — B — 05 NC
SEE NOTE 1
25J 19-223 9BIT EVEN/ODD PARITY GEN/CHK — B — 05 NC

23K * 19-056 SG0

21H * 19-080 SG — 06 PER1 16L8, 15A8

XRP2 14K3
12S6 CHIT1 — 12A * 19-049 SF — DS 09 NC; DC 07
16R9 CPER1
13E4 SCLR0C
218-4
219-4
330 16A * 76 P5
CACHE PARITY ERROR

1657 CAEN1

NOTE 1. DEPOPULATE COMPONENTS MARKED WITH AN ASTERISK FOR F02 VARIATION.

CACHE & CACHE PARITY

SCALE —
TOLERANCE: XXX ± .005; XX ± .02; X ± .03; ANGLES ± 1°; UNLESS OTHERWISE SPECIFIED

	NAME	DATE
DRAFT		
CHK		
ENGR		

TITLE SCHEMATIC
LBC (8MB CAPABILITY)

TAB NO. 03183
DWG NO 35-606 D08
SHEET OF 11—18

PERKIN-ELMER
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REVISIONS
AREA M6, ADDED MISBI & MISAI W/CROSS REF 15AB TO 18F09 & 18F10. AREA N6, ADDED MISSI W/CROSS REF 15A7 TO 18FB1.
KR | | 4909 | MS | 1-15-82 | R01 |

STBO 13H2
TELO 14H2
RSTO 14H2
UCEO 7S4
21H* 19-060 SG
VALØ
21E 19-055 SG
VALI N1
N3

21D 19-259 P/O 2-TO-4 LINE DECODER/DEMULTIPLEXER
3C8 A220, A230
16S7 QWM1, TAA121 16H7
14A 19-055 SG
2Y3, 2Y1, 2Y2, 2Y0

25M* 19-065 2 TO 1 MUX
3C8 A260, 3C5 A190, 3C9 A270, 3C6 A200
NC, NC, NC, NC
13H2 STB1

24M* 19-065 2 TO 1 MUX
3C8 A220, 3C4 A150, 3C8 A230, 3C5 A160, 3C8 A240, 3C5 A170, 3C8 A250, 3C5 A180
ENB, SEL

VALI H1

26R 19-237 256X1 RAM
DATA IN, DATA OUT, WE
NVALI 16L9, N7, 15AB

CACHE VALIDATOR

A0B0:A810 TAG FIELD
3C1 A080, 3C2 A090, 3C2 A100, 3C2 A110
3C3 A120, 3C3 A130, 3C3 A140, 3C4 A150
3C5 A160, 3C5 A170, 3C5 A180, 3C5 A190
3C6 A200, 3C7 A210
3C8 A240, 3C8 A250, 3C8 A260, 3C9 A270

25A* 25B* 25C* 25E*
24A* 24B* 24C* 24E*
23A* 23B* 23C* 23E*
22A* 22B* 22C* 22E*
19-075 16X4 REG STK
SEE NOTE 2

TPP 203-3 TGA081
TPN 205-3 TGA101
TPM 206-3 TGA111
TPL 207-3 TGA121
TPK 208-3 TGA131
TPJ 209-3 TGA141
TPJ 210-3 TGA151
TPH 211-3 TGA161
TPG 212-3 TGA171
TPF 213-3 TGA181
TPE 214-3 TGA191
TPD 215-3 TGA201
TPC 216-3 TGA211

25D* 19-154
24D* 19-154
23D* 19-154

21A* EOUT 19-279
21B* 19-279 EOUT
TAG COMPARE

A2B0:A870 INDEX ADDRESS

FI VALØ, 16D5 TA061, S7 HITI
HIT
16E3 TB081, 16G3 SPWI, 7R4 UCE1
UCE NORM MEM OP
UCE (QWM)
QWM
21C* 19-062 SG

07C 19-236 SA
16S7 QWM1
REFI 13J3
UCECLR0 14S9

15AB MISBI, MISAI
18F 19-241 SN
22D 19-057 SG
MISI 16L8, 15A9
NVALI N3
PSU
15A 19-234 SN
CHITI 11N6
STBO 13H2
P5 221-5 TP4, TP3 222-5, 81 18F 1K 85
15A7 MISSI
P5 4C 19-063 SF DC
HITI N9, 11C2
16D8 TA0B1, 13N8 MB1A
N.C.

CACHE HIT DETECTOR

NOTES:
1. REMOVE JUMPER 221-5 TO 222-5 TO FORCE CACHE MISSES.
2. DEPOPULATE IC'S MARKED WITH AN ASTERISK FOR F02 VARIATION.

SCALE—
NAME | TITLE | DATE
DRAFT
CHK
ENGR

TITLE SCHEMATIC
LBC (8MB CAPABILITY)
SIZE 03183 DWG 35-806R01 REV DOC 12 SHEET 12 OF 18

PERKIN-ELMER

Oceanport, N.J. 07757

REVISIONS				
IN AREA F9, F9, G9 ECS 01M01				
E&C COIL WIRE NOT SPECIFIED				
DS	UPP.	4763	8-18-81	R01
ADDED CROSS REF. 16H4 TO MB1B (AREA R-8).				
AW	AV	5089	MS	8-20-82 R02

16 MICRO SEC. OSC.

1.8 MS OSC.

BURST REFRESH

REFRESH COUNTERS

REFRESH & CONTROL

NOTE: 1 ALL IC ON THIS SHEET ARE P5U UNLESS NOTED OTHERWISE.

2 THIS STRAP MUST BE IN PLACE. IT IS REMOVED FOR TESTING PURPOSES ONLY.

SCALE–	NAME	TITLE	DATE
TOLERANCE .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC LBC (BMB CAPABILITY

FSCM NO. 03183 SIZE D DWG NO. 35-806R02 D08 SHEET OF 13—18

PERKIN-ELMER

Computer Systems Division
Oceanport N.J. 07757

REVISIONS				
AREA M3 WAS SHOWN AS FOLLOWS! REMOVED 18K RES & RE-LOCATED IT ON SHT 16.	KE	4909	MS	1-15-82	RO1

COMMAND DECODE AND CONTROL

SCALE—	NAME	TITLE	DATE
TOLERANCE: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC
LBC (8MB CAPABILITY)

TASK NO. 03183
DWG NO. 35-806 E01 D08
SHEET OF 14—18

PERKIN-ELMER
Systems Division
Oceanport N J 07757

REVISIONS				
APER F3, IC 18A13 WAS NOT SPEC., PIN 05 OF 20D WENT TO 19C13				
DS	AJA	4743	8-18-81	R01
EXTENSIVE CHANGES TO AREA A8, J7 ETC. (REVISED PREVIOUS REV LEVEL SEE R01 MICRO-FILM COPY.				
XR	AJ	4909	1-19-82	R02

CONTROL

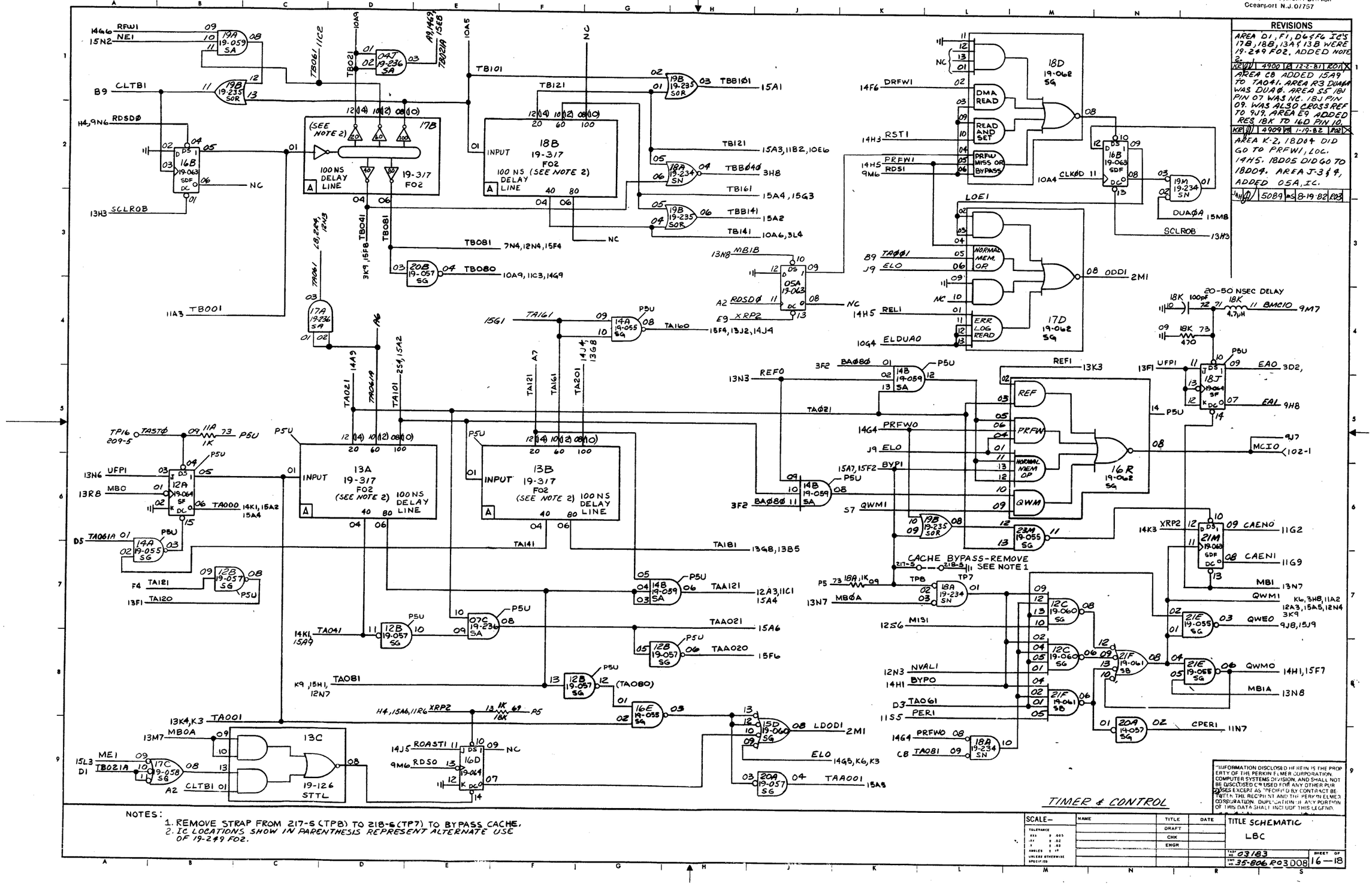
SCALE–	NAME		TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .05, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		DRAFT		
		CHK		
		ENGR		

TITLE SCHEMATIC
LBC (8MB CAPABILITY)

TASK NO. 03183 SHEET OF 15–18
DWG NO. 35-806,R02,D08

PERKIN-ELMER
~~Computer Systems Division~~
Oceanport N.J. 07757

REVISIONS				
AREA D1, F1, D4 & F6 IC'S 17B, 18B, 13A & 13B WERE 19-249 F02. ADDED NOTE 2.	KRT	4900	12-2-81	ROI
AREA C8 ADDED 15A9 TO TA041. AREA R3 DUA6A WAS DUA8. AREA S5 18J PIN 07 WAS NC. 18J PIN 09. WAS ALSO CROSS REF TO 9J9. AREA E9 ADDED RES 18K TO 16D PIN 10.	KRT	4909	1-19-82	R02
AREA K-2, 18D04 DID GO TO PRFW1, LOC. 19H5. 18D05 DID GO TO 18D09. AREA J-3 & 4, ADDED 05A, IC.	JHW	5089	8-19-82	R03



NOTES:
1. REMOVE STRAP FROM 217-S (TP8) TO 218-6 (TP7) TO BYPASS CACHE.
2. IC LOCATIONS SHOW IN PARENTHESIS REPRESENT ALTERNATE USE OF 19-249 F02.

SCALE–	NAME	TITLE	DATE
TOLERANCE .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE SCHEMATIC
LBC
TASK NO. 03183
DWG NO. 35-806 R03 D08
SHEET OF 16—18

CROSS REFERENCE NET#, MNEMONIC, SHEET#

NETS	MNEMONIC	SH	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.
0001	A080	3	0063	D090	11	0125			0187	ELMA31	3	0249	LMB111	8	0311	MDSI50	2	0373	RD021	3	0435	TA161	16	0497	07J05	4	0559	05E06	7	0621	22E02	12	0683	20M08	14
0002	A090	3	0064	D100	11	0126	EB000	6	0188	FNPMO	14	0250	LMB121	8	0312	MDSI60	2	0374	RD031	3	0436	TA181	16	0498	07K06	4	0560	05E08	7	0622	TGA081	12	0684	22H06	14
0003	A100	3	0065	D110	11	0127	EB010	6	0189			0251	LMB131	8	0313	MDSI70	2	0375	RDSO	9	0437	TA201	16	0499	07K05	4	0561	05E11	7	0623	TGA091	12	0685	20J14	14
0004	A110	3	0066	D120	11	0128	EB020	6	0190	TP9	3	0252	LMB141	8	0314	MDSI80	2	0376	RDSI	9	0438	TB001	16	0500	08J06	4	0562	06E03	7	0624	TGA101	12	0686	17H10	14
0005	A120	3	0067	D130	11	0129	EB030	6	0191	LD01	10	0253	LMB151	8	0315	MDSI90	2	0377	REO	15	0439	TB021	16	0501	08J05	4	0563	06E06	7	0625	TGA111	12	0687	21D04	14
0006	A130	3	0068	D140	11	0130	EB040	6	0192	LD02	10	0254	LMB161	8	0316	MDS200	2	0378	REI	15	0440	TB041	16	0502	08K06	4	0564	06E08	7	0626	TGA121	12	0688	21D05	14
0007	A140	3	0069	D150	11	0131	EB050	6	0193	LDBY01	14	0255	LMB171	8	0317	MDS210	2	0379	REFO	13	0441	TB061	16	0503	08K05	4	0565	08D05	7	0627	TGA131	12	0689	21D06	14
0008	A150	3	0070	D160	11	0132	EB060	6	0194	LDBY11	14	0256	LMB181	8	0318	MDS220	2	0380	REFOA	13	0442	TB081	16	0504	09J06	4	0566	08D06	7	0628	TGA141	12	0690	21D07	14
0009	A160	3	0071	D170	11	0133	EB070	6	0195	LDBY21	14	0257	LMB191	8	0319	MDS230	2	0381	REFI	13	0443	TB101	16	0505	09J05	4	0567	10D05	7	0629	TGA151	12	0691	16D05	14
0010	A170	3	0072	D180	11	0134	EB080	6	0196	LDBY31	14	0258	LMB201	8	0320	MDS240	2	0382	RELI	14	0444	TB121	16	0506	09K06	4	0568	10D06	7	0630	TGA161	12	0692	22F08	14
0011	A180	3	0073	D190	11	0135	EB090	6	0197	LDGPI	14	0259	LMB211	8	0321	MDS250	2	0383	REQI	13	0445	TB141	16	0507	09K05	4	0569	12D05	7	0631	TGA171	12	0693	02F06	14
0012	A190	3	0074	D200	11	0136	EB100	6	0198	LDOD1	16	0260	LMB221	8	0322	MDS260	2	0384	RFAOI	13	0446	TB161	16	0508	10J06	4	0570	12D06	7	0632	TGA181	12	0694	01C06	14
0013	A200	3	0075	D210	11	0137	EB110	6	0199	LMBY0	15	0261	LMB231	8	0323	MDS270	2	0385	RFA11	13	0447	TB080	16	0509	10J05	4	0571	06D05	7	0633	TGA191	12	0695	03C06	14
0014	A210	3	0076	D220	11	0138			0200	LMBY1	15	0262	LMB241	9	0324	MDS280	2	0386	RFA21	13	0448	TAA020	16	0510	10K06	4	0572	06D06	7	0634	TGA201	12	0696	02C06	14
0015	A220	3	0077	D230	11	0139	EB120	6	0201	LOE1	16	0263	LMB251	9	0325	MDS290	2	0387	RFA31	13	0449	TAA001	16	0511	10K05	4	0573	05H01	7	0635	TGA211	12	0697	04C06	14
0016	A230	3	0078	D240	11	0140	EB130	6	0202	GP000	7	0264	LMB261	9	0326	MDS300	2	0388	RFA41	13	0450	TAA121	16	0512	11J06	5	0574	03J03	7	0636	25M04	12	0698	03C08	14
0017	A240	3	0079	D250	11	0141	EB140	6	0203	GP010	7	0265	LMB271	9	0327	MDS310	2	0389	RFA51	13	0451	TBB040	16	0513	11J05	5	0575	03F08	7	0637	25M07	12	0699	19C06	15
0018	A250	3	0080	D260	11	0142	EB150	6	0204	GP020	7	0266	LMB281	9	0328	MREO	9	0390	RFA61	13	0452	TBB101	16	0514	11K06	5	0576	13D09	7	0638	24M04	12	0700	18C06	15
0019	A260	3	0081	D270	11	0143	EB160	6	0205	GP030	7	0267	LMB291	9	0329	MREFO	9	0391	RFA71	13	0453	TBB141	16	0515	11K05	5	0577	16C02	7	0639	24M07	12	0701	15J11	15
0020	A270	3	0082	D280	11	0144	EB170	6	0206	GP040	7	0268	LMB301	9	0330	MWA001	9	0392	RFQI	15	0454	TAA021	16	0516	12J06	5	0578	42X10	7	0640	24M09	12	0702	19C11	15
0021	A280	3	0083	D290	11	0145	EB180	6	0207	GP050	7	0269	LMB311	9	0331	MWA011	9	0393	RFWI	14	0455	TEL0	14	0517	12J05	5	0579	16C07	7	0641	24M12	12	0703	17C12	15
0022	A290	3	0084	D300	11	0146	EB190	6	0208	GP060	7	0270	LMB321	9	0332	MWEO	9	0394	RDSTI	14	0456	TEL1	14	0518	12K06	5	0580	42X07	7	0642	21C08	12	0704	15E03	15
0023	A300	3	0085	D310	11	0147	EB200	6	0209	GDDI	15	0271	LMB331	9	0333	MXO21	3	0395	RSELO	13	0457	UP000	9	0519	12K05	5	0581	16C10	7	0643	18F06	12	0705	18C08	15
0024	A310	3	0086	D000A	15	0148	EB210	6	0210	GMERI	15	0272	LMB341	9	0334	MX031	3	0396	RSTO	14	0458	UP010	9	0520	13J06	5	0582	42X04	7	0644	MISS1	12	0706	15A10	15
0025	A161	10	0087	D020A	15	0149	EB220	6	0211	GMVFO	9	0273	LMB351	9	0335	NCEO	9	0397	RSTI	14	0459	UP020	9	0521	13J05	5	0583	42X00	7	0645	25D02	12	0707	14J06	15
0026	A171	10	0088	D160A	15	0150	EB230	6	0212	HITI	12	0274	LMB361	9	0336	NCLRI	14	0398	RUREI	14	0460	UP030	9	0522	13K06	5	0584	42X01	7	0646	25D04	12	0708	14J08	15
0027	A181	10	0089	DA00	5	0151	EB240	6	0213	LMA080	3	0275	LMB371	9	0337	NEO	15	0399	SO01	10	0461	UP040	9	0523	13K05	5	0585	15C03	7	0647	25D06	12	0709	05K08	15
0028	A191	3	0090	DA10	5	0152	EB250	6	0214	LMA090	3	0276	LMB381	9	0338	NEI	15	0400	SO11	10	0462	UP050	9	0524	03F02	5	0586	42X16	7	0648	25D08	12	0710	18J06	15
0029	A301	14	0091	DA20	5	0153	EB260	6	0215	LMA100	3	0277	MBO	13	0339	NPMO	14	0401	SO21	10	0463	UP060	9	0525			0587	09M14	7	0649	MISB1	12	0711	23M08	15
0030	ADO1	10	0092	DA30	5	0154	EB270	6	0216	LMA110	3	0278	MBOA	13	0340	NBALI	12	0402	SO31	10	0464	UCE0	7	0526	11E03	6	0588	09K10	9	0650	MISA1	12	0712	18H06	15
0031	AD11	10	0093	DA40	5	0155	EB280	6	0217	LMA120	3	0279	MBI	13	0341	NVMO	9	0403	SO41	10	0465	UCE1	7	0527	11E06	6	0589	P500K		0651	25D10	12	0713	18K05	15
0032	AD21	10	0094	DB00	5	0156	EB290	6	0218	LMA130	3	0280	MBIA	13	0342	ODDI	16	0404	SO51	10	0466	UDD0	15	0528	11E08	6	0590	19M10	9	0652	25D12	12	0714	04J08	15
0033	AD31	10	0095	DB10	5	0157	EB300	6	0219	LMA140	3	0281	MBIB	13	0343	MATRO	14	0405	SO61	10	0467	UDD1	15	0529	11E11	6	0591	17H02	10	0653	24D02	12	0715	04J06	15
0034	BMC10	9	0096	DB20	5	0158	EB310	6	0220	LMA150	3	0282	MBIC	13	0344	MATDO	14	0406	SDYI	14	0468	UFP1	16	0530	12E03	6	0592	15H06	10	0654	24D04	12	0716	17J08	15
0035	BMVFO	9	0097	DB30	5	0159	EPB000	7	0221	LMA160	3	0283	MCI0	16	0345	PSFWO	14	0407	SCLKI	9	0469	VAL0	12	0531	12E06	6	0593	05K05	10	0655	24D06	12	0717	23D06	15
0036	BSCLRO	9	0098	DB40	5	0160	EPB010	7	0222			0284	MCCO	9	0346	PSHWO	14	0408	SCLKIA	9	0470	VALI	12	0532	12E08	6	0594	15E06	10	0656	24D08	12	0718	16E08	15
0037	BYPO	16	0099	DB50	5	0161	EPB020	7	0223	LMAI70	3	0285	MEO	10	0347	POOO	4	0409	SCLKOA	10	0471	WA000	3	0533	12E11	6	0595	22M08	10	0657	24D10	12	0719	05C06	14
0038	BYPI	16	0100	DB60	5	0162	EPB030	7	0224	LMAI80	3	0286	MEI	15	0348	PO10	4	0410	SCLRIB	13	0472	WA001	3	0534	13E03	6	0596	16H06	10	0658	24D12	12	0720	15E11	14
0039	CAENO	16	0101	DB70	5	0163	EPB040	7	0225	LMAI90	3	0287	MEA000	9	0349	PO20	4	0411	SCLRO	13	0473	WA010	3	0535	13E06	6	0597	19M04	10	0659	23D02	12	0721	19E13	14
0040	CAENI	16	0102	DC00	5	0164	EPB050	7	0226	LMA200	3	0288	MEA010	9	0350	PO30	4	0412	SCLROB	13	0474	WA011	3	0536	13E08	6	0598	16H08	10	0660	23D04	12	0722	15J08	14
0041	CARI	13	0103	DC10	5	0165	EPB060	7	0227	LMA210	3	0289	MEA020	9	0351	PO40	5	0413	SCLROC	13	0475	WCO	3	0537	13E11	6	0599		10	0661	05A67	13	0723	15D06	14
0042	CAWEO	11	0104	DC20	5	0166	EAO	16	0228	LMA220	3	0290	MEA030	9	0352	PO50	5	0414	SFWO	14	0476	WCC0	3	0538	14E03	6	0600	18K12	10	0662	05A63	13	0724	15E08	14
0043	CBO11	3	0105	DC30	5	0167	EDO	15	0229	LMA230	3	0291	MERO	5	0353	PO60	5	0415	SFWI	14	0477	WCCI	3	0539	14E06	6	0601	23K03	11	0663	06A02	13	0725	16D06	14
0044	CB021	3	0106	DC40	5	0168	EDI	15	0230	LMA240	3	0292	MERI	5	0354	PERI	11	0416	SHIFTI	10	0478	WDENO	3	0540	14E08	6	0602	23K06	11	0664	09A06	13	0726	18E08	14
0045	CB031	3	0107	DC50	5	0169	ELO	14	0231	LMA250	3	0293	MISI	12	0355	PFSDO	9	0417	SHWI	14	0479	WEO	15	0541	14E11	6	0603	23K08	11	0665	07A09	13	0727	17F06	14
0046	CHI21	12	0108	DC60	5	0170	ELDUAO	10	0232	LMA260	3	0294	MRDSO	9	0356	PFSDI	13	0418	SPWO	14	0480	WEI	15	0542	07E03	6	0604	23K11	11	0666	09B08	13	0728	17E05	14
0047	CLKOD	10	0109	DC70	5	0171	ELDUAI	10	0233	LMA270	3	0295	MDS000	2	0357	PRFWO	14	0419	SPWI	14	0481	WRTO	3	0543	07E06	6	0605	23J03	11	0667	09A71	13	0729	22H05	14
0048	CLKIC	9	0110	DERRO	5	0172	ELSTI	14	0234	LMA280	3	0296	MDS010	2	0358	PRFWI	14	0420	STBO	13	0482	WRTOA	3	0544	07E08	6	0606	23J06	11	0668	10A06	13	0730	18F05	15
0049	CLKID	9	0111	DHWO	3	0173	ENDI	13	0235	LMA290	3	0297	MDS020	2	0359	PSBYO	14	0421	STBI	13	0483	WRTI	14	0545	07E11	6	0607	23J08	11	0669	09A08	13	0731	14J03	15
0050	CLRO	13	0112	DMHWO	3	0174	ERO	13	0236	LMA300	3	0298	MDS030	2	0360	PSELI	14	0422	TA000	16	0484	XRPI	15	0546	08E03	6	0608	23J11	11	0670	08B12	13	0732	19J08	15
0051	CLROB	15	0113	DPRI	13	0175			0237	LMA310	8	0299	MDS040	2	0361	PSELIA	3	0423	TA080	16	0485	XRP2	16	0547	08E06	6	0609	23K01	11	0671	06A14	13	0733	16J06	15
0052	CLTBI	16	0114	DRELI	14	0176	ELA040	10	0238	LMB001	8	0300	MDS050	2	0362	QWEO	16	0424	TA120	16	0486	21R19	9	0548	08E08	6	0610	22J06	11	0672	06A01	13	0734	20K08	15
0053	CPERI	16	0115	DRFWO	14	0177	ELA050	10	0239	LMB011	8	0301	MDS060	2	0363	QWMO	16	0425			0487	03J06	2	0549	08E11	6	0611	24J06	11	0673	06A14	13	0735	16J07	15
0054	D000	11	0116	DRFWI	14	0178	ELA060	10	0240	LMB021	8	0302	MDS070	2	0364	QWMI	16	0426	TA160	16	0488	18R03	3	0550	09E03	6	0612	25J06	11	0674	11B15	13	0736	16J09	15
0055	D010	11	0117	DDSFWO	14	0179	ELA070	10	0241	LMB031	8	0303			0365	RCARO	10	0427	TA001	16	0489	18R06	3	0551	09E06	6	0613	12A07	11	0675	09A03	13	0737	19C03	15
0056	D020	11	0118	DDSHWO	14	0180	ELA080	10	0242	LMB041	8	0304	MDS080	2	0366	RCLCO	9	0428	TA021	16	0490	23F08	3	0552	09E08	6	0614	42X19	11	0676	22M06	13	0738	15A13	15
0057	D030	11	0119	DUAØ	15	0181	ELA090	10	0243	LMB051	8	0305	MDS090	2	0367	RCLCI	9	0429	TA041	16	0491	22H03	3	0553	09E11	6	0615	03J11	11	0677			0739	19A08	16
0058	D040	11	0120	DUA1	15	0182	ELA100	10	0244	LMB061	8	0306	MDS100	2	0368	RCLRO	13	0430	TA061	16	0492	18R11	3	0554	10E03	6	0616	03J08	11	0678	15B08	13	0740	14A03	16
0059	D050	11	0121	DSHWO	14	0183	ELA110	10	0245	LMB071	8	0307	MDS110	2	0369	RCLRI	13	0431	TA081	16	0493	24F05	3	0555	10E06	6	0617	14A05	12	0679	08B06	13	0741	17C08	16
0061	D070	11	0123	20J14	14	0185	ELMA11	3	0247	LMB091	8	0309	MDS130	2	0371	RCT1	13	0433	TA121	16	0495	21E11	3	0557	10E11	6	0619	22B02	12	0681	19E01	14	0743	12B10	16
0062	D080	11	0124	MARSTO	14	0186	ELMA21	3	0248	LMB101	8	0310	MDS140	2	0372	RDO11	3	0434	TA141	16	0496	07J06	4	0558	05E03	7	0620	22L02	12	0682	22D08	14	0744	16D07	16

NOTES

REVISIONS

DELETED NET 175 SIG. EWE1.					
RS	WP	4763		8-18-81	R01
NET 119 WAS DAO. NET 644 WAS 52A21. NET 649 WAS 21A19. NET 650 WAS 21B19.					
KR	WP	4909	M81-11-78-B2		802IX

UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME	TITLE	DATE
	DES/DFT	
	SUPV	
	CHK	
	ENG	
	MGR	
	QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE

LBC
(SMB CAPABILITY)

TASK 03183	SHT
DWG 35-806 R02 D08	17-18

CROSS REFERENCE NET#, MNEMONIC, SHEET#

NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.	NETS	MNEMONIC	SH.
0745	16E03	16	0807	GND16J		0869	09B04	15	0931			0993			1055			1117			1179			1241			1303			1365			1427		
0746	14B11	16	0808	GND20D		0870	06C03	15	0932			0994			1056			1118			1180			1242			1304			1366			1428		
0747	14B08	16	0809	GND08A		0871	07D03	7	0933			0995			1057			1119			1181			1243			1305			1367			1429		
0748	19B08	16	0810	13C06	2	0872	07D06	7	0934			0996			1058			1120			1182			1244			1306			1368			1430		
0749	18A10	16	0811	GND10C		0873	07D08	7	0935			0997			1059			1121			1183			1245			1307			1369			1431		
0750	12C08	16	0812	06R08	7	0874	07D11	7	0936			0998			1060			1122			1184			1246			1308			1370			1432		
0751	12C06	16	0813	04J11	7	0875			0937			0999			1061			1123			1185			1247			1309			1371			1433		
0752	21F06	16	0814	TB02IA	15	0876	MERRI	3	0938			1000			1062			1124			1186			1248			1310			1372			1434		
0753	23M11	16	0815	42X13	13	0877	01M01	13	0939			1001			1063			1125			1187			1249			1311			1373			1435		
0754	18K71	16	0816	52X19	13	0878	06C08	13	0940			1002			1064			1126			1188			1250			1312			1374			1436		
0755	16B08	16	0817			0879	EWE0	15	0941			1003			1065			1127			1189			1251			1313			1375			1437		
0756	19M01	16	0818	MATRSRØ	3	0880	18A13	15	0942			1004			1066			1128			1190			1252			1314			1376			1438		
0757	18D08	16	0819	MATRSDØ	3	0881	P5U06C	9	0943			1005			1067			1129			1191			1253			1315			1377			1439		
0758	P5U09A		0820	DMARSØ	3	0882	/3A GND	16	0944			1006			1068			1130			1192			1254			1316			1378			1440		
0759			0821	RDSDØ	9	0883	/3B GND	16	0945			1007			1069			1131			1193			1255			1317			1379			1441		
0760	P5U07B		0822	CLKØE	9	0884	/17 GND	16	0946			1008			1070			1132			1194			1256			1318			1380			1442		
0761	P5U05A		0823	07C11	12	0885	/8B GND	16	0947			1009			1071			1133			1195			1257			1319			1381			1443		
0762			0824	UCECLRO	14	0886	DUAØA	15	0948			1010			1072			1134			1196			1258			1320			1382			1444		
0763	GND20R		0825	NCAR1	13	0887	BPMS1	15	0949			1011			1073			1135			1197			1259			1321			1383			1445		
0764	GND19R		0826	07C06	13	0888	EA1	9	0950			1012			1074			1136			1198			1260			1322			1384			1446		
0765	GND23F		0827	08C01	13	0889	GNDØSA	16	0951			1013			1075			1137			1199			1261			1323			1385			1447		
0766	GND07K		0828	08A08	13	0890	05A09	16	0952			1014			1076			1138			1200			1262			1324			1386			1448		
0767	GND08K		0829			0891			0953			1015			1077			1139			1201			1263			1325			1387			1449		
0768	GND09K		0830	19F06	13	0892			0954			1016			1078			1140			1202			1264			1326			1388			1450		
0769	GND10K		0831		14	0893			0955			1017			1079			1141			1203			1265			1327			1389			1451		
0770	GND11K		0832	CCARI	13	0894			0956			1018			1080			1142			1204			1266			1328			1390			1452		
0771	GND12K		0833	7A06IA	14	0895			0957			1019			1081			1143			1205			1267			1329			1391			1453		
0772	GND13K		0834	07M11	10	0896			0958			1020			1082			1144			1206			1268			1330			1392			1454		
0773	GND06D		0835			0897			0959			1021			1083			1145			1207			1269			1331			1393			1455		
0774	GND21R		0836	GND09C	3	0898			0960			1022			1084			1146			1208			1270			1332			1394			1456		
0775	GND07M		0837	ERLA01	3	0899			0961			1023			1085			1147			1209			1271			1333			1395			1457		
0776	GND15F		0838	BA090	3	0900			0962			1024			1086			1148			1210			1272			1334			1396			1458		
0777	GND16F		0839	BA091	3	0901			0963			1025			1087			1149			1211			1273			1335			1397			1459		
0778	GND05K		0840	GND14D	3	0902			0964			1026			1088			1150			1212			1274			1336			1398			1460		
0779	GND21K		0841	09C07	3	0903			0965			1027			1089			1151			1213			1275			1337			1399			1461		
0780	GND22K		0842	MX011	3	0904			0966			1028			1090			1152			1214			1276			1338			1400			1462		
0781	GND24K		0843	15H08	10	0905			0967			1029			1091			1153			1215			1277			1339			1401			1463		
0782	GND06J		0844	13H06	10	0906			0968			1030			1092			1154			1216			1278			1340			1402			1464		
0783	GND17J		0845	RELA1	10	0907			0969			1031			1093			1155			1217			1279			1341			1403			1465		
0784	GND18J		0846	02K06	10	0908			0970			1032			1094			1156			1218			1280			1342			1404			1466		
0785	GND01H		0847	06M01	10	0909			0971			1033			1095			1157			1219			1281			1343			1405			1467		
0786	GND12H		0848	06M13	10	0910			0972			1034			1096			1158			1220			1282			1344			1406			1468		
0787	GND18D		0849	06M04	10	0911			0973			1035			1097			1159			1221			1283			1345			1407			1469		
0788	GND17D		0850	06M10	10	0912			0974			1036			1098			1160			1222			1284			1346			1408			1470		
0789	GND16B		0851	GND05M	10	0913			0975			1037			1099			1161			1223			1285			1347			1409			1471		
0790	GND12A		0852	05M09	10	0914			0976			1038			1100			1162			1224			1286			1348			1410			1472		
0791	GND16D		0853	02K12	10	0915			0977			1039			1101			1163			1225			1287			1349			1411			1473		
0792	GND13D		0854	02K08	10	0916			0978			1040			1102			1164			1226			1288			1350			1412			1474		
0793	GND22A		0855	GND02M	10	0917			0979			1041			1103			1165			1227			1289			1351			1413			1475		
0794	GND22B		0856	02M05	10	0918			0980			1042			1104			1166			1228			1290			1352			1414			1476		
0795	GND22C		0857	22M06	10	0919			0981			1043			1105			1167			1229			1291			1353			1415			1477		
0796	GND22E		0858			0920			0982			1044			1106			1168			1230			1292			1354			1416			1478		
0797	GND25K		0859	10A11	13	0921			0983			1045			1107			1169			1231			1293			1355			1417			1479		
0798	GND25R		0860	10A08	13	0922			0984			1046			1108			1170			1232			1294			1356			1418			1480		
0799	GND17E		0861	CSTRIN10	13	0923			0985			1047			1109			1171			1233			1295			1357			1419			1481		
0800	GND21D		0862	CSTRIN00	13	0924			0986			1048			1110			1172			1234			1296			1358			1420			1482		
0801	GND21A		0863	RFCTLDO	13	0925			0987			1049			1111			1173			1235			1297			1359			1421			1483		
0802	GND21B		0864	PFSDIA	13	0926			0988			1050			1112			1174			1236			1298			1360			1422			1484		
0803			0865	TASTO	16	0927			0989			1051			1113			1175			1237			1299			1361			1423			1485		
0804	GND24M		0866	BA080	3	0928			0990			1052			1114			1176			1238			1300			1362			1424			1486		
0805	GND25M		0867	17A08	14	0929			0991			1053			1115			1177			1239			1301			1363			1425			1487		
0806	GND26R		0868	16E11	14	0930			0992			1054			1116			1178			1240			1302			1364			1426			1488		

NOTES

REVISIONS					
NETS 876 THRU 881 WERE NOT SPECIFIED					
RS	4763		8-18-81	R01	
NET 818 WAS MNEMONIC "06C03"					
JLV	4855	R	11-11-81	R02	
ADDED NETS 882-885.					
KR	4900	P	12-2-81	R03	X
ADDED NETS 886-888					
KR	4909	M	1/26/82	R04	X
ADDED NETS 889 & 890					
JAH	5089	MS	8/31/82	R05	

UNLESS OTHERWISE SPECIFIED			
SCALE: NONE	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
		DES/DFT	
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

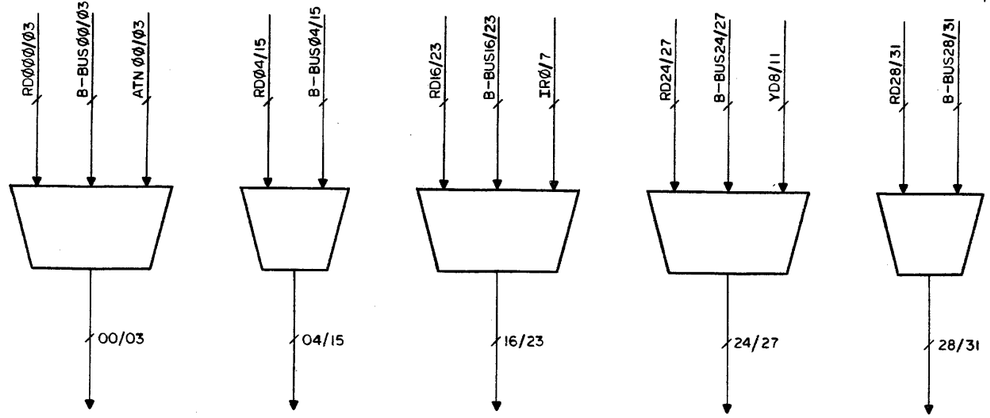
TITLE

LBC
(8 MB CAPABILITY)

TASK 03183	SHT
DWG 35-806 R05 DCB	18-18

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

BACKPANEL
CPU – A



TEST AID
DISPLAY

100-0,141-0,100-1,141-1,
100-2,124-2,200-2,224-2,

101-0,111-0,128-0,137-0,
140-0,200-0,201-0,211-0,
228-0,237-0,240-0,241-0,
101-1,121-1,140-1,200-1,
201-1,221-1,240-1,101-2,
123-2,201-2,223-2,200-1

C9,C10
15μF
25V

C1 – C8

P5

CONN	TERM. NO.	CABLE CONNECTOR MAP ROW 2	CABLE CONNECTOR MAP ROW 1	BACK PANEL MAP ROW 1	BACK PANEL MAP ROW 2	TERM. NO.	CONN
2	16			P5		41	1
	15			GND	GND	40	
	14					39	
	13					38	
	12					37	
	11					36	
	10					35	
	09			RD22I	RD23I	34	
	08			RD2ØI	RD21I	33	
	07				RD19I	32	
	06			RD17Ø	RD18I	31	
	05				RD27I	30	
	04			RD25I	RD26I	29	
	03			RD24Ø	RD12I	28	
	02			RD14I	RD13I	27	
	01			RD15Ø	RD16I	26	
	00			RDØØI	RDØ1I	25	
				RDØ2I	RDØ3I	24	
				RDØ4I	RDØ5I	23	
	24			RD3ØI	RD31I	22	
	23			GND	GND	21	
	22			RDØ9Ø	RDIØØ	20	
	21			RD11Ø		19	
	20			RD28I	RD29I	18	
	19					17	
	18					16	
	17					15	
	16					14	
	15					13	
	14			IRØ7Ø	IRØ6Ø	12	
	13			IRØ5Ø	IRØ4Ø	11	
	12			IRØ3Ø	IRØ2Ø	10	
	11			IRØ1Ø	IRØØØ	09	
	10			YDØ8I	YDØ9I	08	
	09			YDIØI	YDIII	07	
	08			FLR28I	FLR29I	06	
	07			FLR3ØI	FLR31I	05	
	06					04	
	05					03	
	04					02	
	03			GND	GND	01	
	02			P5	GND	00	
	01						
	00			P5	GND	41	
				GND	GND	40	
						39	
						38	
				GND	GND	37	
	24	P5	P5			36	
	23	GND	GND			35	
	22					34	
	21	FLR29Ø	FLR28Ø			33	
	20	FLR31Ø	FLR3ØØ			32	
	19	MXDØ11	MXDØØ1	SFTENØ	DFTENØ	31	
	18	MXDØ31	MXDØ21	ATNØØØ	ATNØ1Ø	30	
	17	MXDØ51	MXDØ41	ATNØ2Ø	ATNØ3Ø	29	
	16	MXDØ71	MXDØ61	GND	GND	28	
	15	MXDØ91	MXDØ81	BØØI	BØ1I	27	
	14	MXDIII	MXDIØI	BØ2I	BØ3I	26	
	13	MXDI31	MXDI21	BØ4I	BØ5I	25	
	12	MXDI51	MXDI41	BØ6I	BØ7I	24	
	11	MXDI71	MXDI61	BØ8I	BØ9I	23	
	10	MXDI91	MXDI81	BIØI	BIII	22	
	09	MXD211	MXD2ØI	BI2I	BI3I	21	
	08	MXD231	MXD221	BI4I	BI5I	20	
	07	MXD251	MXD241	BI6I	BI7I	19	
	06	MXD271	MXD261	BI8I	BI9I	18	
	05	MXD291	MXD281	B2ØI	B2II	17	
	04	MXD3II	MXD3ØI	B22I	B23I	16	
	03	IRØ	RDØ	B24I	B25I	15	
	02			B26I	B27I	14	
	01	GND	GND	B28I	B29I	13	
	00	P5	P5	B3ØI	B3II	12	
				GND	GND	11	
						10	
	16					09	
	15					08	
	14					07	
	13					06	
	12					05	
	11					04	
	10					03	
	09					02	
	08			GND	GND	01	
	07			P5	GND	00	
	06						
	05						
	04						
	03						
	02						
	01						
	00						

REF. DESIG.	PART NUMBER	SPARE OUTPUT
A06	19-154	02,04,12
A02	19-154	06
SPARE I.C.'S		

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

REVISIONS
RELEASED FOR PRODUCTION
ENG. [illegible] DATE 4/23

USED IN MANUAL :
29-695

35-734MØ1	RØØ
BOARD	REV.

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE SAME REVISION LEVEL.

REVISION	Ø	Ø
SHEET	1	2

NOTES:
1. UNLESS OTHERWISE SPECIFIED :
   A. ALL RESISTORS ARE ± 5%, 1/4 W
   B. ALL CAPACITORS ARE .1μF, 30V

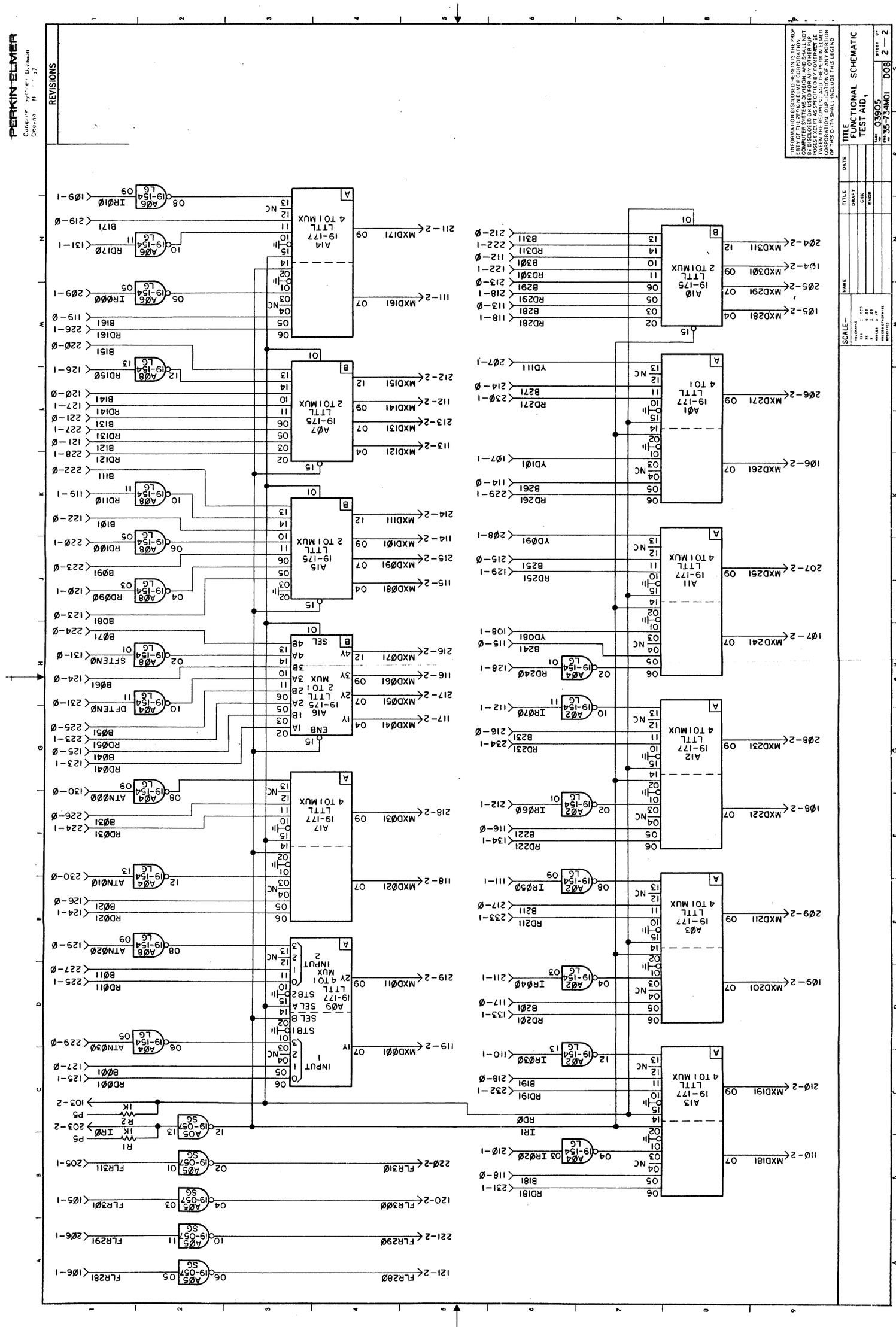
SCALE —

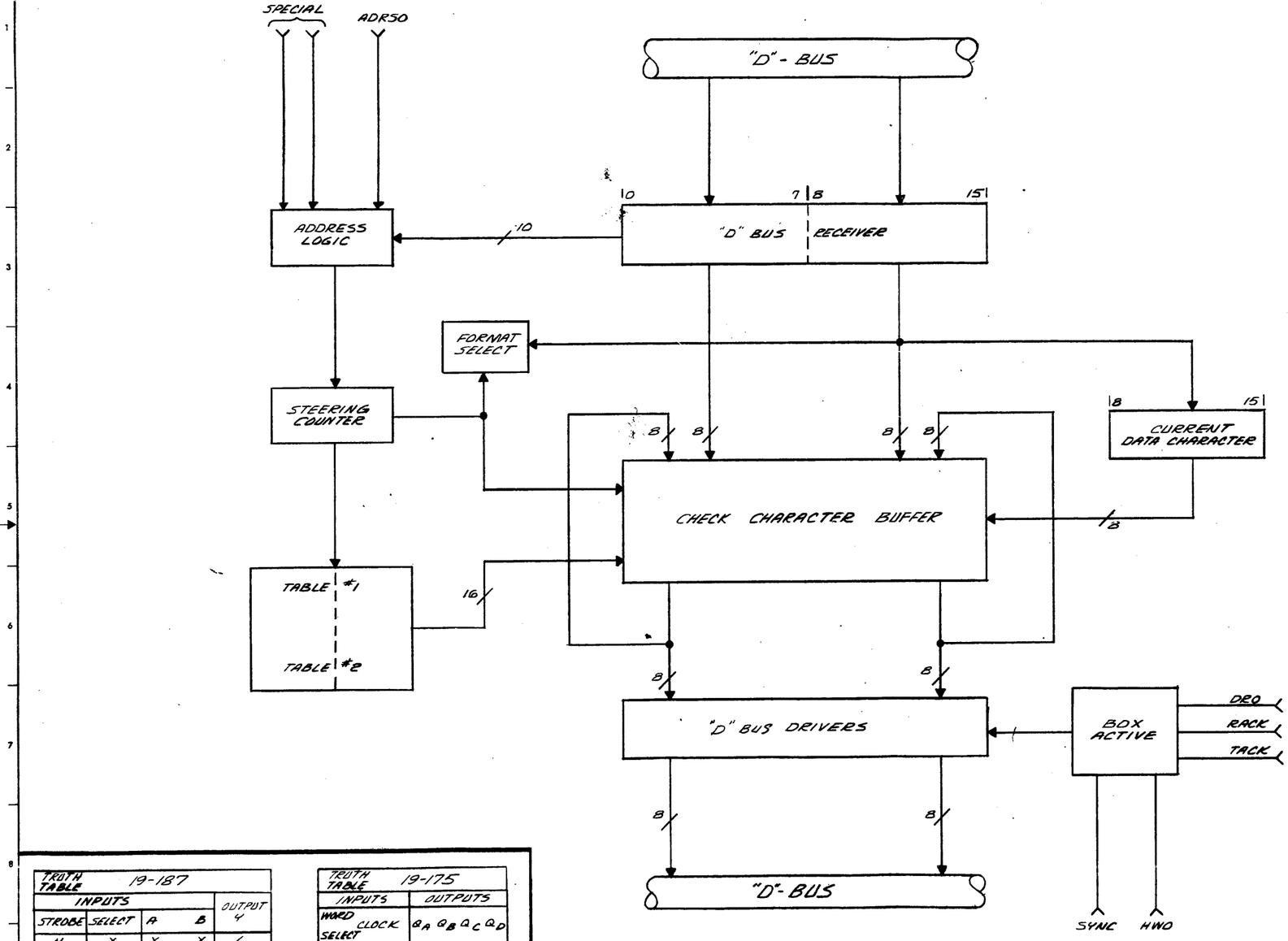
	NAME	TITLE	DATE
	J.R. BIELSKIE	DRAFT	11-1-79
	E. GREENSTEIN	SYS. TEST	5-13-80
	E. MARCH	ENGR	5-13-80
	R. BARKER	Q.C.	5-8-80
	D. FRANKENBERGER	MGR.	5-13-80

TITLE
FUNCTIONAL SCHEMATIC
TEST AID

DWG 03976
SIZE 35-734MØ1 DØ8
SHEET 1 OF 2

DRAWING 44231 24538


PERKIN-ELMER
REVISIONS
TITLE FUNCTIONAL SCHEMATIC TEST AID, D08
DWG 03905
PAT 35-734MOI D08
SHEET 2 OF 2
A14 19-177 LTTL 4 TO 1 MUX
A07 19-175 LTTL 2 TO 1 MUX
A15 19-175 LTTL 2 TO 1 MUX
A16 19-175 LTTL 2 TO 1 MUX
A17 19-177 LTTL 4 TO 1 MUX
A09 19-177 LTTL STB2 INPUT 2 MUX
A10 19-175 LTTL 2 TO 1 MUX
A01 19-177 LTTL 4 TO 1 MUX
A11 19-177 LTTL 4 TO 1 MUX
A12 19-177 LTTL 4 TO 1 MUX
A03 19-177 LTTL 4 TO 1 MUX
A13 19-177 LTTL 4 TO 1 MUX
A05 19-057 SG
A06 19-154 LG
A08 19-154 LG
A04 19-154 LG
A02 19-154 LG



TRUTH TABLE 19-187				
INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	H	X	L	L
L	H	X	H	H

H = HIGH LEVEL (STEADY STATE)
L = LOW LEVEL (STEADY STATE)
X = IRRELEVANT (ANY INPUT INCL TRANSITIONS)

TRUTH TABLE 19-175		
INPUTS		OUTPUTS
WORD SELECT	CLOCK	Q_A Q_B Q_C Q_D
L	↓	a_1 b_1 c_1 d_1
H	↓	a_2 b_2 c_2 d_2
X	H	Q_{A0} Q_{B0} Q_{C0} Q_{D0}

NOTES:
1. WHEN CONFIGURED ON DIOS PRIVATE BUS, ALL BACK PANEL CONNECTIONS ARE TO CONN-1 SIDE OF CHASSIS.

REVISION	5			2	1					
SHEET	1	2	3	4	5	6	7	8	9	10

DRAWING 44-231 24538

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Computer Systems Division
Oceanport, N.J. 07757

BACK PANEL MAP ROW 1	BACK PANEL MAP ROW 2	TERM. NO.	CONN
		41	
		40	
		39	
		38	
		37	
		36	
		35	
		34	
		33	
		32	
		31	
		30	
		29	
		28	
		27	
		26	
		25	
		24	
		23	
		22	
		21	
		20	
		19	
		18	
		17	
		16	
		15	
		14	
		13	
		12	
		11	
		10	
		09	
		08	
		07	
		06	
		05	
		04	
		03	
		02	
		01	
		00	
PS GND	GND GND	41	
		40	
		39	
		38	
		37	
		36	
		35	
BCNT0 (F00 ONLY)	BADR0 (F00 ONLY)	34	
		33	
		32	
		31	
		30	
		29	
		28	
	DCR0 (F00 ONLY)	27	
SCLR0	HWO	26	
PRACK0 (F01 ONLY)		25	
DBCNT0 (F01 ONLY)	CBIN0 (F01 ONLY)	24	
SYND		23	
ACR0	TACK0 (F00 ONLY)	22	
		21	
DR0	CMD0	20	
	ADRE0	19	
D140	D150	18	
D120	D130	17	
D100	D110	16	
D080	D090	15	
D060	D070	14	
D040	D050	13	
D020	D030	12	
D000	D010	11	
		10	
		09	
		08	
		07	
		06	
		05	
		04	
		03	
		02	
GND	GND	01	
PS	GND	00	

SEE NOTE 1

REVISIONS				
PRE PRODUCTION APPROVAL	INIT	DATE		
DEV		8-20-76		

REVISED SHT 5. 35-622 (BELOW) WAS R00

	3073	7-5-76	R01

REVISED SHTS 1, 4, & 5. 35-622 (BELOW) WAS R01.

	3073	9-20-76	R02

RELEASED FOR PRODUCTION
DATE

REVISED SHT 5. BOARD REV LEVEL WAS R02.

	3883	TAT	8-24-77	R03

ADDED NOTE 1 & USED IN MANUAL. BOARD REV WAS R03. REVISE SHTS 4 & 5. ADDED F00 & F01 ONLY TO BACK PANEL MAP. ALSO ON SHT 5 ADDED F00 & F01 VARIATIONS.

KR	3938	M	9-13-79	R04

AREA 59: DELETED 29-683 & ADDED 47-009 & 47-009 TO "USED IN MANUAL" AREA 58: 35-622 F01 WAS R01 & 35-622 WAS R05. REVISED SHTS 1 & 5.

MV	4683	MS	5-27-81	R05

USED IN MANUALS
29-519, 29-724, 29-695, 29-520, 47-004, 47-009

35-622	F01	R01
35-622		206
BOARD		REV LEVEL

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL.

SCALE —

TOLERANCE: XXX ± .005; XX ± .02; X ± .09; ANGLES ± 1°; UNLESS OTHERWISE SPECIFIED

	NAME	TITLE	DATE
	V. PERRI	DRAFT	1-30-76
	R. LEED	CHK	1-30-76
	G. JOYCE	ENGR	1-28-76
	R.A. JACKER		1-28-76
	S. MESSINA	MGR.	1-28-76

TITLE FUNCTIONAL SCHEMATIC COMM. MDM. ASSIST BD

SIZE	SYS NO.	SHEET OF
D	3073	1 – 5
	02-428-0508	

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

4H9 TDAT001 — A58 19-175 4B — C001
4H9 TDAT011 — A58 19-175 4A — C011
4J9 TDAT021 — A58 19-175 3B — C021
4J9 TDAT031 — A58 19-175 3A — C031
4R4 LRCENO — A58 19-175 S
4K9 TDAT041 — A49 19-175 4B — C041
4K9 TDAT051 — A49 19-175 4A — C051
4K9 TDAT061 — A49 19-175 3B — C061
4K9 TDAT071 — A49 19-175 3A — C071
5R2 ELRES1
5R2 LLRES1
3R9 LRESID1

R2 DD00 — A60 19-154 LG — A59 19-187 D1
R2 DD10 — A60 19-154 LG — A59 19-187 B2
R3 DD20 — A60 19-154 LG — A59 19-187 C1
R4 DD30 — A60 19-154 LG — A59 19-187 A2
R6 DD40 — A51 19-154 LG — A50 19-187 D2
E7 DD50 — A51 19-154 LG — A50 19-187 B2
5A8 DD61
R8 DD60 — A51 19-154 LG — A50 19-187 C2
5A9 DD71
E9 DD70 — A51 19-154 LG — A50 19-187 A2
A59 19-187 CLK, SEL; A50 19-187 CLK, SEL

A59 QD → A61 19-036 HPD → DD00 → 111-0, F1
A59 QB → A61 19-036 HPD → DD10 → 211-0, F2
A59 QC → A61 19-036 HPD → DD20 → 112-0, F3
A59 QA → A61 19-036 HPD → DD30 → 212-0, F4
A50 QD → A52 19-036 HPD → DD40 → 113-0, F6
A50 QB → A52 19-036 HPD → DD50 → 213-0, F7
A50 QC → A52 19-036 HPD → DD60 → 114-0, F8
A50 QA → A52 19-036 HPD → DD70 → 214-0, F8

RCD001 3A2
RCD011 3A2
RCD021 3A3
RCD031 3A4
ULCRCIA 5R8
RCD041 3A6
RCD051 3A7
RCD061 3A8
RCD071 3A8
ACCM0 3E9,5B1

RESIDUAL CHECK CHARACTER REGISTER HIGH

SCALE—	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	V. PERRI	DRAFT	1-21-76
		CHK	
		ENGR	

TITLE

TAPE NO. 03073
DWG NO. 02-928 D08
SHEET OF 2 — 5

BRUNING 44-231 24558

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

4B9 LRCD081
2R4 RCD001
4L9 TDAT081
4B9 LRCD091
2R4 RCD011
4M9 TDAT091
4C9 LRCD101
2R5 RCD021
4M9 TDAT101
4C9 LRCD111
2R5 RCD031
4M9 TDAT111
A40 19-172 LXR
A41 19-175
4R5 LRCENI
4E9 LRCD121
2R5 RCD041
4N9 TDAT121
4F9 LRCD131
2R5 RCD051
4N9 TDAT131
4F9 LRCD141
2R6 RCD061
4N9 TDAT141
4G9 LRCD151
2R6 RCD071
4E9 TDAT151
A31 19-172 LXR
A32 19-175
C081
C091
C101
C111
C121
C131
C141
C151
R2 D081
R3 D091
R3 D101
R4 D111
R6 D121
R7 D131
R8 D141
R9 D151
A42 19-187
A33 19-187
A44 19-036 MPD
A43 19-154 LG
A34 19-154 LG
A35 19-036 MPD
D080 <115-0
D081 H1, 4M1, 5B7
D090 <215-0
D091 H2, 4M1, 5B6
D100 <116-0
D101 H3, 4L1, 5B6
D110 <216-0
D111 H3, 4L1, 5B5
D120 <117-0
D121 H6, 4L1, 5B5
D130 <217-0
D131 H7, 4L1, 5B7
D140 <118-0
D141 H7, 4L1, 5B7
D150 <218-0
D151 H8, 4L1, 5B8
RCD081 4D9
RCD091 4D9
RCD101 4D9
RCD111 4D9
RCD121 4D9
RCD131 4D9
RCD141 4E9
RCD151 4E9
ACCMO 4E9
LRESIDI 2A9

RESIDUAL CHECK CHARACTER REGISTER LOW

SCALE—	NAME	TITLE	DATE	TITLE
TOLERANCE .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	V. PERRI	DRAFT	1-21-76	
		CHK		
		ENGR		

TASK NO. 03073 SHEET OF 3-5
DWG NO. 02-428 D08

DRAWING 44-231 24538

PERKIN ELMER

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Oceanport, N.J. 07757

REVISIONS				
AREA M4: ADDED K, L, M STRAP OPTION AND NOTE 1				
[illegible]	03073		4-20-76	R01
ADDED 3220 & 3240 PROCESSOR TO NOTE 1.				
KR	3938	M	9-9-79	R02

LDATA1 5R3 · LFMT1 5R1 · D15I 3R9 · D14I 3R8 · D13I 3R7 · D12I 3R6 · D11I 3R4 · D10I 3R3 · D09I 3R3 · D08I 3R2 · A0ES1 5D4 · LLCRI 5R7 · CLENTD 5B1

19-167 A37 HDFF

19-167 A28 HDFF

E9 1K · E10 1K · E4 1K · E1 6.8K · P5

00 = BISYNC (CRC-16)
10 = LRC
01 = SDLC

SEE NOTE 1

A48 DC 19-165 DS LSDF1 · A57 19-153 LSG · A6 19-042 EXC EXR

LRCEN0 2A5 · LRCEN1 3A5

A38 19-172 LSX · A29 19-172 LSX

3A1 LRCD08I · 3A2 LRCD09I · 3A3 LRCD10I · 3A3 LRCD11I · 3B4 LRCD08I · 3B5 LRCD09I · 3B5 LRCD10I · 3B5 LRCD11I · 3B5 LRCD12I · 3B5 LRCD13I · 3B5 LRCD14I · 3B5 LRCD15I · 3A6 LRCD12I · 3A7 LRCD13I · 3A7 LRCD14I · 3A7 LRCD15I · 3A8

CURRENT CHARACTER REGISTER

CRC TABLES FORMAT REGISTER

A56 19-195 F01 · A47 19-195 F02 · A39 19-195 F03 · A30 19-195 F04

2A1 TDAT00I · 2A2 TDAT01I · 2A3 TDAT02I · 2A3 TDAT03I · 2A6 TDAT04I · 2A7 TDAT05I · 2A7 TDAT06I · 2A8 TDAT07I · 3A2 TDAT08I · 3A2 TDAT09I · 3A3 TDAT10I · 3A4 TDAT11I · 3A6 TDAT12I · 3A7 TDAT13I · 3A8 TDAT14I · 3A8 TDAT15I

1. AS SHOWN IS STRAPPED FOR 7/320 PROCESSOR, 3220 PROCESSOR OR DIOS OPERATIONS (K TO L).
FOR 8/32 PROCESSOR OR 3240 PROCESSOR OPERATIONS REMOVE STRAP FROM K TO L AND ADD STRAP FROM K TO M.

SCALE—	NAME	TITLE	DATE	TITLE
TOLERANCE: .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED		DRAFT		
		CHK		
		ENGR		
				TASK NO. 03073
				DWG NO. 02-428 FORDOB
				SHEET OF 4—5

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
AREA B3: ADDED R11, R12, C50 & C51, AREA E8: DELETED R6 & C1. AREA D1&3: REMOVED 14 DECOUPLING CAPS. ADDED TP6 TO E. AREA I2 WAS SCLRO. A17-01 WAS ACCMO. A17-02 WAS CLRNTO				
JLV	03873		4-5-76	R01
AREA D4: ADDED ADRSI CROSS REF. AREA F6: CONNECTED A19-04 TO A19-01. A19-04 WAS TO A19-13.				
RC	03873		4-20-76	RC2
AREA F-5, ADDED SPARE GATE A21 PINS 3 & 4. A20 PIN 1 WAS TO A19 PIN 6.				
JLV	3883	M	3-19-79	R03
EXTENSIVE CHANGES IN AREAS B3-4, ADDED FOO & FOI VARIATIONS. SEE MICRO FILM REV R03 FOR PREVIOUS CHANGES.				
KR	3938	M	9-13-79	R04
AREA F6 ADDED A11, A20-02 WAS TO A19-03				
JLV	4683	MS	5-27-81	R05

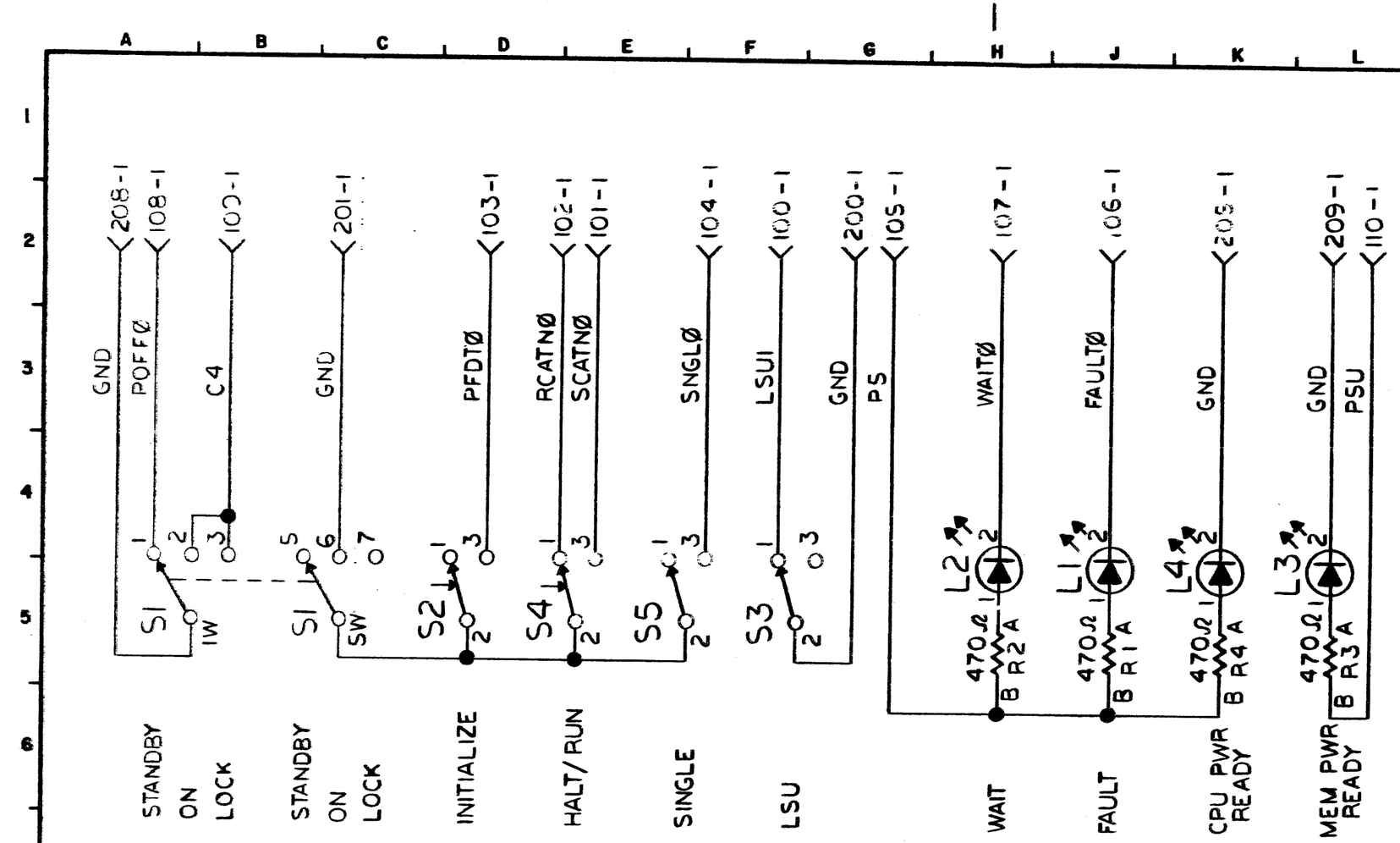
TIMING & CONTROL

NOTES:
1. WHEN USED ON A 7/32C PROCESSOR 3220 PROCESSOR DRDIOS 'TP4' MUST BE STRAPPED TO GROUND. WHEN USED ON AN 8/32 PROCESSOR OR 3240 PROCESSOR 'TP6' MUST BE STRAPPED TO GROUND.
2. WHEN USED ON A 7/32C PROCESSOR OR 3220 PROCESSOR 'G' MUST BE STRAPPED TO 'J' AS SHOWN. WHEN USED ON AN 8/32 PROCESSOR 3220 PROCESSOR OR DIOS 'G' MUST BE STRAPPED TO 'H'.

DECOUPLING CAPACITORS

SCALE —	NAME	TITLE	DATE	TITLE
TOLERANCE .XX ± .005, .X ± .02, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		DRAFT		
		CHK		
		ENGR		

TABS NO. 03073 SHEET 5 OF 5
DWG NO. 02-[illegible]005 DOB



REVISIONS		
	INIT	DATE
PRODUCTION APPROVAL	DEV	

RELEASED FOR PRODUCTION
DEV ENG. DATE

USED IN MANUAL - 71 022

NOTES

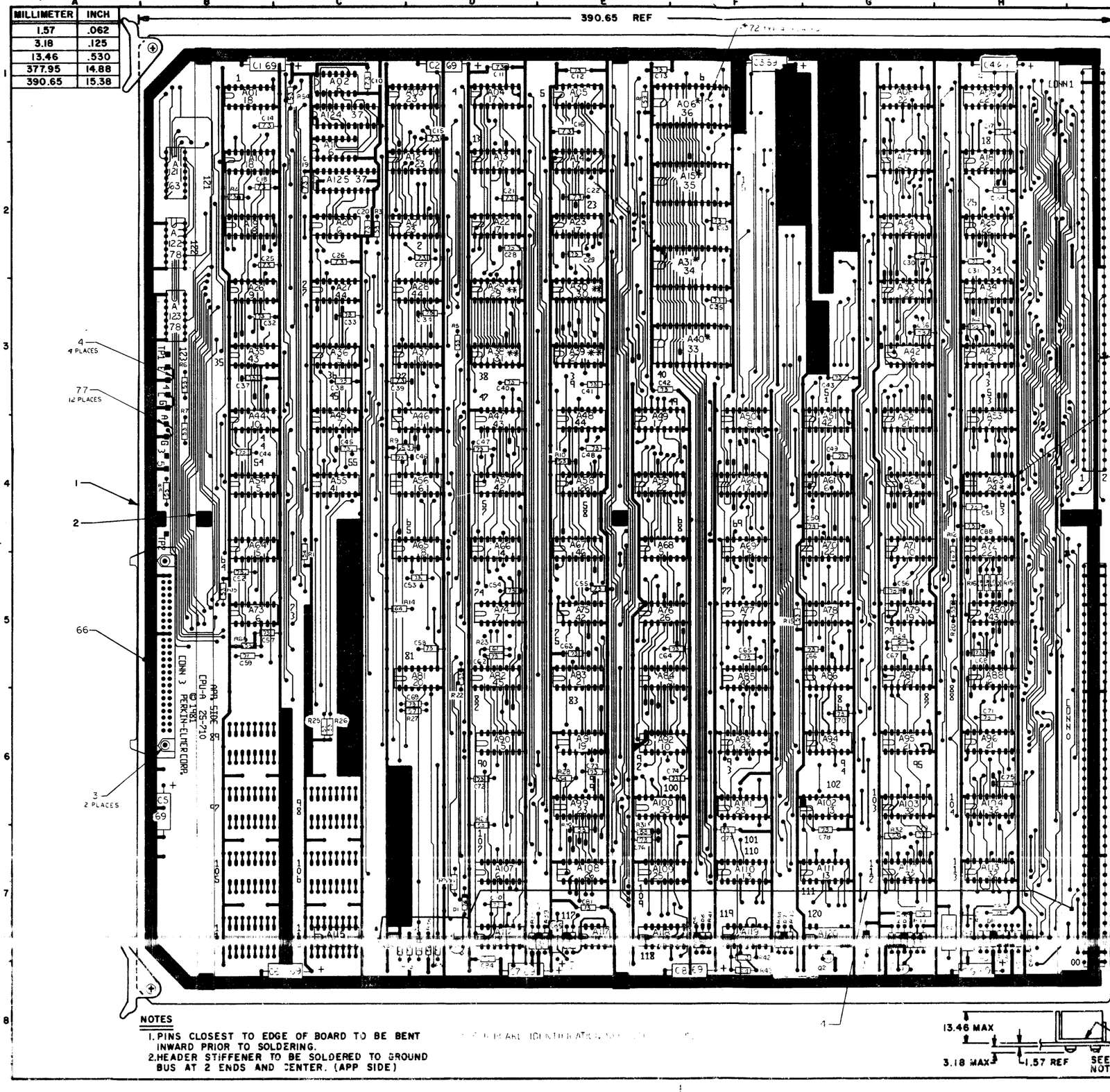
UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ± .005 .X ± .03 .XX ± .02 ANGLES ± 1°	
NAME	TITLE	DATE
J. TAMUL	DES / DFT	1-21-81
B. CERO	SUPV	2 15 81
	CHK	
D. FOGGIA	ENG	2 - 81
P. ABITANTE	MGR	2 - 81
R. BARKER	QC	2 - 81

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE
SCHEMATIC
CONTROL PANEL

TASK 03175
DWG 09-140 B08
SHT 1-1

MILLIMETER	INCH
1.57	.062
3.18	.125
13.46	.530
377.95	14.88
390.65	15.38



NOTES

1. PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.
2. HEADER STIFFENER TO BE SOLDERED TO GROUND BUS AT 2 ENDS AND CENTER. (APP SIDE)

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	
	PROD	

IN ITEM 14 A15 ITEM 3 WAS NOT SPEC. IT WAS TO BE A FLAT ITEM 77 WAS SPEC AS PLATE.

VT	ENG	4373	M	3-11-82	R01

RELEASED FOR PRODUCTION
MFG. ENG. _____ DATE 11/6/81

ADDED C87 TO AREA H7

VT		4373	M	3-23-82	R02

USED IN MANUAL 47-022

CKT.BREAKER	A120
RES.MODULE	A121
RESISTOR	R1-R54
SWITCH	A122, A123
TRANSISTOR	Q1-Q3
DIODE	D1-D13
CAPACITOR	C1-C59, C62-C89
INTEGRATED CIRCUIT	A01-A06, A08-A15, A17-A31, A33-A40, A42-A88, A90-A96, A98-A104, A107-A113, A115-A119, A124, A125
COMPONENT	REF DESIGNATION

UNLESS OTHERWISE SPECIFIED

SCALE: 2/1

TOLERANCE: .XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

DIMENSIONS ARE IN INCHES

NAME		TITLE	DATE
V. PERRI	H. NGUYEN	DES/DFT	11-6-81
R. CEHO		SUPV	11-6-81
		CHK	
M. MANGIONE		ENG	11-6-81
F. OBRDA		MGR	11-6-81
R.A. BARKER		QC	11-6-81

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Oceanport, N.J. 07757

TITLE
ASSEMBLY
PRINTED CIRCUIT BOARD
CPU-A

TASK 68179	SHT
DWG 35-216 R02 ECR	1 of 1

MILLIMETER	INCH
1.57	.062
3.18	.125
13.46	.530
377.95	14.880
390.65	15.380

390.65

377.95

REVISIONS

PRE PRODUCTION APPROVAL	DEPT.	DATE	
	PROD.		

RELEASED FOR PRODUCTION
MFG ENG. DATE 7-2-80
REV. A LOC 11 NOB -11 MIS
WAS ITEM 40.
KR | 4960 | R | H-1381 | RD1

CONN 8 CONN 5 CONN 4 CONN 3 CONN 2 CONN 6 CONN 7 CONN 1 CONN 0

CPU-B

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25 660 ROWS APP SIDE 35-768 ROWS

ITEM 50 (TYP. 2 PLCS)

ITEM 3 (TYP. 4 PLCS)

ADD APPROPRIATE REV. LEVEL IDENTICAL TO REV LEVEL OF PARTS LIST TO WHICH BOARD WAS BUILT.

TYP 119 PLCS ITEM 46

TYP 10 PLCS ITEM 45

NOTES:
1. FOR MOUNTING OF STANDARD HARDWARE SEE 16-696 SHT.
2. BEVEL PINS CLOSEST TO EDGE OF BOARD AWARD RIBBON TO FACILITATE.
3. ALL DIMENSIONS ARE IN MILLIMETERS.

USED IN ASSEMBLY 47-004

13.46 MAX.
1.57 REF.
3.18 MAX.

PARTIAL VIEW A-A
TYPICAL 3 PLACES

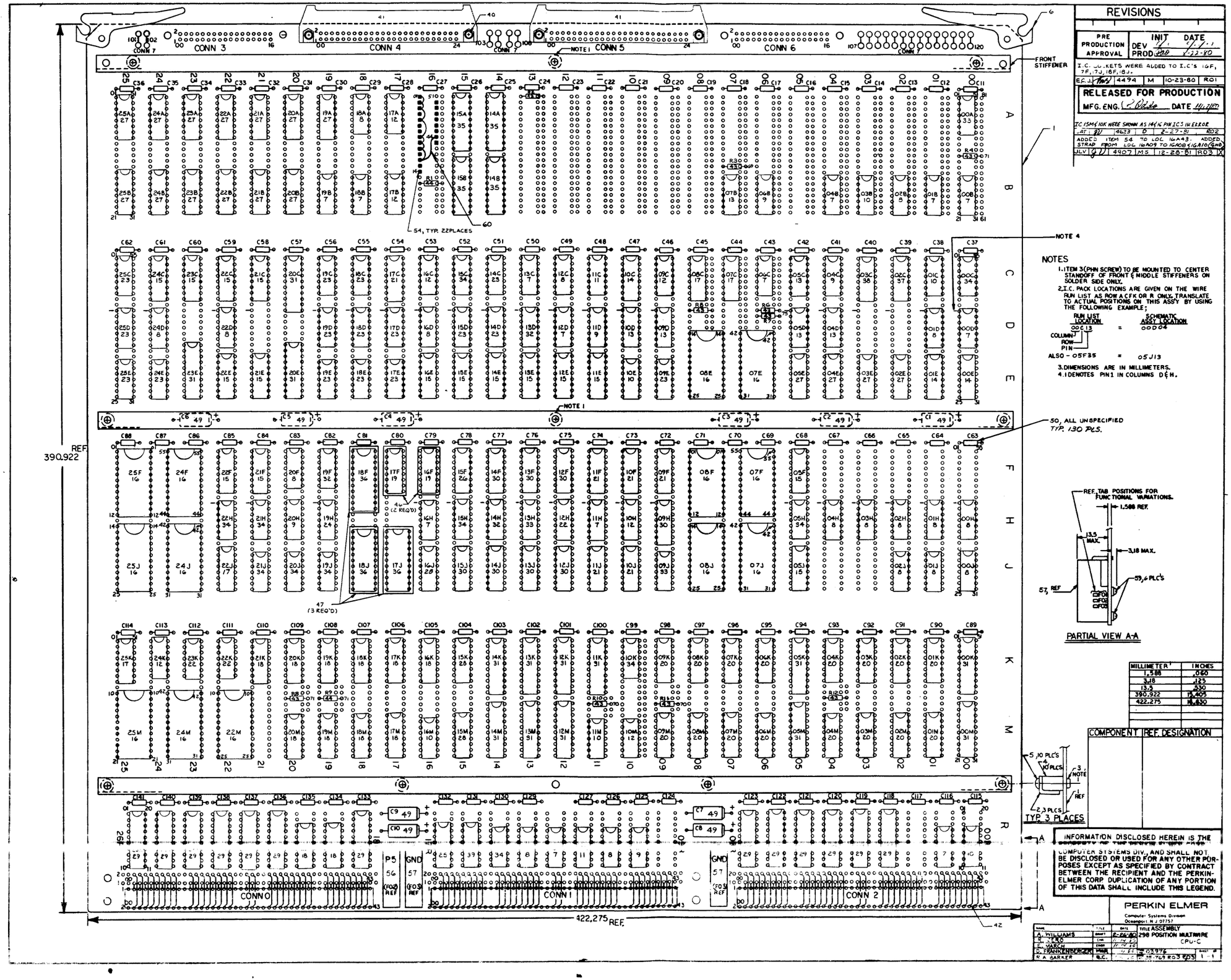
METRIC

COMPONENT REF DESIGNATION

PERKIN ELMER
Computer Systems Division
Oceanport, N J 07757

PIN CONFIGURATION I.C. LOCATION FOR ROWS 02, 05, 11, & 14

DRAWN	DATE	TITLE: CPU-B ASSEMBLY	
CHECKED			
ENGR			
P.D. BARELLE	7/2	47-039	
QUALITY ASSURANCE		16-8801603	SHEET 1 OF 1



REVISIONS

	INIT	DATE
PRE PRODUCTION APPROVAL	DEV	
	PROD	

I.C. SOCKETS WERE ADDED TO I.C.'S 16F, 7F, 7J, 16F, 18J.

E.C.J.	MW	4494	M	10-23-80	R01

RELEASED FOR PRODUCTION

MFG. ENG. [illegible] DATE 11-7-80

IC 15M & 10K WERE SHOWN AS 14/16 PIN IC'S IN ERROR

AT	BW	4633	0	2-27-81	802

ADDED ITEM 54 TO LOC 16A43. ADDED STRAP FROM LOC 16A09 TO IGA08 & IGA10 (GND)

JLV	GW	4907	MS	12-28-81	R03

NOTES

1. ITEM 3 (PHN SCREW) TO BE MOUNTED TO CENTER STANDOFF OF FRONT & MIDDLE STIFFENERS ON SOLDER SIDE ONLY.
2. I.C. PACK LOCATIONS ARE GIVEN ON THE WIRE RUN LIST AS ROW A CFK OR R ONLY. TRANSLATE TO ACTUAL POSITIONS ON THIS ASSY BY USING THE FOLLOWING EXAMPLE;

RUN LIST LOCATION		SCHEMATIC ASSY LOCATION
00C13	=	00D04

COLUMN J
ROW
PIN

ALSO - 05F35 = 05J13

3. DIMENSIONS ARE IN MILLIMETERS.
4. 1 DENOTES PIN 1 IN COLUMNS D & H.

PARTIAL VIEW A-A

MILLIMETER	INCHES
1.588	.060
3.18	.125
13.5	.530
390.922	15.405
422.275	16.630

COMPONENT	REF. DESIGNATION

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

NAME	TITLE	DATE	TITLE ASSEMBLY
A. WILLIAMS	DRAFT	5-26-80	298 POSITION MULTIWIRE
R. [illegible]	ENG	11-14-80	CPU-C
E. MARCH	ENG	11-14-80	
D. FRANKENBERGER	MFG	11-14-80	SIZE C 05976 SHEET 1 1
W. A. BARKER	Q.C.		SCALE 1:1.769 R03 MDS

CONN 7 CONN 3 CONN 4 CONN 5 CONN 6 CONN 1 CONN 2

NOTE 1

FRONT STIFFENER

REF 390.922

422.275 REF.

CONN 0 CONN 1 CONN 2

P5 GND GND

NOTE 4

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	
	PROD	

ADDED ITEM 70 IN POSITIONS 05C, 05F, 08S & 08T. ITEM 7 ON TEST PANELS. W.O. WAS NOT SPEC. 7.9 W/ SEQUENCING. ADDED CONNECTOR BETWEEN CONNECTOR 1 & 2. DELETED 3 NO-FUNCTION 3 HOLES TO MAKE IT A SOLID UNIT.

4.1"	JH	4527	M	12-29-80	R01

RELEASED FOR PRODUCTION

ENG. _____ DATE _____

ADD		TRW-71 ACROSS UNUSED SOCKETS			
0-0123		14-24 AWG			
JH	JH	4657	M	3-25-81	R02
ECS AT		TRW-71 WAS 2.49.			
KE	JH	4706	M	12-16-81	R03
ADDED		1.1.			
KE		4827		11-24-82	ECP-1124
ADD	JH	"	M	11-24-82	1249

NOTES

1. ITEM 3 (PHN SCREW) TO BE MOUNTED TO CENTER STANDOFF OF FRONT & MIDDLE STIFFENERS ON SOLDER SIDE ONLY.
2. I.C. PACK LOCATIONS ARE GIVEN ON THE WIRE RUN LIST AS ROW A,C,F,K OR R ONLY. TRANSLATE TO ACTUAL POSITIONS ON THIS ASS'Y BY USING THE FOLLOWING EXAMPLE:

RUN LIST LOCATION		SCHEMATIC ASSY LOCATION
COLUMN	=	
ROW		
PIN		
ALSO -	=	

3. DIMENSIONS ARE IN MILLIMETERS.
4. ▯ DENOTES PIN 1 IN COLUMNS D & H.

SQ. ALL UNSPECIFIED

REF. TAB POSITIONS FOR FUNCTIONAL VARIATIONS.

1.588 REF

13.5 MAX.

3.18 MAX.

5, 8 PLC'S

REF

PARTIAL VIEW A-A

MILLIMETER	INCHES
1.588	.060
3.18	.125
13.5	.530
390.922	15.405
422.275	16.630

COMPONENT	REF. DESIGNATION

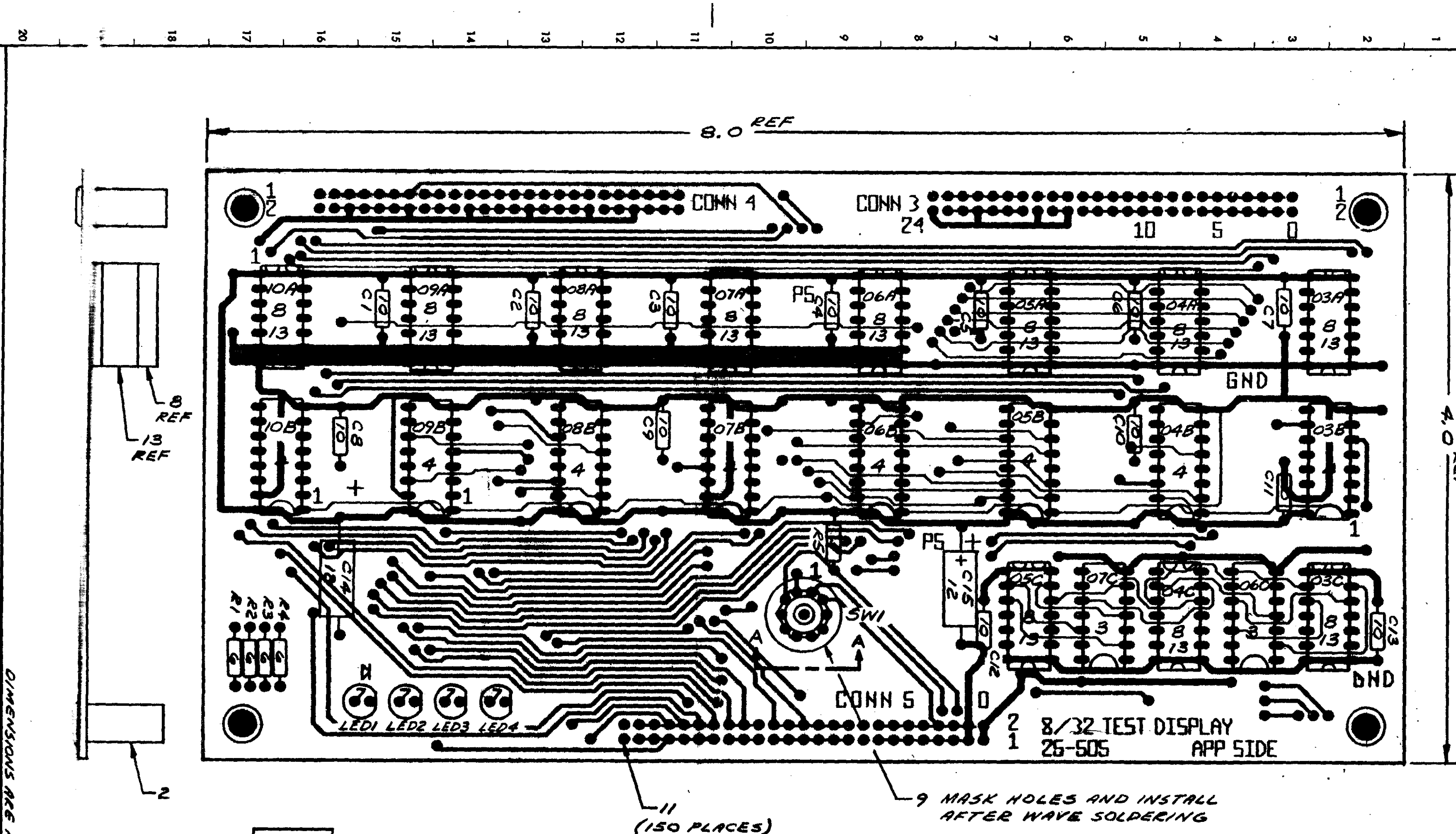
4, 10 PLC'S
10 PLCS
93 PLCS
TYP 3 PLACES
NOTE 1
REF

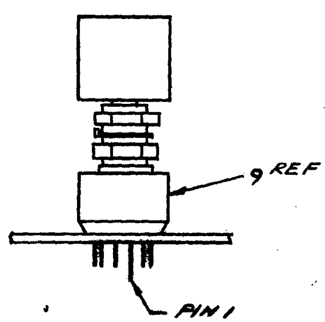
PERKIN ELMER

Oceanport, N.J. 07757

C. JOHNSON	DRAFT	7-6-82	TITLE ASSEMBLY 298 POSITION MULTIWIRE
P. BALAS	ENGR	11-4-80	SIZE CPU-D
D. FENDERBACK	MGR	11-4-80	DWG. NO. 03276
P. BARKER	QC	11-4-80	SCALE 25-775 REV 03

USED IN MANUAL 47-504





VIEW A-A
PINS OF SWITCH (ITEM 9) ARE SHOWN BEFORE CLINCHING, FOR REF ONLY.

DIMENSIONS ARE IN INCHES

SCALE–2:1

NAME	TITLE	DATE
H. MATTER	DRAFT	3-3-76
	CHK	3-30-76
T. FYFE	ENGR	3-30-76
R. A. BAKKER	QC	3-30-76
S. MESSINA	MGR	3-30-76

TITLE
ASSEMBLY
8/32 TEST DISPLAY

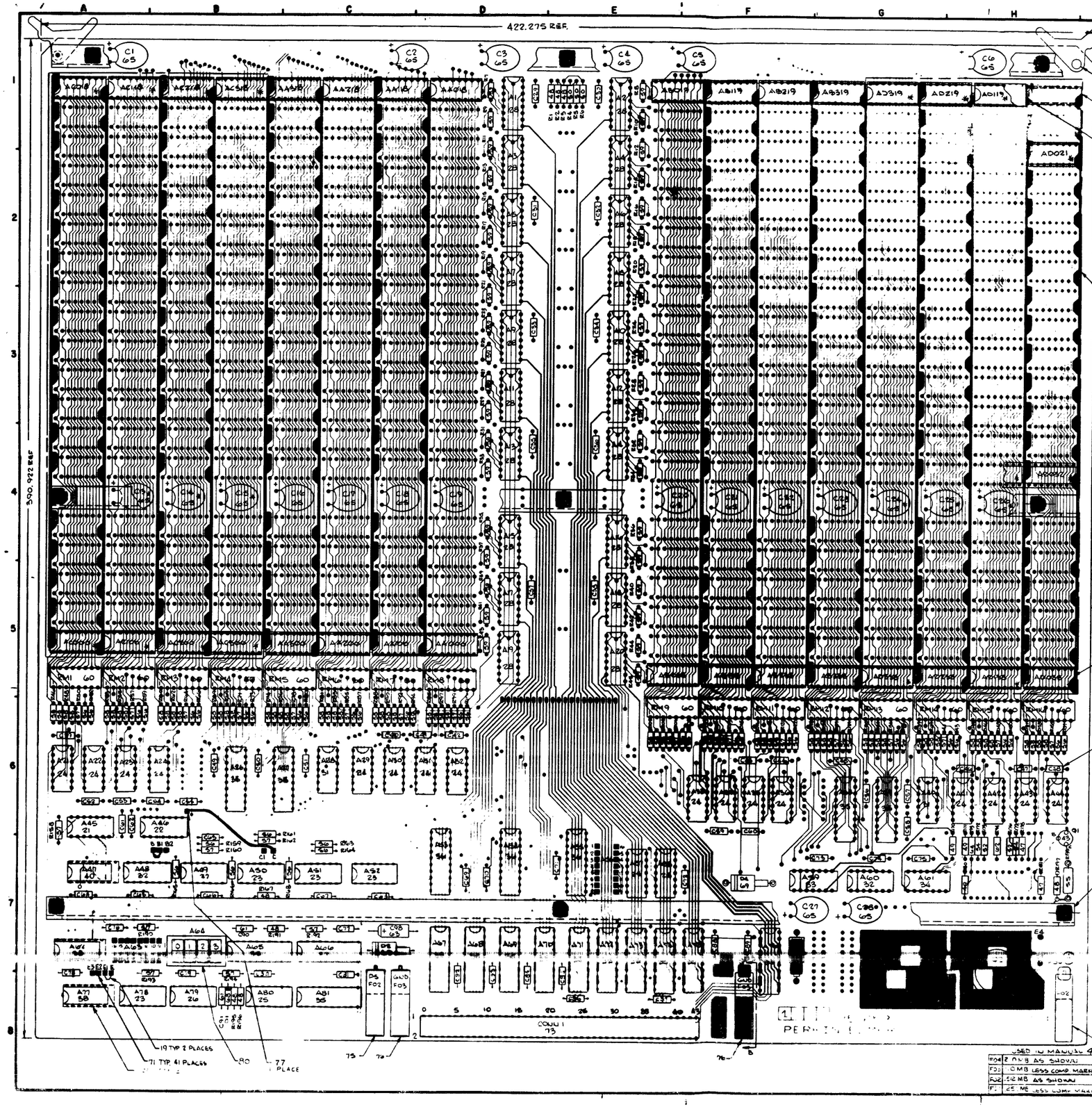
TAB NO. 03071
DWG NO. 35-612 R01 C03
SHEET 1 OF 1

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.

REVISIONS

PRE PRODUCTION APPROVAL			INIT	DATE
REDRAWN TO AGREE WITH 25-505 R01 C05				
	QE 3071-01	[illegible]	3-3-76	R01

RELEASED FOR PRODUCTION
MFG. ENG. [illegible] DATE 3/31/76



MILLIMETERS	INCHES
1.588	.060
3.18	.125
13.494	.530
390.922	15.405
422.275	16.650

METRIC

REVISIONS

	INIT	DATE
PRE PRODUCTION APPROVAL	DEV	
	PROD	

RELEASED FOR PRODUCTION

MFG. ENG. _____ DATE _____

NOTES -

1. TEM 9 (PUH SCREW) TO BE MOUUTED WITH CENTER STANDOFF OF STIFFENERS ON SOLDER SIDE. (9 PLACES)
2. ON FO3 AND FO4 VARIATIONS ALL HOLES FOR MOUNTING ITEM 72 I.C. SOCKETS (IDENTIFIED WITH AN ASTERISK (*)) MUST BE FREE OF SOLDER, EXCEPT HOLES MOUNTING ITEM 17 CAPACITOR STRIP. TYPICAL 156 PLACES
3. IC'S (TYP 3 PLCS) AA7, AL2 CA77: DASHED LINES REPRESENT ALTERNATE MTG. 14-PIN DIP (16 PIN NOTE THAT IC'S SHOWN (16 PIN) IS LEFT JUSTIFIED.

RESISTOR	R1-R168, R170-R173, R176, R177, R178 R180, R189-R198
TRANSISTOR	Q1, Q2,
DIODE	D1-D4
CAPACITOR	C1-C6, C13-C91, C93, C94, C98
SWITCH	A64
INTEGRATED CIRCUIT	A1-A24, A26-A36, A38-A55, A57-A62, AA000-AD558, A65-A81
RESISTOR MODULE DIP	RM1 THRU RM16

COMPONENT	REF DESIGNATION

UNLESS OTHERWISE SPECIFIED

SCALE: 2/1

TOLERANCE:

DIMENSIONS ARE IN MILLIMETERS

.XX ±.13 X±.8

.X ±.5 ANGLES ±1°

NAME		TITLE	DATE
G. SHINU	G. SHINU	DES/DFT	1-2-80
W. LIMPERT/R. CERO		SUPV	10-16-81
W. LIMPERT		CHK	10-16-81
P. OBEDA		ENG	10-16-81
D. FRANKENBERGER		MGR	10-16-81
R. BARKER		QC	10-16-81

PERKIN-ELMER

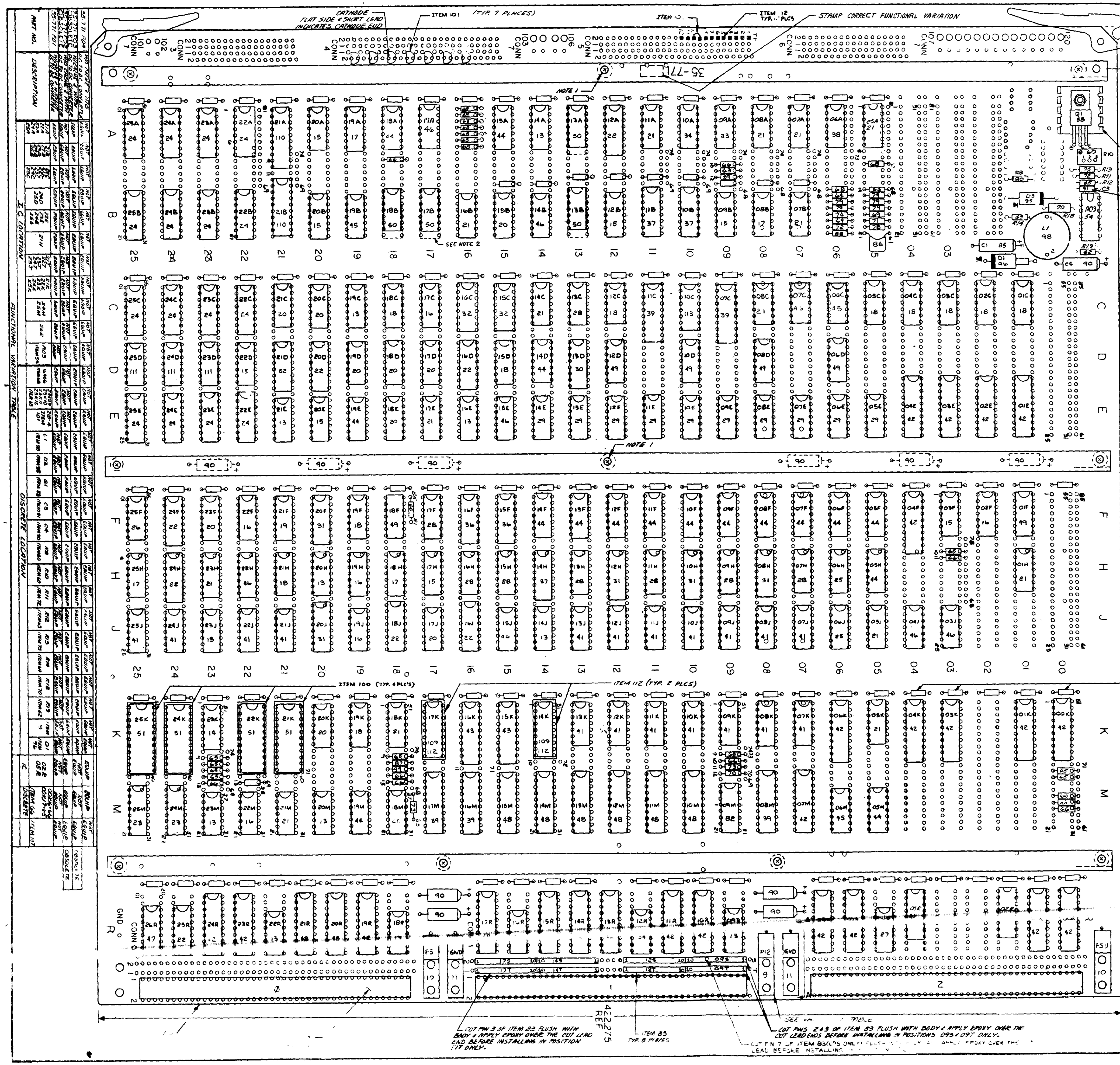
Computer Systems Division
Oceanport, N.J. 07757

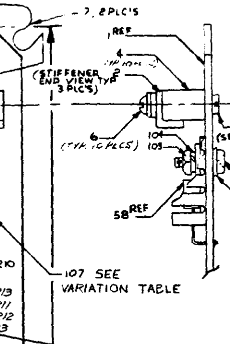
TITLE
ASSEMBLY PRINTED CIRCUIT BOARD
2.0MB STORAGE MODULE

TASK 03979

DWG 35-7164 R01 E03

SHT 1 - 1





PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

IC LOCATIONS 13A, 13B, 17B & 18B WERE 19-249 FAX. NOTE 3 WAS NOTE 2. ADDED NEW NOTE 2.

IC 18M WAS ITEM 25 (19-082). RESISTOR 18K AT PIN 63 WAS LABELED 33; THIS RESISTOR WAS ITEM 65. MADE F02 & F03 VERSION OBSOLETE.

REMOVED 21D FROM FUNCTIONAL VARIATION TABLE

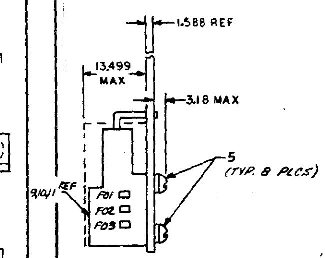
RELEASED FOR PRODUCTION

NOTES:

1. ITEM 3 (PHN SCREW) TO BE MOUNTED INTO CENTER STANDOFFS OF FRONT & MIDDLE STIFFENERS ON SOLDER SIDE ONLY.
2. IC LOCATIONS (TYP 4 PLACES) 13A, 13B, 17B & 18B DASHED LINES REPRESENT ALTERNATE USE OF 19-249FAX.
3. I.C PACK LOCATION ARE GIVEN IN THIS LIST AS ROW A, C, F, K, OR R ONLY. TO FIND ACTUAL LOCATION ON ASS'Y DWG 35-771 F03 SCHEMATIC, USE THE FOLLOWING EXAMPLES;

RUN LIST LOCATION		SCHEMATIC & ASSY LOCATION
00F13	=	00H04
ALSO		
03K32	=	03M10

(00H04: COLUMN, ROW, PIN NUMBER)



PARTIAL VIEW A-A

MILLIMETERS	INCHES
1.588	.060
3.18	.125
13.499	.530
390.922	15.390
422.275	16.630

METRIC

PERKIN-ELMER
Computer Systems Division
Oceanport, N J 07757

NAME	TITLE	DATE
J. PEER	DES DFT	11-14-80
R CEBO	SUPV	11-14-80
R.C.	CHK	11-14-80
S. AGRAWAL	ENG	11-14-80
D. FRANKENBERGER	MGR	11-14-80
P.A. BARKER	QC	11-14-80

ASSEMBLY LOCAL BANK CONTROLLER

DWG 35-771 R07 F03 SHT 1-1

PERKIN ELMER

Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

PRE PRODUCTION APPROVAL	DEV PROD	INIT	DATE

RELEASED FOR PRODUCTION

MFG ENG. ____ DATE ____

REMOVED 31D FROM FUNCTIONAL VARIATION TABLE

VT W 4597 MS 2-5-81 ROZ

ITEM 3 (PHN SCREW) TO BE MOUNTED INTO CENTER STANDOFFS OF FRONT (MIDDLE STIFFENERS ON SOLDER SIDE ONLY.

I.C LOCATIONS (TYP. 4 PLACES) 13A, 12B, 17B/18B DASHED LINES REPRESENT ALTERNATE USE OF 19 249 FAX.

2. I.C PACK LOCATION ARE GIVEN IN THIS LIST AS ROW A,C,F,H, OR K ONLY. TO FIND ACTUAL LOCATION ON ASS'Y DWG 35-771, (593) SCHEMATIC, USE THE FOLLOWING EXAMPLES;

RUN LIST LOCATION		SCHEMATIC & ASSY LOCATION
00F13	=	00H04 (PIN NUMBER, ROW, COLUMN)
ALSO		
03K32	=	03M10

NOTES:

1. ITEM 3 (PHN SCREW) TO BE MOUNTED INTO CENTER STANDOFFS OF FRONT (MIDDLE STIFFENERS ON SOLDER SIDE ONLY.
   I.C LOCATIONS (TYP. 4 PLACES) 13A, 12B, 17B/18B DASHED LINES REPRESENT ALTERNATE USE OF 19 249 FAX.
2. I.C PACK LOCATION ARE GIVEN IN THIS LIST AS ROW A,C,F,H, OR K ONLY. TO FIND ACTUAL LOCATION ON ASS'Y DWG 35-771, (593) SCHEMATIC, USE THE FOLLOWING EXAMPLES;

RUN LIST LOCATION		SCHEMATIC & ASSY LOCATION
00F13	=	00H04 (PIN NUMBER, ROW, COLUMN)
ALSO		
03K32	=	03M10

IC 18M WAS ITEM 25 (19-082) RESISTOR 18K AT-PN 63 WAS LABELED 33; THIS RESISTOR WAS ITEM 65. MADE FOR E.FOS VERSION OBSOLETE

J.W 4891 MS 11-9-81 ROZ

IC LOCATIONS 13A, 15B, 17B/18B WERE 19 249 FAX. NOTE 3 WAS NOTE 2. ADDED NEW NOTE 3

KC 4892 11-28-81 ROZ

METRIC

USED IN MANUAL 17-011

ITEM 100 (TYP. 4 PLCS)

ITEM 112 (TYP. 2 PLCS)

ITEM 91 (ALL UNSPECIFIED) TYP. 134 PLCS LESS C3.

CATHODE FLAT SIDE / SHORT LEAD INDICATES CATHODE END

ITEM 101 (TYP. 7 PLACES)

ITEM 10 TYP. 11 PLCS

STAMP CORRECT FUNCTIONAL VARIATION

7 EPLC'S

(STIFFENER END VIEW TYP. 3 PLCS)

107 SEE VARIATION TABLE

SEE VARIATION TABLE

NOTE 1

SEE NOTE 2

CUT PIN 3 OF ITEM 83 FLUSH WITH BODY & APPLY EPOXY OVER THE CUT LEAD END BEFORE INSTALLING IN POSITION 17 ONLY.

ITEM 83 TYP. 8 PLACES

CUT PINS 2 & 3 OF ITEM 83 FLUSH WITH BODY & APPLY EPOXY OVER THE CUT LEAD ENDS BEFORE INSTALLING IN POSITIONS 09 & 10 ONLY.

CUT PIN 2 OF ITEM 83 FLUSH WITH BODY & APPLY EPOXY OVER THE LEAD BEFORE INSTALLING IN POSITION 11 ONLY.

422.275 REF

390.922 REF

1.588 REF

13.499 MAX

3.18 MAX

5 (TYP. 8 PLCS)

PARTIAL VIEW A-A

MILLIMETERS	INCHES
1.588	.060
3.18	.125
13.499	.530
390.922	15.390
422.275	16.630

I.C LOCATION

FUNCTIONAL VARIATION TABLE

DISCRETE LOCATION

PART NO.	DESCRIPTION	
35-771-001	PWB ASSY, MEMORY CONTROLLER	
35-771-101	PWB ASSY, MEMORY CONTROLLER	

OBSOLETE

OBSOLETE

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

ASSEMBLY
LOCAL BANK CONTROLLER

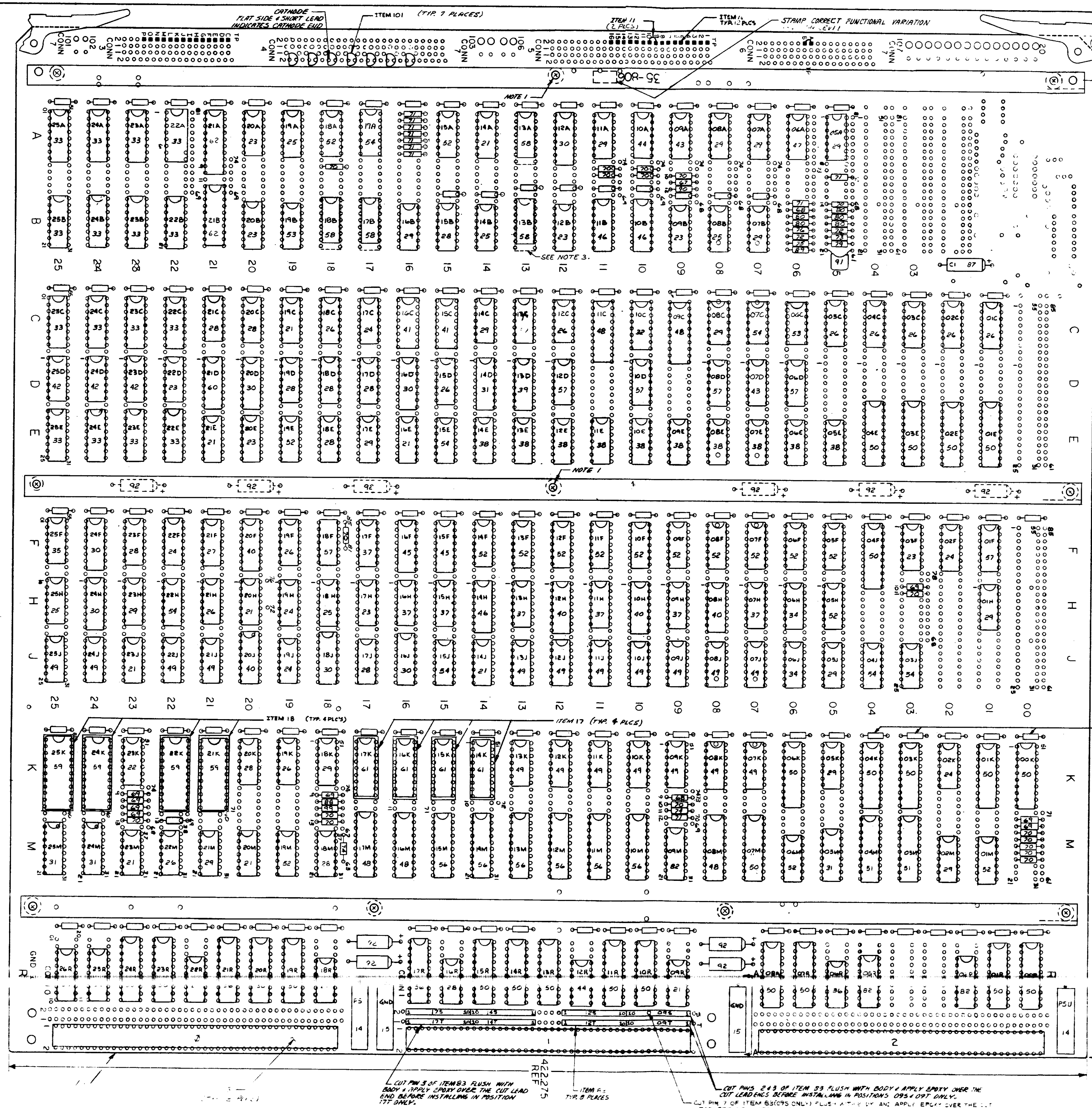
NAME	TITLE	DATE
L. FREEL	DES	11-14-80
R. CERBO	SUPV	11-18-80
R. KO	CHK	11-19-80
S. KASHMAR	ENG	11-19-80
D. SCHULLENBERGER	MFR	11-19-80
R.A. [illegible]	QC	11-19-80

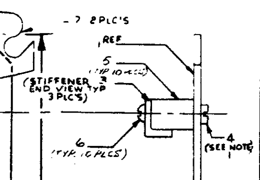
TASK 35-771 DWG 35-771 REV [illegible] SHT 1 OF 1

PART NO.	DESCRIPTION	21A 22A 23A 24A 25A	21B 22B 23B 24B 25B	21C 22C 23C 24C 25C	24D 25D	22E 23E 24E 25E	21H	21J 22J 23J 24J 25J	21K 22K 23K 24K 25K	24M 25M	26R	02R 05R	23K09 23K10 23K11 23K12 ITEM 69	21B-4 ITEM 101	16R06 ITEM 71	00K65 00K66 ITEM 70
35-806 F02	W/O CACHE	NOT EQUIP	NOT EQUIP	NOT EQUIP	NOT EQUIP	NOT EQUIP	NOT EQUIP	NOT EQUIP	NOT EQUIP	NOT EQUIP	NOT EQUIP	EQUIP	NOT EQUIP	NOT EQUIP	NOT EQUIP	EQUIP
35-806 F01	W/ CACHE	EQUIP	EQUIP	EQUIP	EQUIP	EQUIP	EQUIP	EQUIP	EQUIP	EQUIP	EQUIP	NOT EQUIP	EQUIP	EQUIP	EQUIP	NOT EQUIP

I.C. LOCATION — DISC. LOCATION

FUNCTIONAL VARIATION TABLE





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REVISIONS

AT LOC 01M ITEM 52 WAS NOT SPEC. ... ITEM 76 ... NOT SPEC. AT LOC 18K65 ITEM 69 WAS SHOWN AS AN ITEM 70. IN FUNCTIONAL VARIATION TABLE FOR F02 VARIATION 21D WAS DELETED FROM NOT EQUIPPED COLUMN.

DS	11-4763		8-20-81	R01

RELEASED FOR PRODUCTION

IC 18M WAS ITEM 34 ECS AT 18K63 TO 18K67 WAS ITEM 69. MANUAL LISTED WAS 47-004.

	4909	MS	-9-82	E03

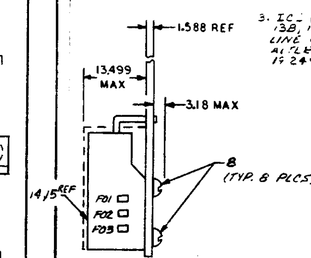
NOTES:

1. ITEM 4 (PHN SCREW) TO BE MOUNTED INTO CENTER STANDOFFS OF FRONT (MIDDLE STIFFENERS ON SOLDER SIDE ONLY.
2. I.C PACK LOCATION ARE GIVEN IN THIS LIST AS ROW A,C,F,K, OR R ONLY. TO FIND ACTUAL LOCATION ON ASS'Y DWG 35-806 E03 SCHEMATIC, USE THE FOLLOWING EXAMPLES;

RUN LIST LOCATION		SCHEMATIC & ASSY LOCATION
00F13	=	00H04
ALSO		
03K32	=	03M10

(00H04: PIN NUMBER, ROW, COLUMN)

3. IC'S (TYP 4 PLCS) 13A, 13B, 17B & 18B DASHED LINE REPRESENTS ALTERNATE USE OF P/N 19 249 F02.



PARTIAL VIEW A-A

MILLIMETERS	INCHES
1.588	.060
3.18	.125
13.499	.530
390.922	15.390
422.275	16.630

TOLERANCE IN MILLIMETERS
.X ± .8
.X ± .5
.XX ± .13
UNLESS OTHERWISE SPECIFIED

METRIC

USED IN MANUAL 47-022

NAME	TITLE	DATE
Q.STINE Q.STINE	DES / DFT	1-19-81
R.CERO	SUPV	9-11-81
	CHK	
M.MONGIONE	ENG	9-11-81
P.OBRCA	MGR	9-11-81
R.BLA...	QC	9-11-81

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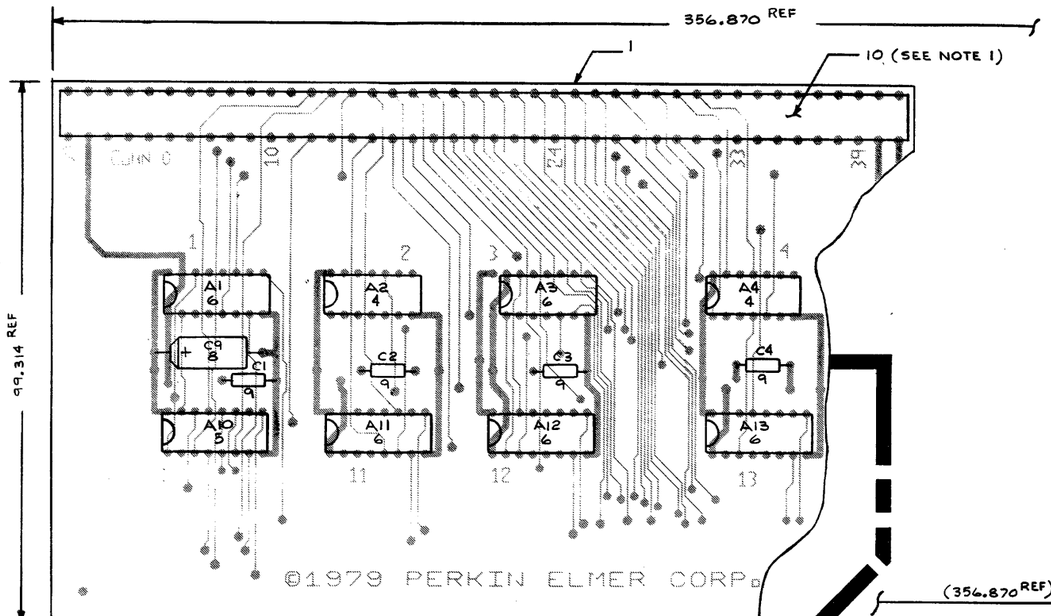
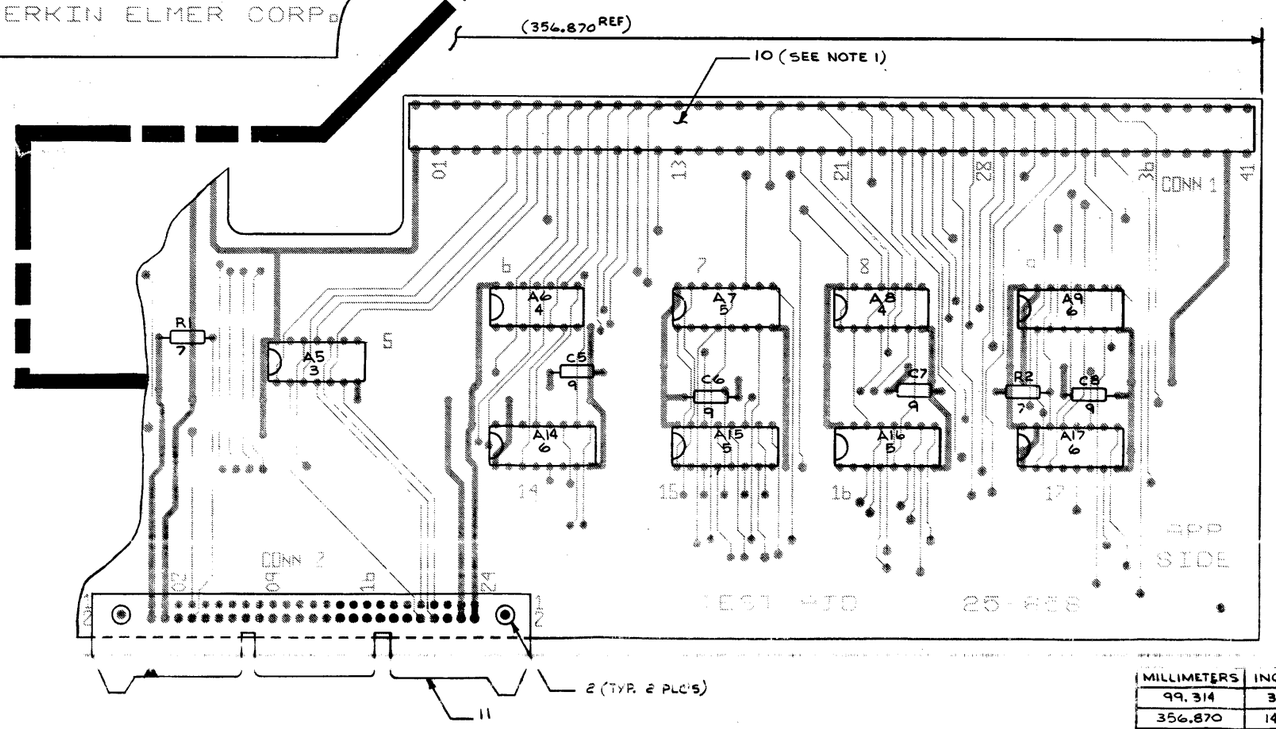
Oceanport, N.J. 07757

ASSEMBLY
LOCAL DISK CONTROLLER (8 MB)

TASK 03183 — DWG 35-806 F03 E03 — SHT 1 — 1





NOTES 1. CONNECTOR PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.

MILLIMETERS	INCHES
99.314	3.91
356.870	14.05

REVISIONS

RELEASED FOR PRODUCTION
MFG. ENG. P Odso DATE 6/20/80

METRIC

USED ON MANUAL 29-695

UNLESS OTHERWISE SPECIFIED	
SCALE:	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
J.BIELSKIE	DESTINE	DES/DFT	12-19-79
R. CERO		SUPV	5-13-80
R. CERO		CHK	5-13-80
E. MARCH		ENG	5-13-80
D. FRANKENBERGER		MGR	5-13-80
R. BARKER		QC	5-8-80

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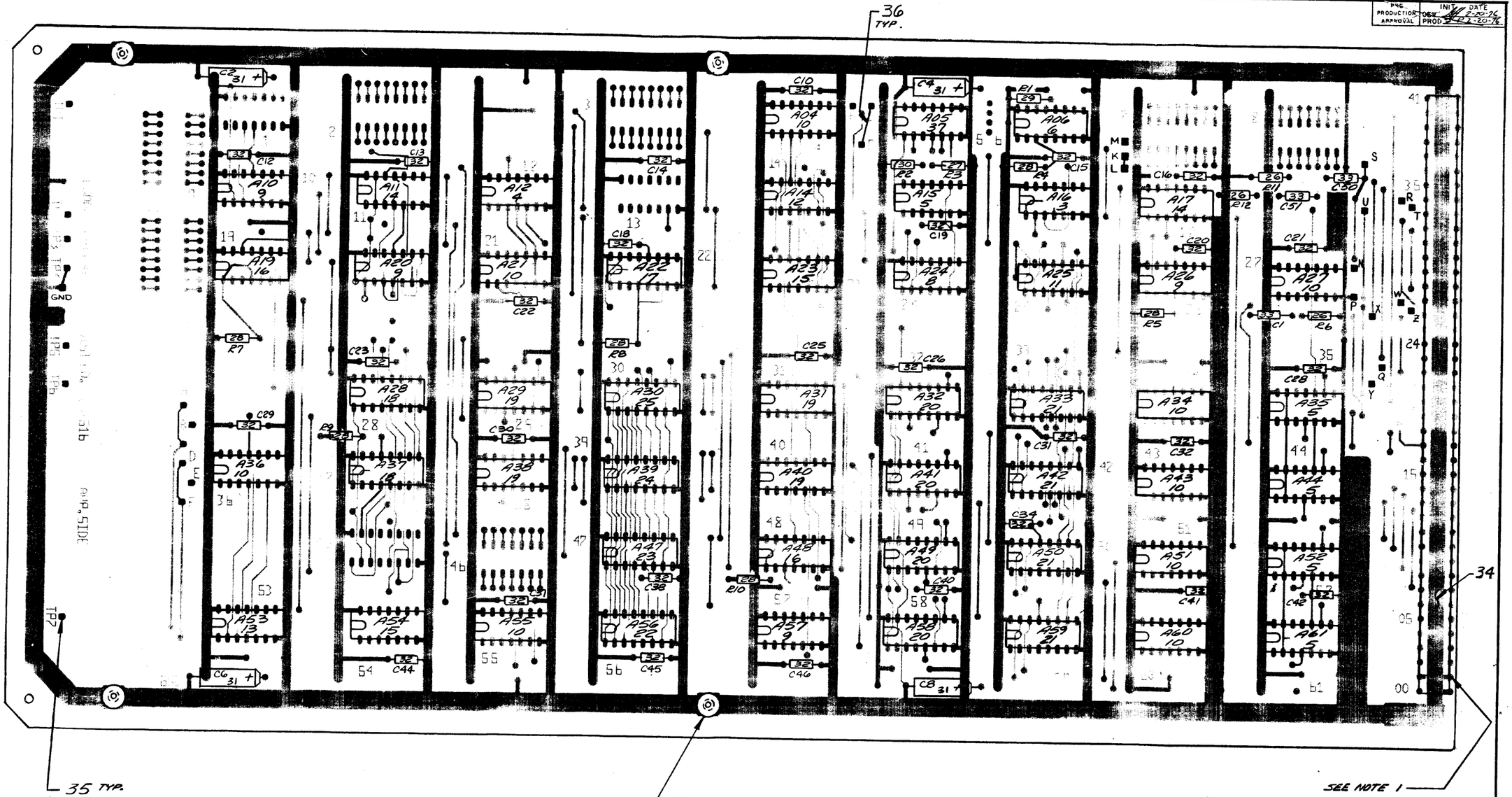
Oceanport, N.J. 07757

TITLE ASSEMBLY
TEST AID

TASK 03976	SHT
DWG 35-734 M01 D03	1 - 1

PWC PRODUCTION APPROVAL	INIT.	DATE
	PROD.	4-20-76



VARIATION TABLE														
	RESISTORS		CAP.		STRAPS									
	R12	R11	C50	C51	G-J	G-H	N-P	P-Q	R-S	S-U	T-U	U-W	X-Y	X-Z
35-622 F00	YES	YES	YES	YES	YES	NO	YES	NO	YES	NO	YES	NO	YES	NO
													NO	YES

NOTES:
1. PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO WAVE SOLDERING.

REVISIONS			
REVISED PER R05 COPPER	JCW	4683	MS 5-27-81 R06
EXTENSIVE CHANGE MADE FOR R04. SEE PREVIOUS MICRO FILM COPY. ADDED VARIATIONS & TABLE	KR	3938	M 9-13-79 R05
A48 WAS SPEC'D AS ITEM 2.		6923	I 12-2-76 R03
REVISED PER R03 COPPER		3903-1	FM 4-20-76 R02
ADDED STAKES K, L, & M. REVISED PER R02 COPPER			
RELEASED FOR PRODUCTION	MFG ENG.		DATE 4-2-

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CAPACITORS	C1,C2,C4,C6,C8,C10,C12-16,C18-C28,C30-C46,C48-C52
CAPACITORS	C1,C2,C4,C6,C8,C10,C12-16,C18-C28,C30-C46,C48-C52
RESISTORS	R1-R12
I.C.'S	A04-A06, A10-A12, A14-A17, A19-A44, A47-A61

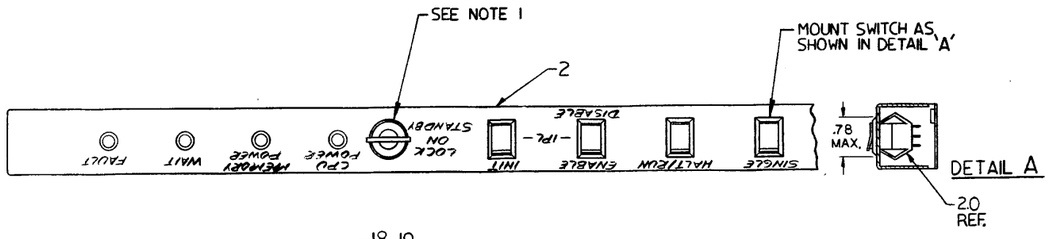
NAME	TITLE	DATE
V. PERRI	DRAFT	2-5-76
P. CEBO	CHECK	2-5-76
S. JOYCE	ENGR	4-28-76
R.A. BAELER	Q.C.	4-28-76
S. MESSINA	MGR.	4-28-76

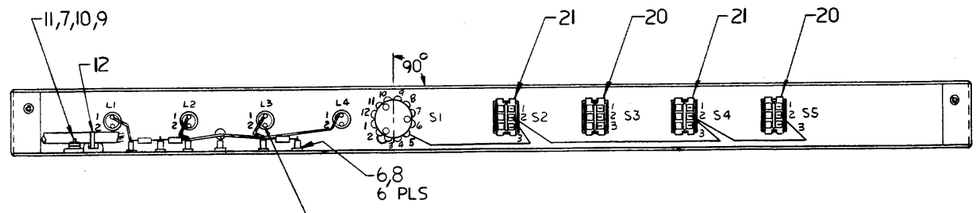
ASSEMBLY COMMUNICATION HDW. ASSIST BOARD

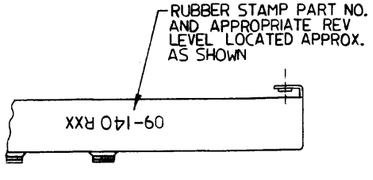
03073

SHT OF 1 — 1

35-622206 D03







WIRING INFORMATION

WIRE NO.	FROM	TO	MNEMONIC	LENGTH
1	100-1	S3-1	LSU 1	
2	200-1	S3-2	GND	
3	101-1	S4-3	SCATNØ	
4	201-1	S1-6	GND	
5	102-1	S4-1	RCATNØ	
6	202-1	NC		
7	103-1	S2-3	PFDTØ	
8	203-1	NC		
9	104-1	S5-3	SGNLØ	
10	204-1	NC		
11	105-1	R1,2,4-B	P5	
12	205-1	L4-2	GND	
13	106-1	L1-2	FAULTØ	
14	206-1	NC		
15	107-1	L2-2	WAITØ	
16	207-1	NC		
17	108-1	S1-1	POFFØ	
18	208-1	S1-1W	GND	
19	109-1	S1-3	C4	
20	209-1	L3-2	GND	
21	110-1	R3-B	P5U	
22	210-1	NC		
23	111-1	NC		
24	211-1	NC		
25	112-1	NC		
26	212-1	NC		
27	L1-1	R1-A		4.0
28	L2-1	R2-A		4.0
29	L3-1	R3-A		4.0
30	L4-1	R4-A		4.0
31	S4-2	S5-2		4.0
32	S4-2	S2-2		4.0
33	S1-5W	S2-2		4.0
34	S1-2	S1-3		.5

PART OF 17-568 ITEM 1

#24 GA. WHT STRIP. 25 EACH END ITEM 4

NOTES
1. TURN SWITCH (S1) TO CENTER POSITION ℄ ORIENT AS SHOWN.

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV [illegible]	4-15-81
	PROD MJR	4/15/81

REVISED AREAL [illegible]

BWL	JP.	4814	R	8-25-81	R01

RELEASED FOR PRODUCTION
MFG. ENG. [illegible] DATE 9-16-81

EXTENSIVE CHANGES TO WIRING TABLE, FOR PREVIOUS REV LEVEL SEE R01 MICROFILM.

KR	[illegible]	4881	B	3-26-82	R02

USED IN MANUAL 47-022

UNLESS OTHERWISE SPECIFIED

SCALE: | TOLERANCE:
DIMENSIONS ARE IN INCHES | .XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
	J. TAMUL	DES/DFT	1-6-81
R. CERO		SUPV	9.15.81
		CHK	
D. FOGGIA		ENG	9.15.81
P. ABITANTE		MGR	9.15.81
R. BARKER		QC	9.15.81

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Computer Systems Division
Oceanport, N.J. 07757

TITLE
ASSEMBLY - CONTROL PANEL CABINET

TASK 03175	SHT
DWG 09-140 R02 D03	1-1

REVISIONS		
PRE PRODUCTION APPROVAL	INIT	DATE
	DEV SS	8-28-81
	PROD MDA	8/28/81

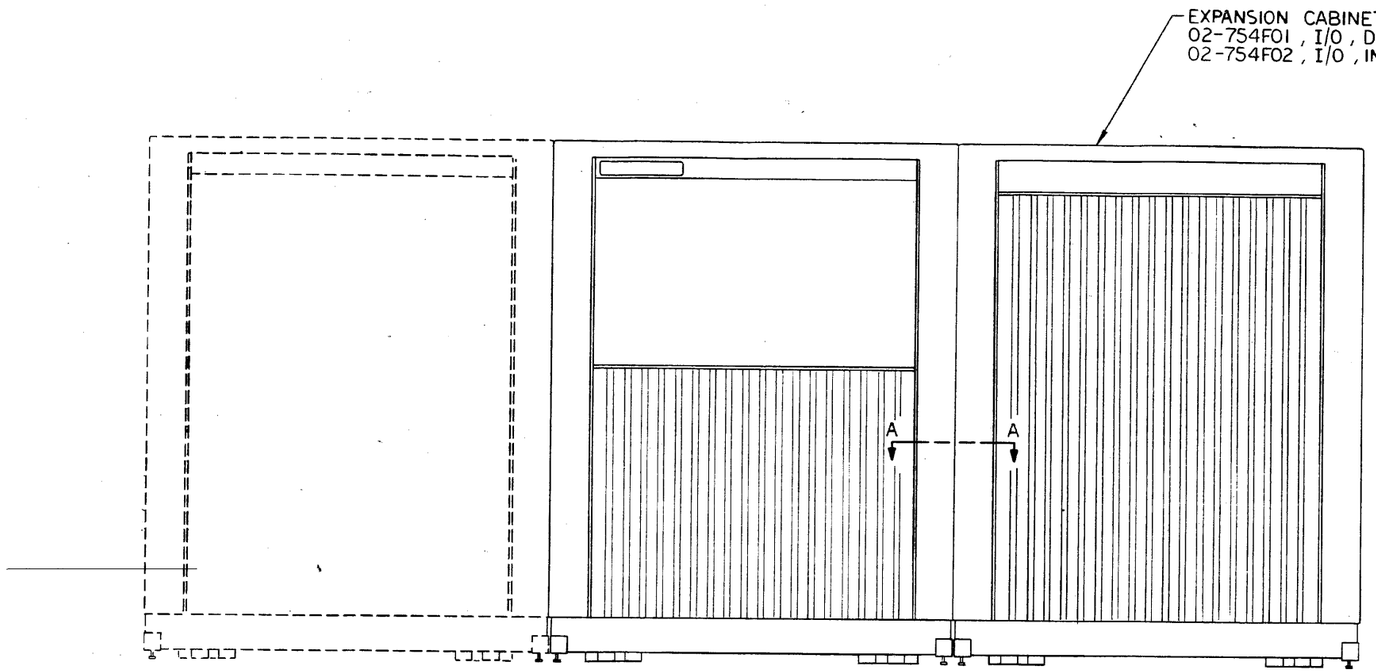
EXTENSIVE CHANGES FOR PREVIOUS REV. SEE R00 MICROFILM COPY. REVISED SHT. 2

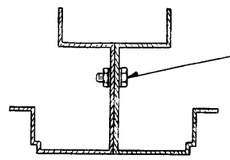
JT	VJP.	4868	R	10-15-81	R01

REVISED SHT'S, 2&3

JT	CMF	4913	R	12-3-81	R02 X

RELEASED FOR PRODUCTION
MFG. ENG. MDA DATE 12/9/81





WHEN BOLTING CABINETS TOGETHER;
REMOVE APPROPRIATE HOLE PLUGS AND SIDE SKINS.
BOLT TOGETHER WITH:
1 EA, 5/16-18 X 3/4" HEX HEAD BOLT, 16-410F01
2 EA, 5/16 EXTERNAL TOOTH LOCKWASHER, 16-380F05
1 EA, 5/16-18 HEX NUT, 16-058F05

SECTION A-A

USED IN MANUAL: 47-022

UNLESS OTHERWISE SPECIFIED	
SCALE: 1/4	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
	J TAMUL	DES/DFT	6-8-81
R CERO		SUPV	12-8-81
		CHK	
R DENGEL		ENG	12-8-81
P ABITANTE		MGR	12-8-81
R BARKER		QC	12-7-81

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Computer Systems Division
Oceanport, N.J. 07757

NOTES

3	2	SHEET NO.
01	02	REV. LEVEL
D	D	SHEET SIZE

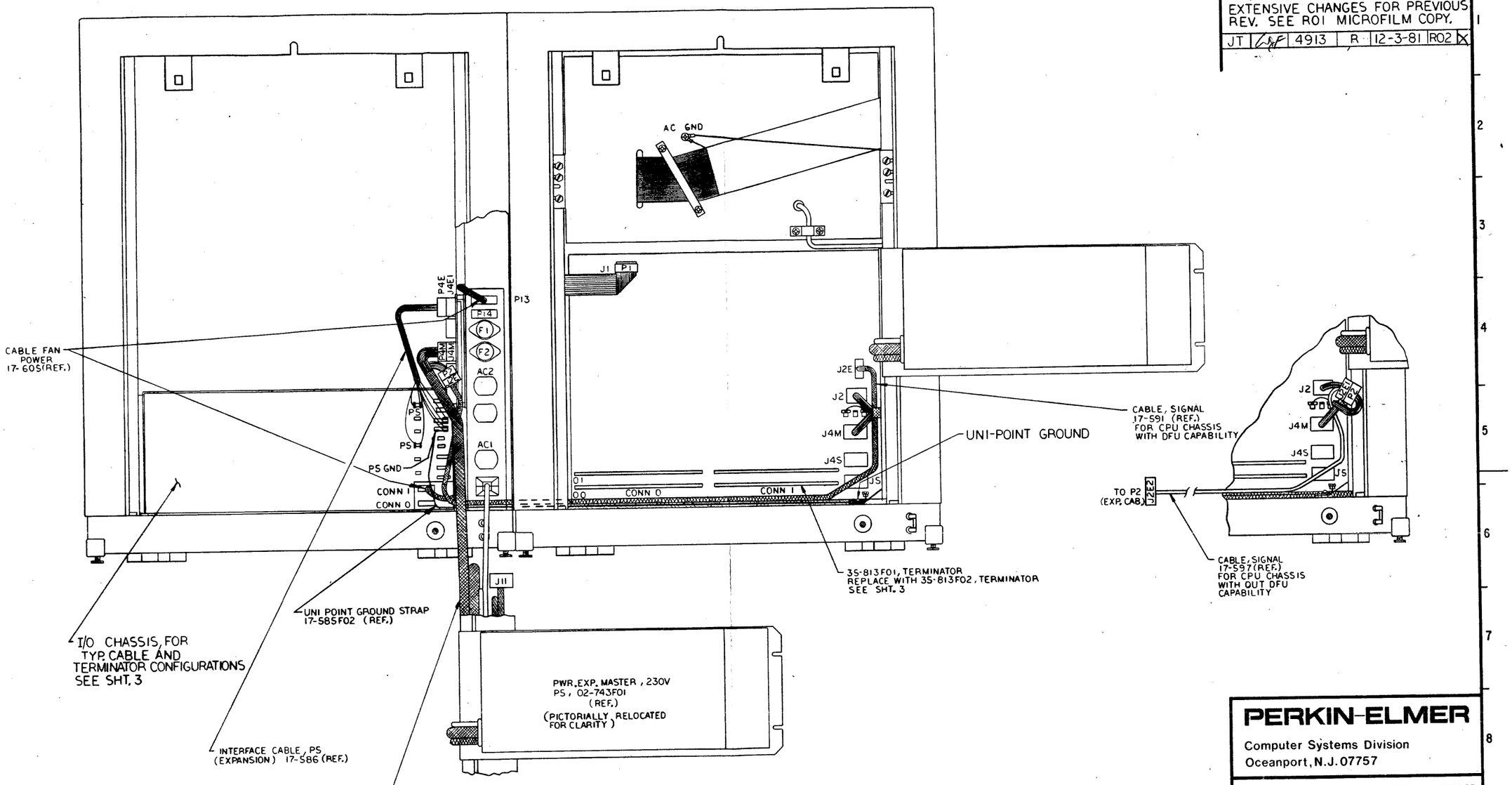
THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

TITLE
INFORMATION DWG.
I/O EXPANSION CABINET
MOD 3210 , 208V

TASK 03175	SHT
DWG 02-754R02 D12	1-3

BRUNING 44-131 4/5/79

REVISIONS				
EXTENSIVE CHANGES FOR PREVIOUS REV. SEE R01 MICROFILM COPY.				
JT	[illegible]	4913	R	12-3-81 R02 X



REAR VIEW

NOTES

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Oceanport, N.J. 07757

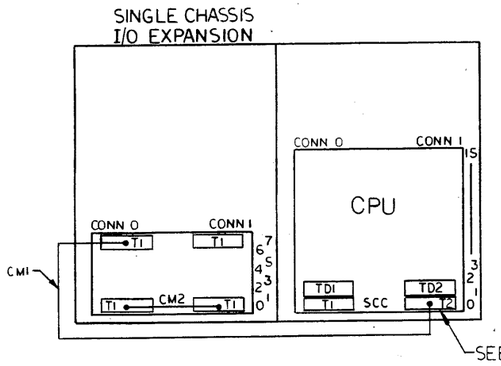
DRAFTER	J TAMULEVICIUS
DATE	5-13-81

TITLE: INFORMATION DWG. I/O EXPANSION CABINET MOD 3210, 208V

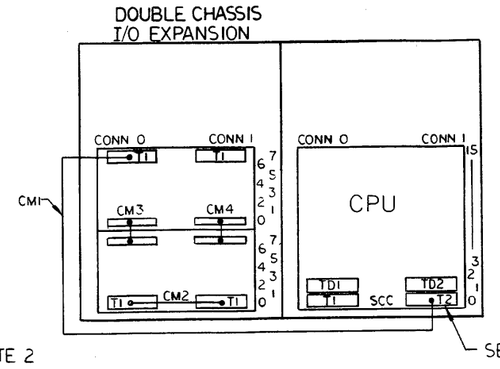
TASK 03175		SHT 2-3
DWG 02-754R02	D12	

REVISIONS					
AREAS D3, H3, M3, D8, H8 & M8, CPU CONN 1, T2 WAS T1. ADDED T2 TO AREA R4. ADDED NOTE 2					
JT	GP	4913	R	12-3-81	R01

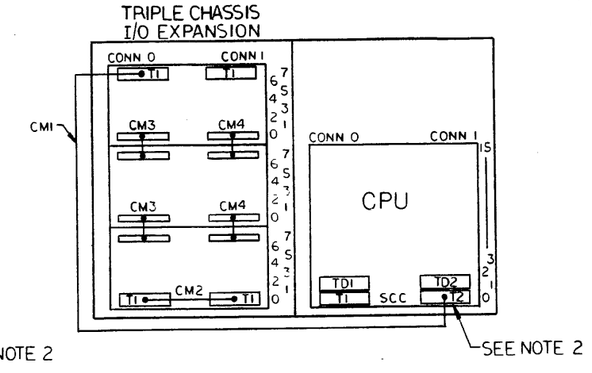
SINGLE CHASSIS
I/O EXPANSION



DOUBLE CHASSIS
I/O EXPANSION



TRIPLE CHASSIS
I/O EXPANSION



TYPICAL I/O EXPANSION CABLE INTERFACE

TERMINATORS

TERMINATOR	PART NO. REF.
T1	35-813F01
T2	35-813F02
TD1	35-814F01
TD2	35-814F02

T = MUX BUS TERMINATOR
TD = DMA TERMINATOR

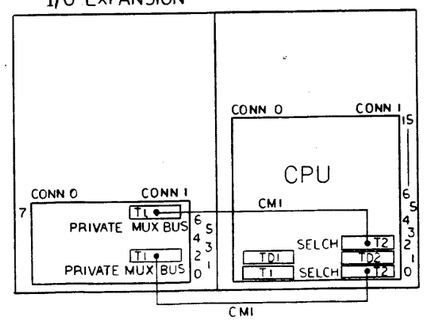
CABLES

CABLE	PART NO. REF.
CM1	17-464F04
CM2	17-464F02
CM3	17-193M02
CM4	17-194M02

CM = CABLE (MUX)

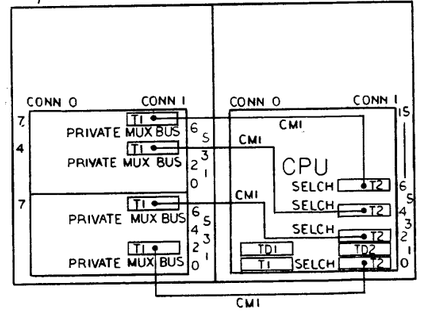
SCC = SUB CHANNEL CONTROLLER
SELCH = SELECTOR CHANNEL

SINGLE CHASSIS
I/O EXPANSION



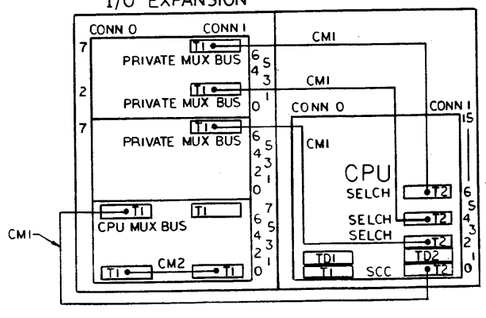
TYPICAL
I/O EXPANSION WITH SELCH
PRIVATE MUX BUSSES

DOUBLE CHASSIS
I/O EXPANSION



TYPICAL
I/O EXPANSION WITH SELCH
PRIVATE MUX BUSSES

TRIPLE CHASSIS
I/O EXPANSION



TYPICAL
I/O EXPANSION WITH CPU MUX BUS AND SELCH
PRIVATE MUX BUSSES

REAR VIEWS

NOTES
1. REF. SELCHES IN CPU CABINET ARE SHOWN FOR CONFIGURATIONS WITHOUT DFU. UP TO 3 SELCHES ARE OFFERED FOR CONFIGURATIONS WITH DFU.
2. T2 NOTED REPLACES T1 SUPPLIED WITH CPU CHASSIS. T1 IS RELOCATED IN I/O CHASSIS.

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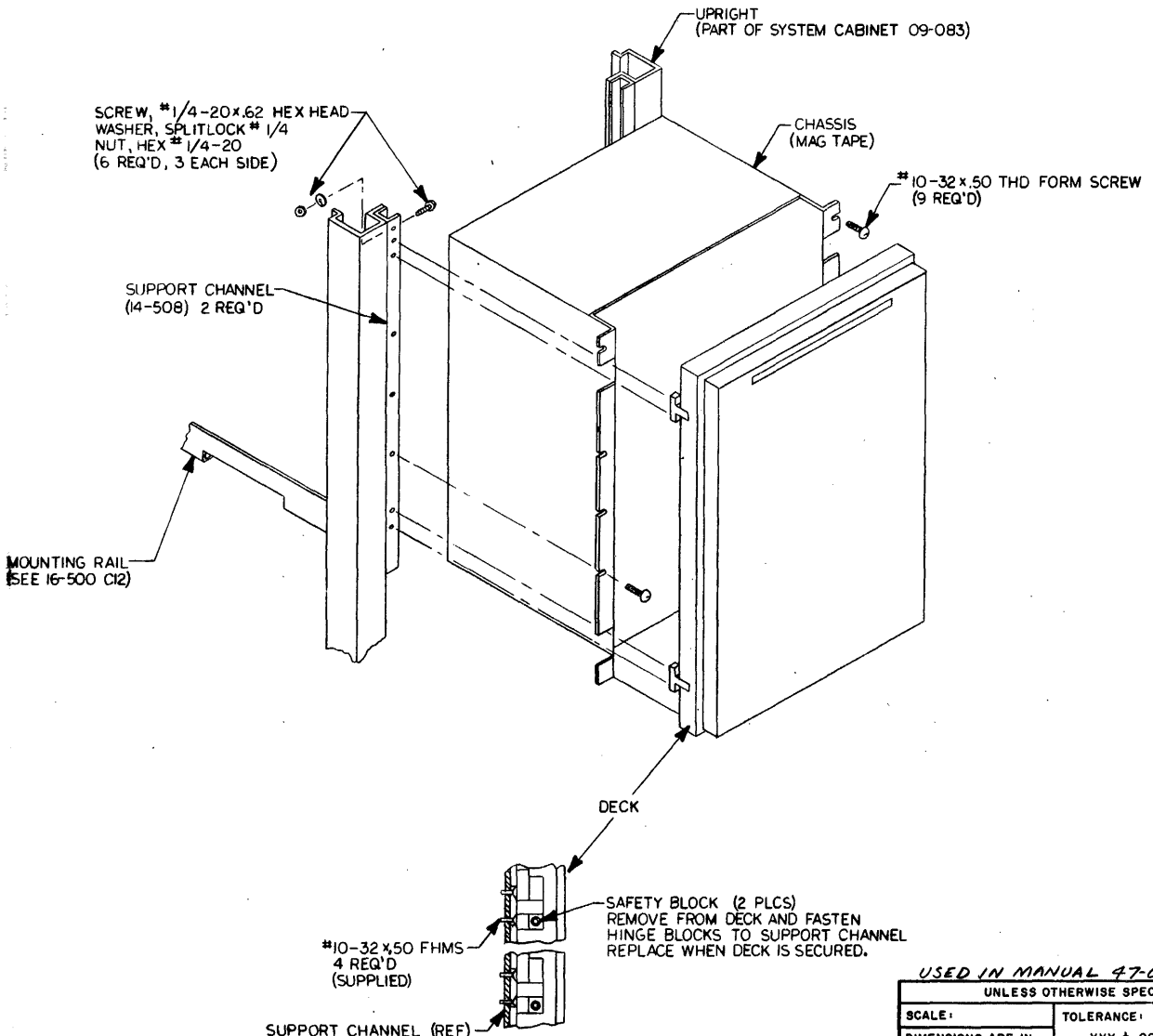
Computer Systems Division
Oceanport, N.J. 07757

DRAFTER	J TAMULEVICIUS
DATE	8-21-81

TITLE INFORMATION DWG.
I/O EXPANSION CAB.
MOD 3210 208V

TASK	03175	SHT
DWG	02-754 R01 D12	3-3

REVISIONS					
EXTENSIVE CHANGES TO SHT 1, COMPLETELY RE-DRAWN. SEE VOIDED R00 IN FILE					
KR	AJ	4888	MS	10-22-81	R01



USED IN MANUAL 47-022

SHEET NO.	2
REV LEVEL	00
SHEET SIZE	C

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT

UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE: .XXX ± .003 .X ± .03 .XX ± .02 ANGLES ± 1°	
DIMENSIONS ARE IN INCHES		
NAME	TITLE	DATE
K. REED	DES / DFT	10-19-81
G. MILLER	SUPV	
J. VIGILANTE	CHK	
D FOGGIA	ENG	
P ABITANTE	MGR	
R BARKER	QC	

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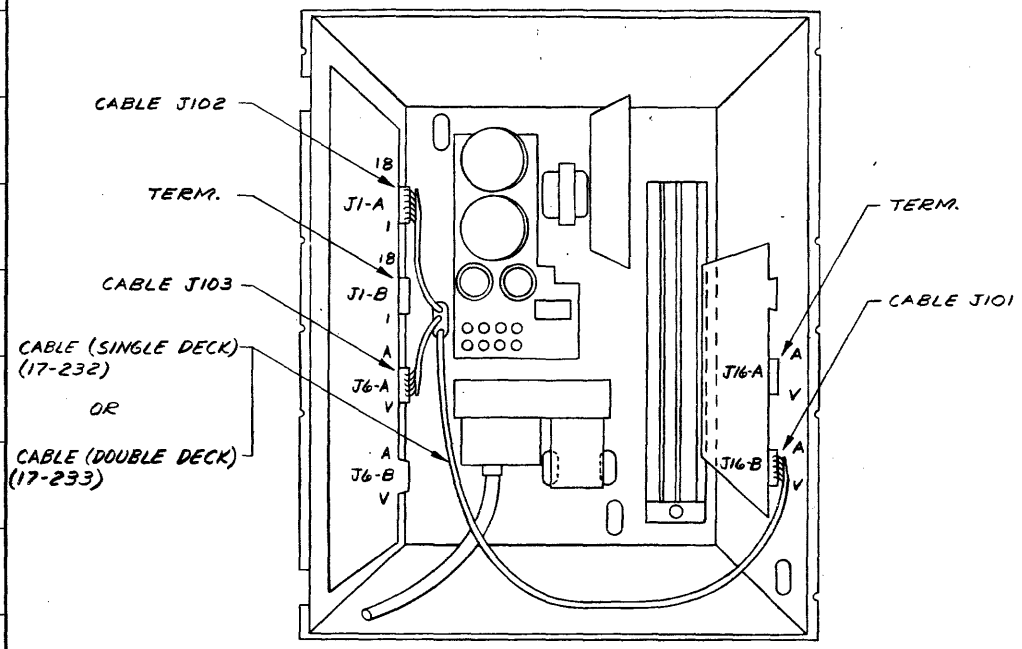
Oceanport, N.J. 07757

TITLE
INFORMATION DRAWING
WANGCO, 1175, 800 BPI
MAG TAPE SYSTEM

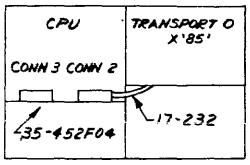
TASK	03175	SHT
DWG	02-766 R01 C12	1 - 2

PERKIN ELMER

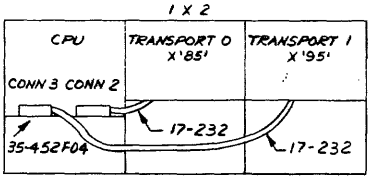
REVISIONS



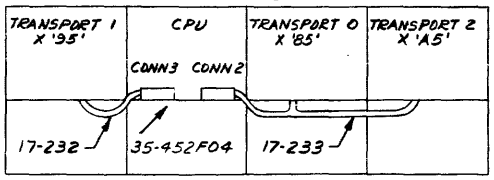
1 X 1



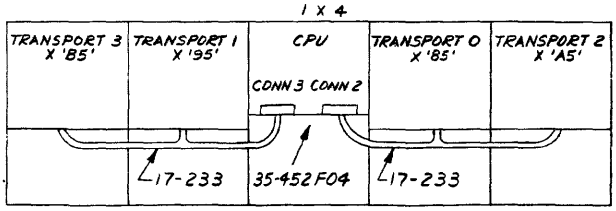
1 X 2



1 X 3



1 X 4



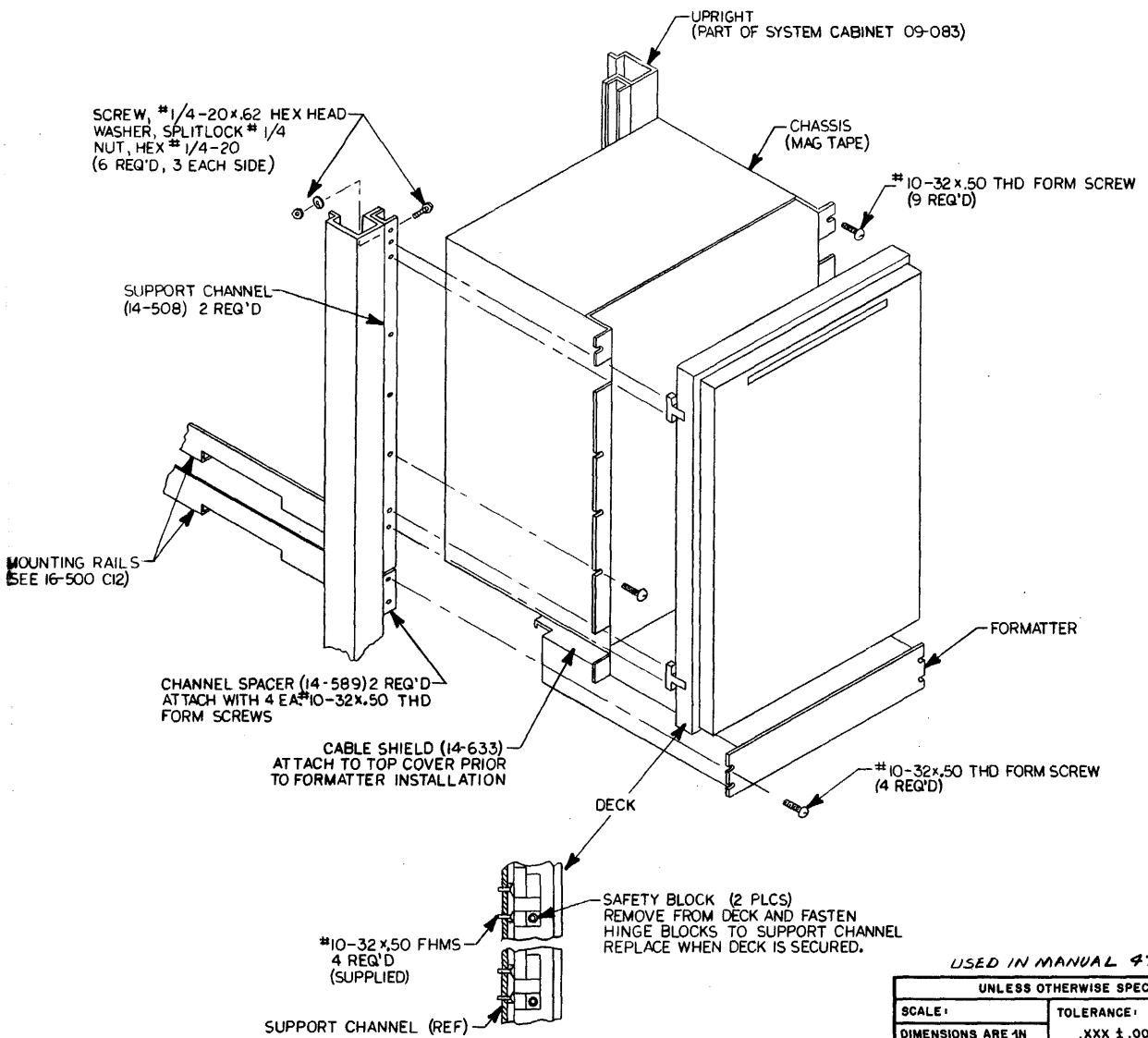
SCALE- NONE	NAME	TITLE	DATE
TOLERANCE: .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	J. TAMUL	DRAFT	
		CHK	
		ENGR	

TITLE
INFORMATION
WANGCO 1175 800 BPI
MAG TAPE SYSTEM

TASK NO. 0217 SHEET OF
DWG. NO. 02-766 C12 2 — 2

ORILVIE PRESS

REVISIONS					
EXTENSIVE CHANGES TO SHT 1, COMPLETELY RE-DRAWN. SEE VOIDED R00 IN FILE					
KP	AV	4888	MS	10-22-81	201



USED IN MANUAL 47-022

SHEET NO.	2
REV LEVEL	00
SHEET SIZE	C

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
K. REED		DES / DFT	10-19-81
G. MILLER		SUPV	
J. VIGILANTE		CHK	
D FOGGIA		ENG	
P ABITANTE		MGR	
R BARKER		QC	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE
INFORMATION DRAWING
WANGCO DUAL DENSITY
MAG TAPE SYSTEM

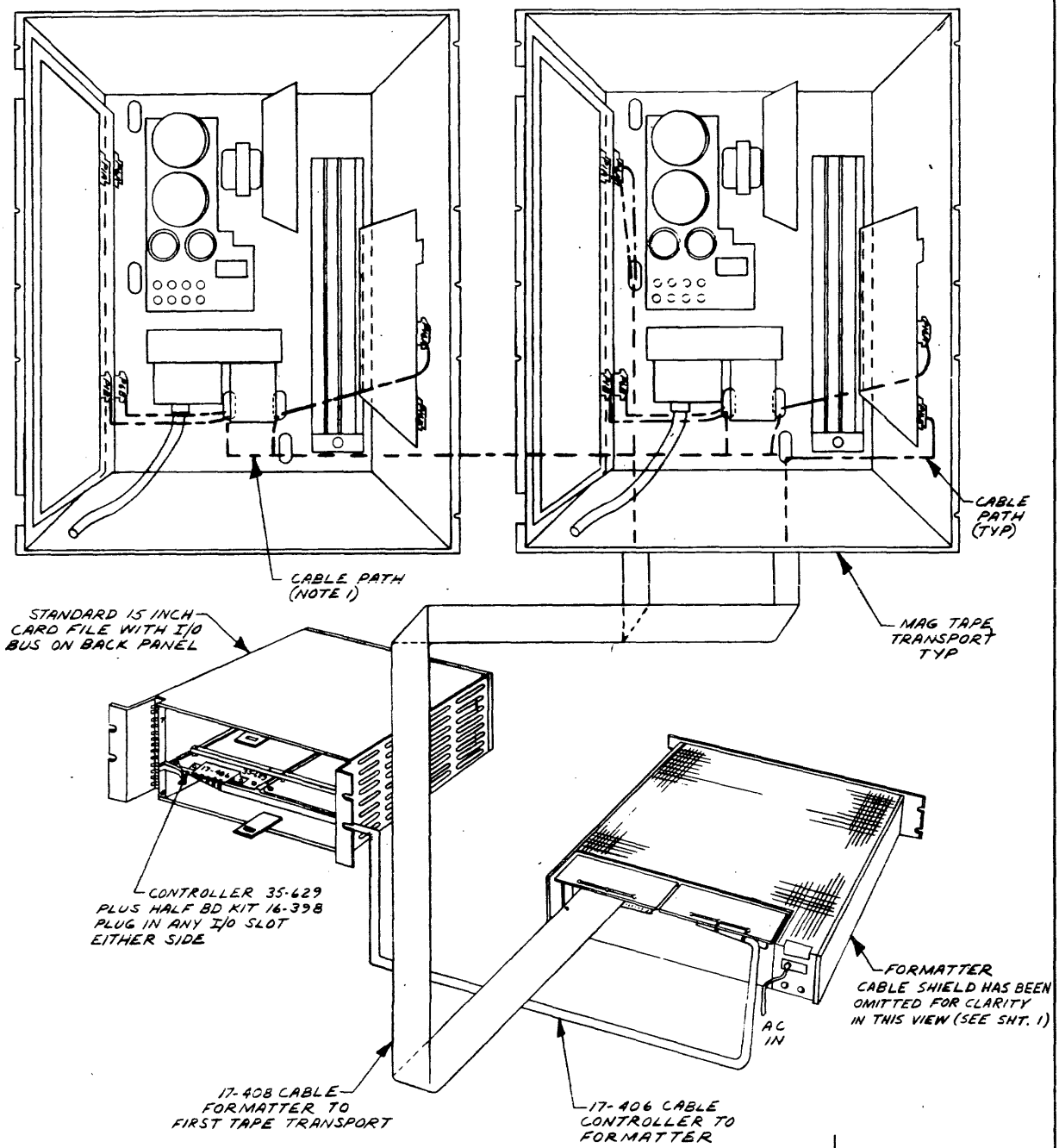
TASK	SHT
03982 (ECN 4888)	
DWG 02-764 R01 C12	1 - 2

PERKIN-ELMER

REVISIONS

NOTES

1. INTRA TRANSPORT CABLE CONNECTIONS
   P1B TO P1B
   P6B TO P6B
   P16A TO P16A



CONTROL CABLING

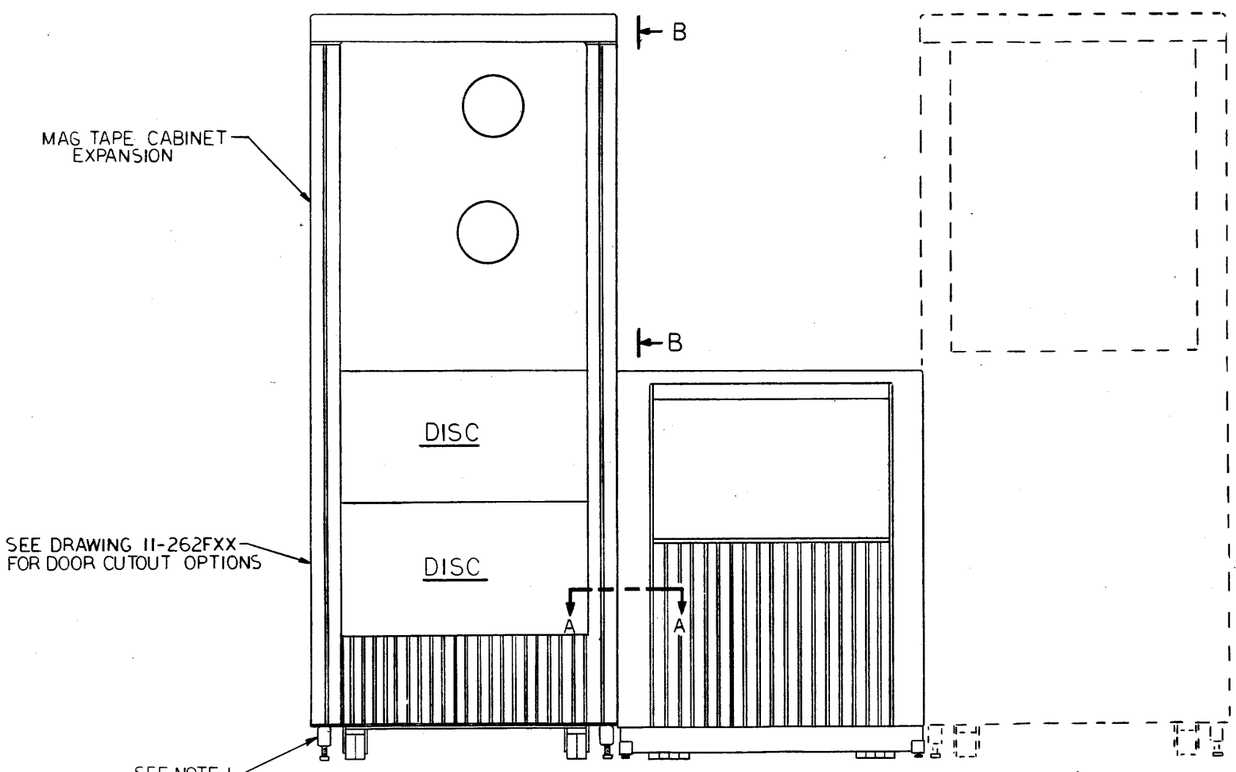
SCALE–	NAME	TITLE	DATE
TOLERANCE: .XXX ± .005, .XX ± .02, .X ± .05, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	J.TAMUL	DRAFT	
		CHK	
		ENGR	

TITLE INFORMATION WANGCO DUAL DENSITY MAG TAPE SYSTEM

DWG. NO. 03175

DWG. NO. 02-764 C/B

SHEET OF 2–2

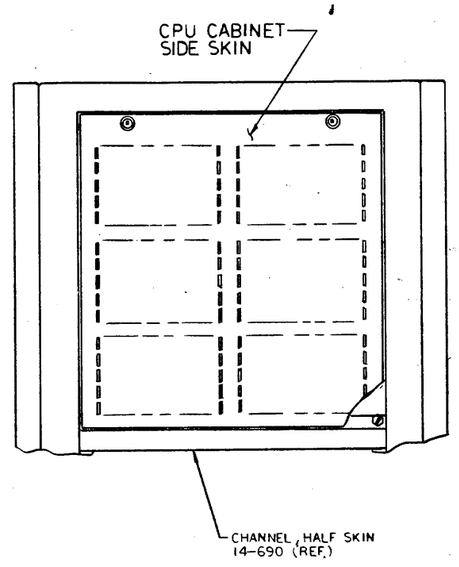


EXPANSION CABINET
(PREFERRED LOCATION FOR DISC)

CPU CABINET

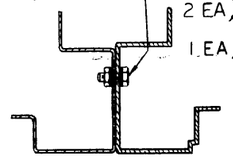
FRONT VIEW

EXPANSION CABINET
(PREFERRED LOCATION FOR I/O)



VIEW B-B

WHEN BOLTING CABINETS TOGETHER; REMOVE APPROPRIATE HOLE PLUGS AND SIDE SKINS. PLACE CPU CABINET SIDE SKIN PER VIEW B-B ON EXPANSION CABINET. BOLT TOGETHER WITH:
1 EA, 5/16-18 X 3/4 HEX HD. BOLT, 16-410F01
2 EA, 5/16 EXTERNAL TOOTH LOCKWASHER, 16-380F05
1 EA, 5/16-18 HEX NUT, 16-058F05



SECTION A-A

NOTES
1. STABILIZER LEGS ARE REQUIRED FOR ALL DISC EXPANSION 56" CABINETS. SEE INSTALLATION DRAWING 16-832

REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

BRUNING 44-131 40579

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
DEV	JT	8-28-81
PROD	MJQ	8/28/81

EXTENSIVE CHANGES FOR PREVIOUS REV. SEE R00 MICROFILM COPY, REVISED SHT. 2

JT	D.P.	4868	R	10-15-81	R01

RELEASED FOR PRODUCTION
MFG. ENG. MJQ DATE 12/9/81

REVISED SHT 2.

KR		5050	R	5-17-82	R02

USED IN MANUAL 47-022

UNLESS OTHERWISE SPECIFIED

SCALE: 3/16	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
J.TAMUL		DES/DFT	8-10-81
R.CERO		SUPV	12-8-81
		CHK	
R.DENGEL		ENG	12-8-81
P. ABITANTE		MGR	12-8-81
R.BARKER		QC	12-4-81

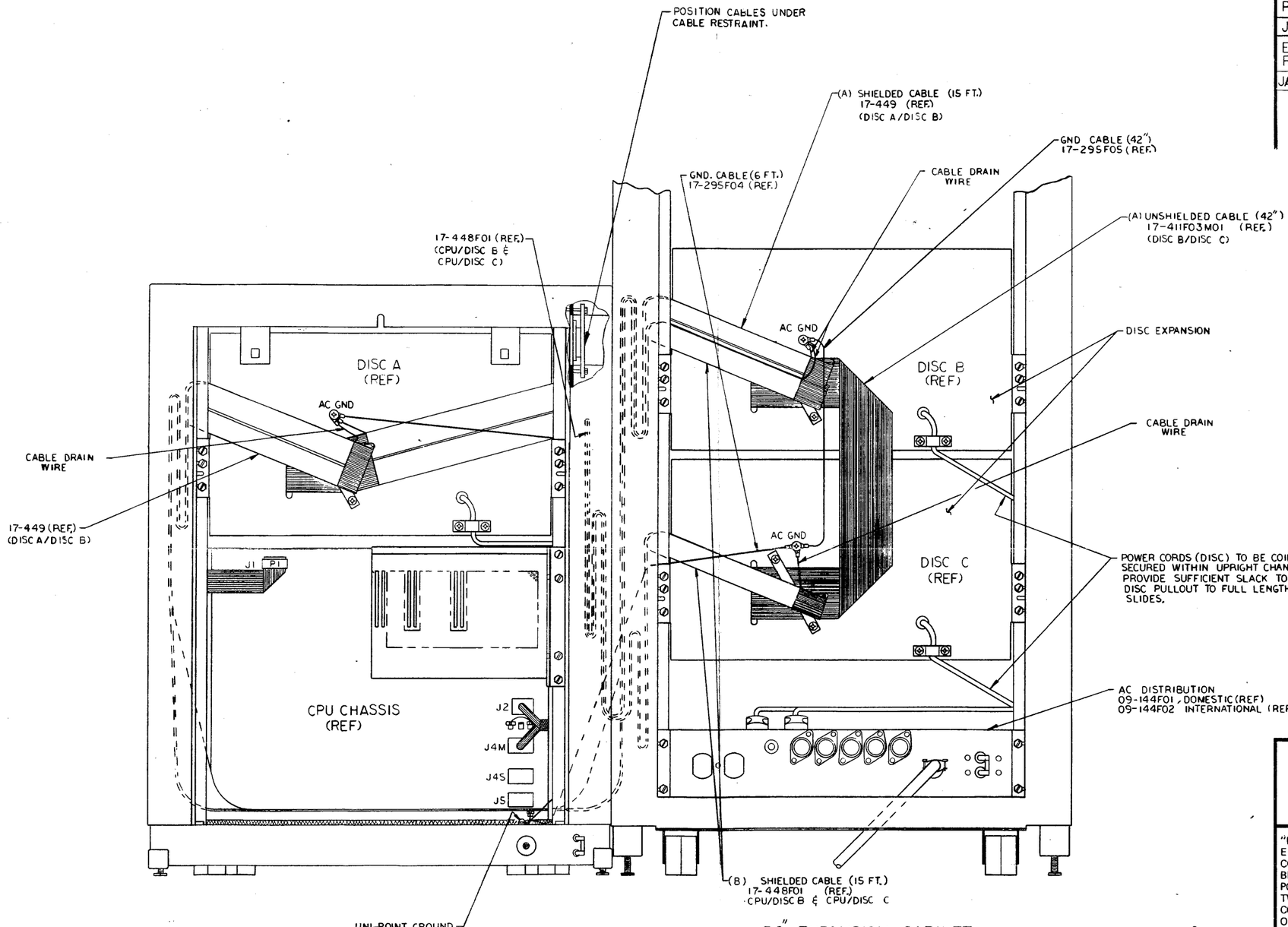
PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

2	SHEET NO.
02	REV LEVEL
D	SHEET SIZE

TITLE INFORMATION DWG.
DISC EXPANSION, 56" CABINET
MOD 3210

TASK	03175	SHT
DWG	02-761R02 D12	1-2

REVISIONS					
EXTENSIVE CHANGES FOR PREVIOUS REV SEE R00 MICROFILM COPY.					
JT	U.J.P.	4868	R	10-15-81	R01
EXTENSIVE CHANGES FOR PREVIOUS REV SEE R01 MICROFILM COPY.					
JAI		5050	F	4 12 82	R02



CPU CABINET (REF.) REAR VIEW

56" EXPANSION CABINET WITH DOUBLE DISC

NOTES

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

DRAFTER	J. TAMULEVICIUS
DATE	6-29-81

TITLE: INFORMATION DWG. 56" CABINET EXP.

TASK 03175 | SHT 2-2

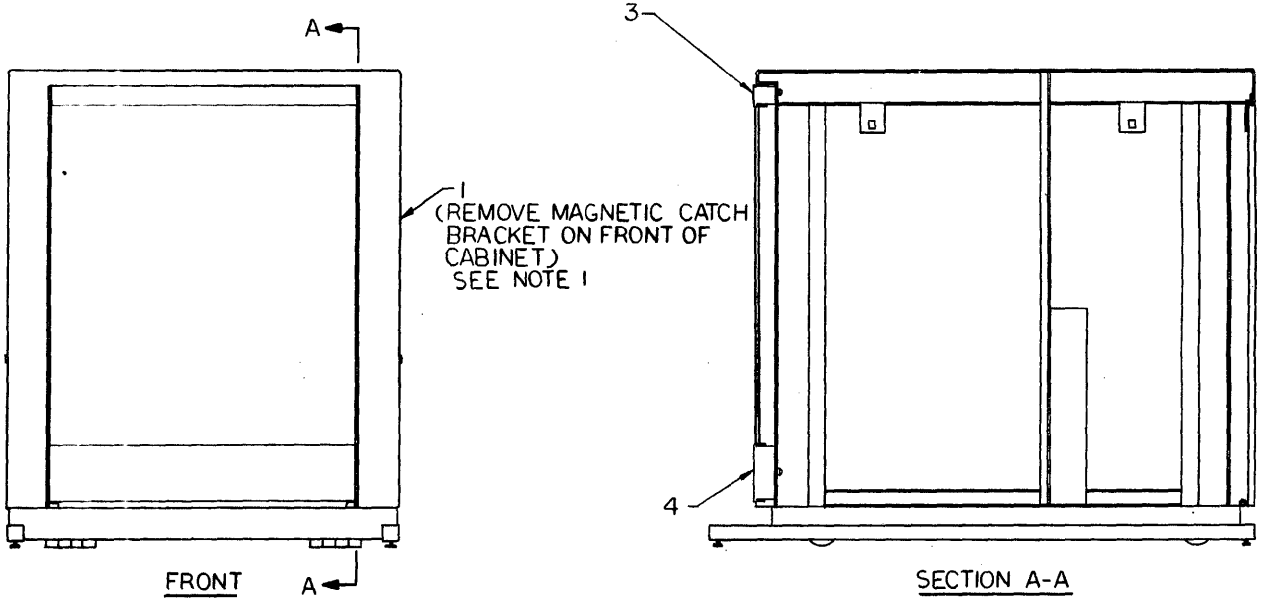
DWG 02-761R02 D12

REVISIONS			
PRE PRODUCTION APPROVAL		INIT	DATE
	DEV		8 28 81
	PROD	JM	8/27/81

AREA D4, RMVD. ITEM 7, 4 PLS.
AREA J2, RMVD. ITEM 2
CHANGED ITEM 1 PICTORIALLY

JT	DWP	9868 R	10-15-81	R01

RELEASED FOR PRODUCTION
MFG. ENG. MJG DATE 12/9/81



USED IN MANUAL 47-022

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

PART NO	DESCRIPTION
02-756 F02	INTERNATIONAL, 208V
02-756 F01	DOMESTIC, 208V

VARIATION TABLE

NOTES
1. ITEMS 8 THRU 10 TO BE INSTALLED PER 02-756 D12, SHEET 2

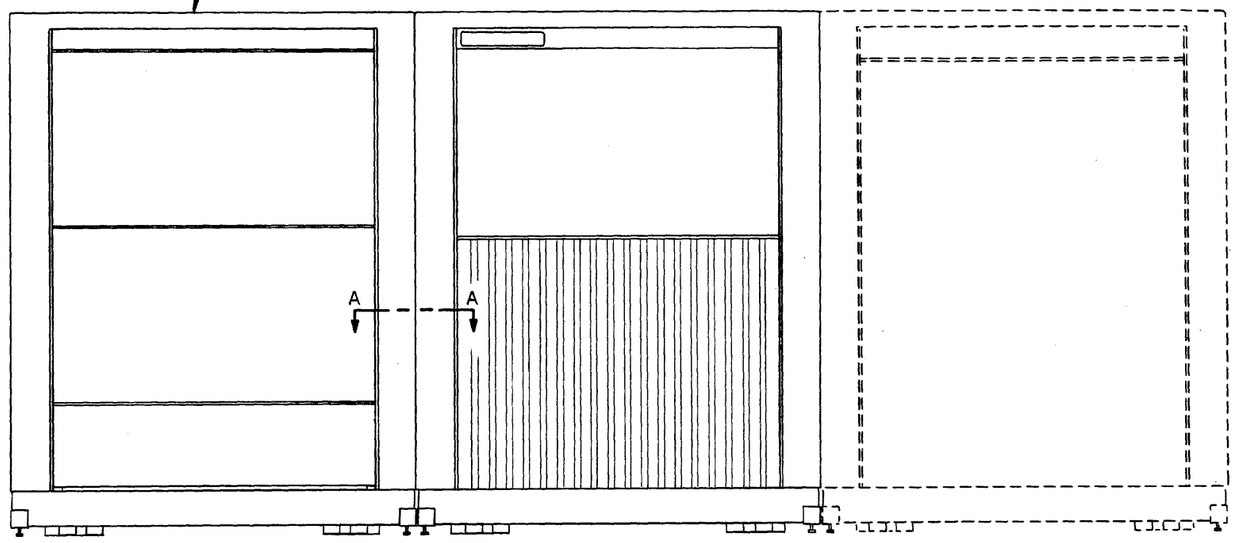
UNLESS OTHERWISE SPECIFIED			
SCALE: 3/16	TOLERANCE: .XXX ± .005 .X ± .03 .XX ± .02 ANGLES ± 1°		
DIMENSIONS ARE IN INCHES			
NAME		TITLE	DATE
	J TAMUL	DES/DFT	6-5-81
R CERO		SUPV	12-8-81
		CHK	
R DENGEL		ENG	12-8-81
P ABITANTE		MGR	12-8-81
R BARKER		QC	12-4-81

TITLE ASSEMBLY
MOD 3210 DOUBLE DISC EXPANSION CABINET

TASK 03175 SHT 1 - 1
DWG 02-756R01 C03

REVISIONS					
PRE PRODUCTION APPROVAL	INIT	DATE			
	DEV	8-28-81			
	PROD MJQ	8/28/81			
EXTENSIVE CHANGES FOR PREVIOUS REV. SEE ROO MICROFILM COPY. REVISED SHEET 2					
JT	DWP	4868	R	10-15-81	R01
RELEASED FOR PRODUCTION MFG. ENG. MJQ DATE 12/1/81					
REVISED SHT 2.					
KR	JW	3050	R	5-17-82	R02 X

EXPANSION CABINET
02-756F01, DOUBLE DISC, DOMESTIC
02-756F02, DOUBLE DISC, INTERNATIONAL

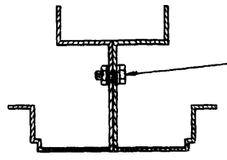


PREFERRED LOCATION FOR DOUBLE DISC EXPANSION CABINET

CPU CABINET

I/O EXPANSION CABINET

FRONT VIEW



WHEN BOLTING CABINETS TOGETHER;
REMOVE APPROPRIATE HOLE PLUGS
AND SIDE SKINS.
BOLT TOGETHER WITH:
1 EA, 5/16-18 X 3/4 HEX HEAD BOLT, 16-410F01
2 EA, 5/16 EXTERNAL TOOTH LOCKWASHER, 16-380F05
1 EA, 5/16-18 HEX NUT, 16-058F05

SECTION A-A

USED IN MANUAL 47-022

UNLESS OTHERWISE SPECIFIED	
SCALE: 1/4	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME	TITLE	DATE
J TAMUL	DES/DFT	6-8-81
R CERO	SUPV	12-8-81
	CHK	
R DENGEL	ENG	12-8-81
P ABITANTE	MGR	12-8-81
R BARKER	QC	12-4-81

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

NOTES

C SHEET NO.
C REV. LEVEL
D SHEET SIZE

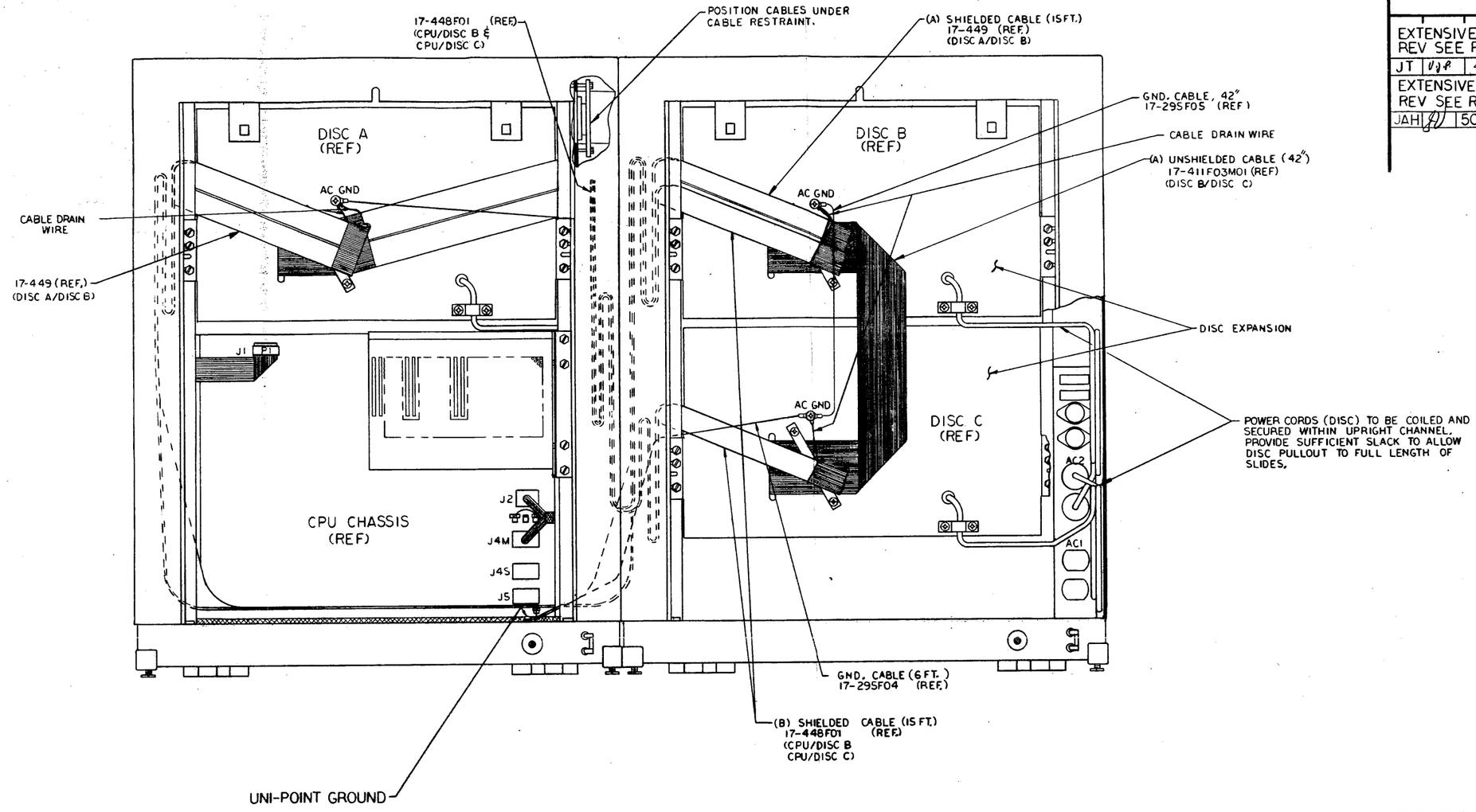
THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

TITLE INFORMATION DWG.
DOUBLE DISC EXPANSION
MOD 3210 , 208V

TASK 03175	SHT
DWG 02-756 R02 D12	1-2

BRUNING 44-137-40579

REVISIONS					
EXTENSIVE CHANGES FOR PREVIOUS REV SEE R00 MICROFILM COPY.					
JT	VJP	4868	R	10-15-81	R01
EXTENSIVE CHANGES FOR PREVIOUS REV SEE R01 MICROFILM COPY					
JAH		5050	R	4 8 82	R02



CPU CABINET (REF)

DOUBLE DISC EXPANSION CABINET

REAR VIEW

NOTES

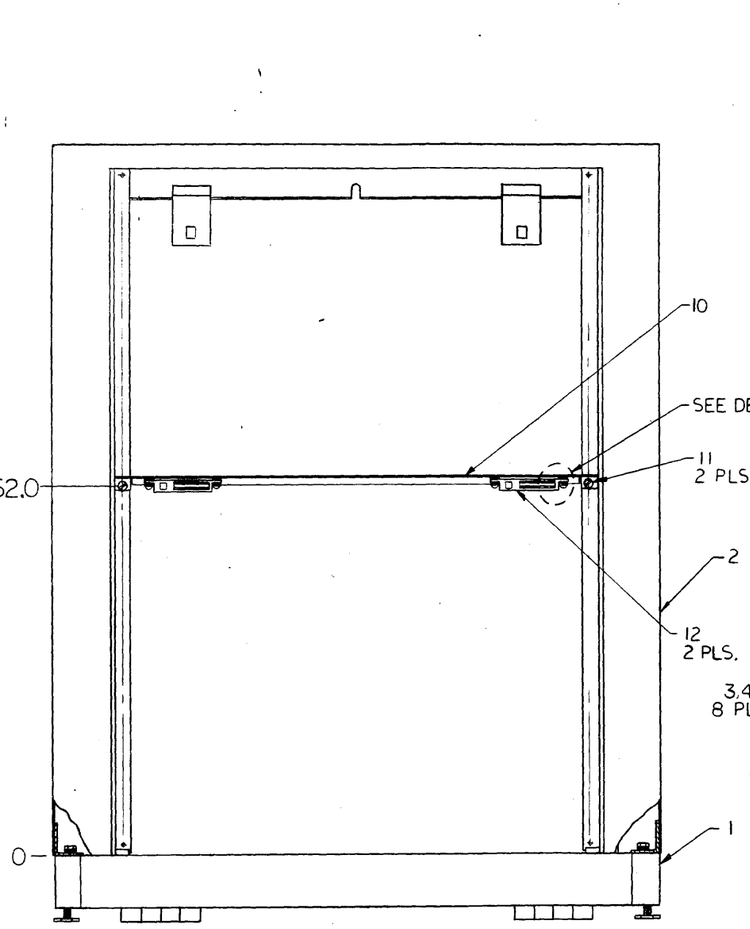
DRAFTER	
J TAMULEVICIUS	
DATE	
6-9-81	

PERKIN-ELMER

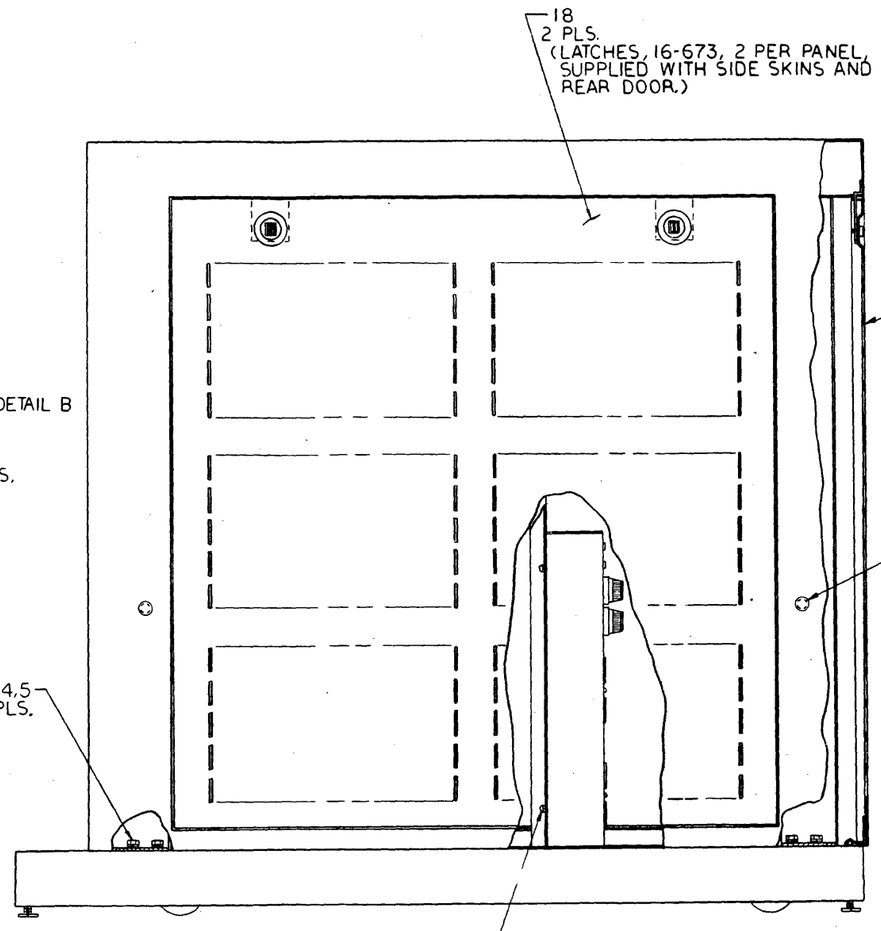
Computer Systems Division
Oceanport, N.J. 07757

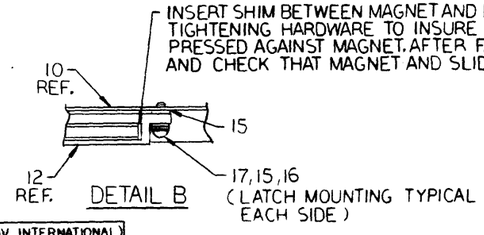
TITLE INFORMATION DWG.
DOUBLE DISC EXPANSION
MOD 3210 , 208V.

TASK	SHT
03175	2-2
DWG 02-756 R02 D12	



FRONT





DETAIL B

09-142F02	AS SHOWN (208V INTERNATIONAL)
09-142F01	AS SHOWN (208V DOMESTIC)
PART NO.	DESCRIPTION
VARIATION TABLE	

MILLIMETERS	INCHES
362.0	14.25

NOTES

BRUNING 44-131 60579

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	9-29-81
	PROD	9/25/81

RELEASED FOR PRODUCTION

MFG. ENG. _____ DATE 12-11

EXTENSIVE CHG'S MADE. SEE ROD MICRO FILM:

JMH		9476	R	11-19-82	X01	X

METRIC

USED IN MANUAL: 47-022

UNLESS OTHERWISE SPECIFIED

SCALE: 3/8

TOLERANCE:

DIMENSIONS ARE IN MILLIMETERS	INCHES	MILLIMETERS
	.XXX ±.005	.XX ±.13
	.XX ±.02	.X ±.5
	.X ±.03	X ±.8

NAME	TITLE	DATE
J. TAMUL	DES/DFT	9-2-81
R. CERO	SUPV	12-8-81
	CHK	
D. FOGGIA	ENG	12-8-81
P. ABITANTE	MGR	12-8-81
R. BARKER	QC	12-7-81

PERKIN-ELMER

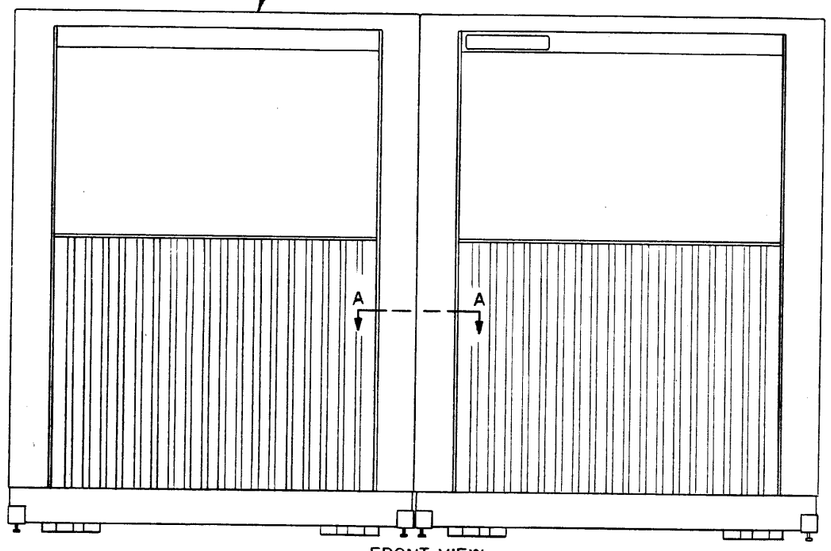
Computer Systems Division
Oceanport, N.J. 07757

TITLE ASSEMBLY BASIC CABINET (REMOVABLE SIDE SKINS)

TASK 03175 SHT 1-1

DWG 09-142 R01 D03

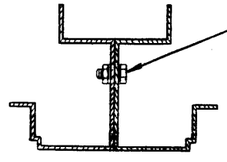
EXPANSION CABINET (REF.)
02-755F01, SINGLE DISC, DOMESTIC
02-755F02, SINGLE DISC, INTERNATIONAL
02-755F03, I/O & SINGLE DISC, DOMESTIC
02-755F04 I/O & SINGLE DISC, INTERNATIONAL



FRONT VIEW

PREFERRED LOCATION FOR
SINGLE DISC EXPANSION
OR
I/O & SINGLE DISC EXPANSION
CABINET

CPU CABINET



SECTION A-A

WHEN BOLTING CABINETS TOGETHER;
REMOVE APPROPRIATE HOLE PLUGS
AND SIDE SKINS.
BOLT TOGETHER WITH:
1 EA, 5/16-18 X 3/4" HEX HEAD BOLT, 16-410F01
2 EA, 5/16 EXTERNAL TOOTH LOCKWASHER, 16-380F05
1 EA, 5/16-18 HEX NUT, 16-058F05

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	8-28-81
	PROD	8/28/81

EXTENSIVE CHANGES FOR PREVIOUS REV. SEE R00 MICROFILM COPY. REVISED SHT. 2

JT	WJA	4868	R	10-15-81	R01

REVISED SHT. 2

JT	[illegible]	4913	R	12-3-81	R02 X

RELEASED FOR PRODUCTION
MFG. ENG. [illegible] DATE 12/9/81

REVISED SHT 2

KR	[illegible]	5050	R	5-17-82	R03 X

USED IN MANUAL 47-022

UNLESS OTHERWISE SPECIFIED		
SCALE: 1/4	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME	TITLE	DATE
J TAMUL	DES/DFT	6-8-81
R CERO	SUPV	12-8-81
	CHK	
R DENGEL	ENG	12-8-81
P ABITANTE	MGR	12-8-81
R BARKER	QC	12-4-81

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

NOTES

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

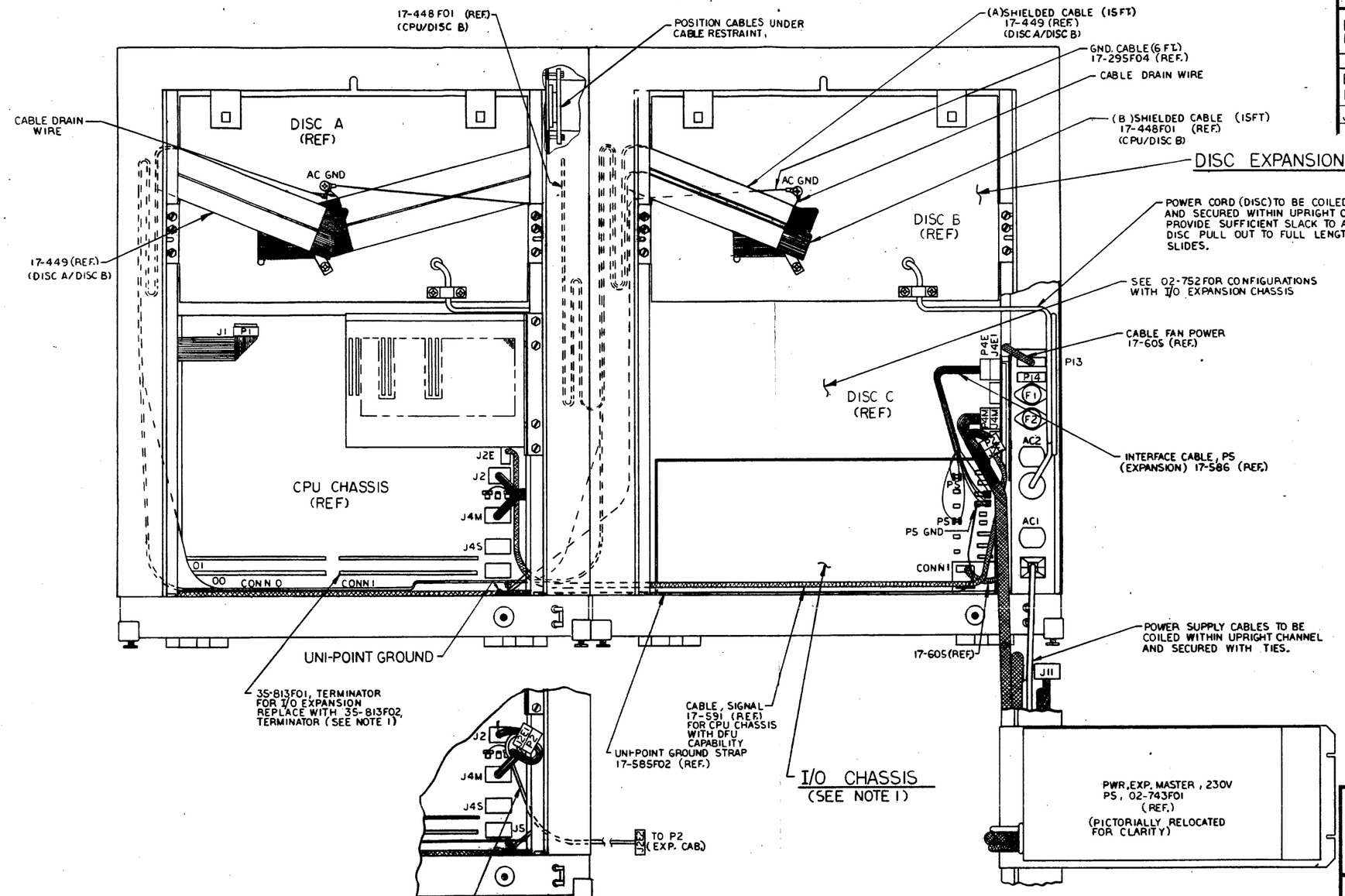
2	SHEET NO.
03	REV. LEVEL
D	SHEET SIZE

TITLE
INFORMATION DWG.
SINGLE DISC EXPANSION OR I/O & SINGLE DISC EXPANSION CABINET
MOD 3210 , 208V

TASK	SHT
03175	1-2
DWG 02-755R03 D12	

HRUNNING 44-131 40679

REVISIONS					
EXTENSIVE CHANGES FOR PREVIOUS REV. SEE R01 MICROFILM COPY.					
JT	[illegible]	4913	R	12-3-81	R02
EXTENSIVE CHANGES FOR PREVIOUS REV. SEE R02 MICROFILM COPY.					
JAH	[illegible]	5050	R	4-8-82	R03



NOTES 1. SEE 02-754 D12, SHT. 3 FOR TYPICAL I/O CABLE AND TERMINATOR CONFIGURATIONS.

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

DRAFTER	J TAMULEVICIUS
DATE	6-9-81

TITLE INFORMATION DWG. SINGLE DISC EXPANSION OR I/O & SINGLE DISC EXPANSION CABINET MOD 3210, 208V

TASK 03175 | SHT 2-2

DWG 02-755 R03 D12

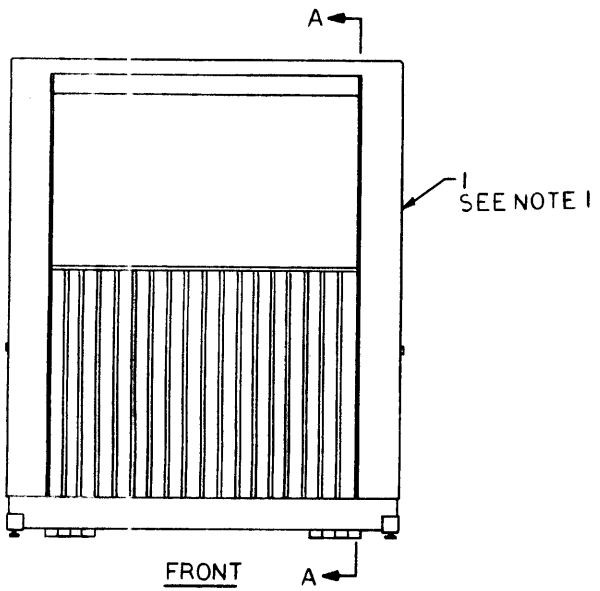
BRUNING 44-131-40579-2

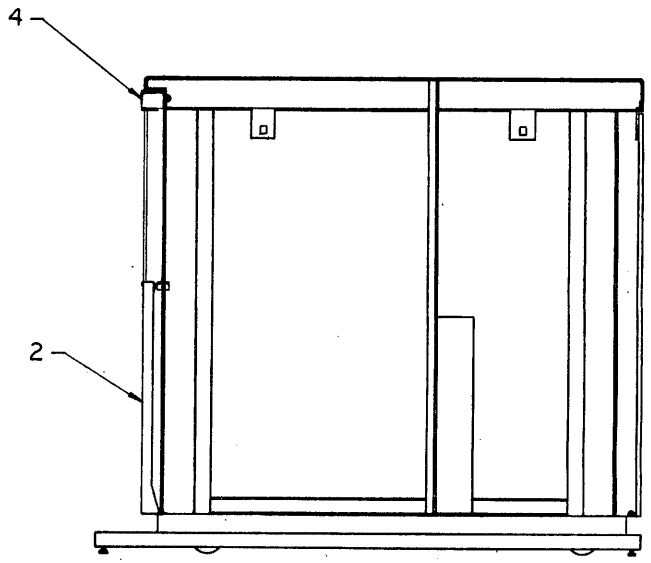
REVISIONS			
PRE PRODUCTION APPROVAL	INIT	DATE	
	DEV	8 28 81	
	PROD	8 28 81	

AREA D4, RMVD. ITEM 6, 4 PLS.
AREA J4, RMVD. ITEM 3
CHANGED ITEM 1, PICTORIALLY
REVISED SHEET 2

JT	D.P.	4868	R	10-15-81	R01
REVISED SHT. 2					
JT	DP	4913	R	12 3 81	R02

RELEASED FOR PRODUCTION
MFG. ENG. MJ DATE 12/9/81





METRIC

USED IN MANUAL 47-022

PART NO	DESCRIPTION
02-755 F01	AS SHOWN, SHT. 1 (SINGLE DISC, DOMESTIC, 208V)
02-755 F02	AS SHOWN, SHT. 1 (SINGLE DISC, INTERNATIONAL, 208V)
02-755 F03	AS SHOWN, SHT. 2 (I/O & SINGLE DISC, DOMESTIC, 208V)
02-755 F04	AS SHOWN, SHT. 2 (I/O & SINGLE DISC, INTERNATIONAL, 208V)

VARIATION TABLE

NOTES:
1. ITEMS 7-9 TO BE INSTALLED PER 02-755 D12

2	SHEET NO
02	REV LEVEL
C	SHEET SIZE

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

UNLESS OTHERWISE SPECIFIED

SCALE: 3/16	MILLIMETERS	INCHES
DIMENSIONS ARE IN MILLIMETERS	.XX ± .13 .X ± .5 .X, ± .8	.XXX ± .005 .XX ± .02 .X ± .03

NAME	TITLE	DATE
J TAMUL	DES / DFT	6-5-81
R CERO	SUPV	12-8-81
	CHK	
R DENGEL	ENG	12-8-81
P ABITANTE	MGR	12-8-81
R BARKER	QC	12-4-81

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

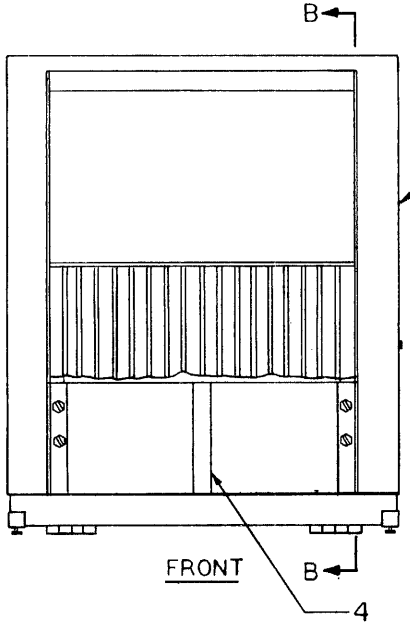
TITLE ASSEMBLY
MOD 3210 SINGLE DISC EXP. CAB. OR I/O & SINGLE DISC EXP. CAB.

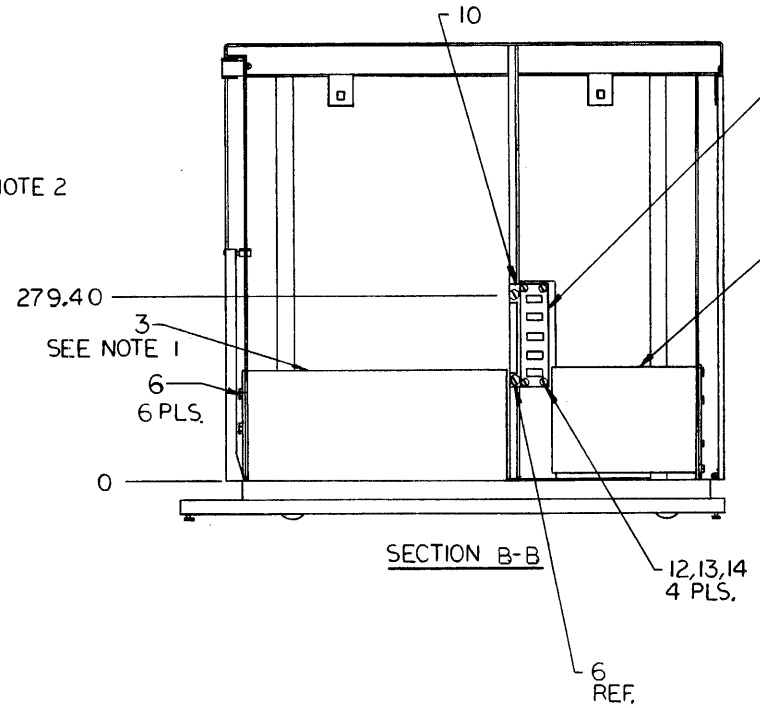
TASK 03175 SHT 1-2
DWG 02-755 R02 C03

BRUNING 44-131 40579

MILLIMETERS	INCHES
279.40	11.00

REVISIONS				
CHANGED ITEM 1 PICTORIALLY ADDED DIM. AREA G5, SECTION B-B WAS A-A				
J T	J&P	4868	R	10-15-81 R01
ADDED ITEMS 15-19 TO NOTE 2				
J T		4913	R	12-3-81 R02





NOTES

1. FOR TERMINATION OF CABLES SEE 02-755 D12
2. ITEMS 7-9,15-19 TO BE INSTALLED PER 02-755D12, SHT. 2

NAME		TITLE	DATE
	J TAMUL	DES / DFT	6-5-81
R CERO		SUPV	
		CHK	
R DENGEL		ENG	
P ABITANTE		MGR	
R BARKER		QC	

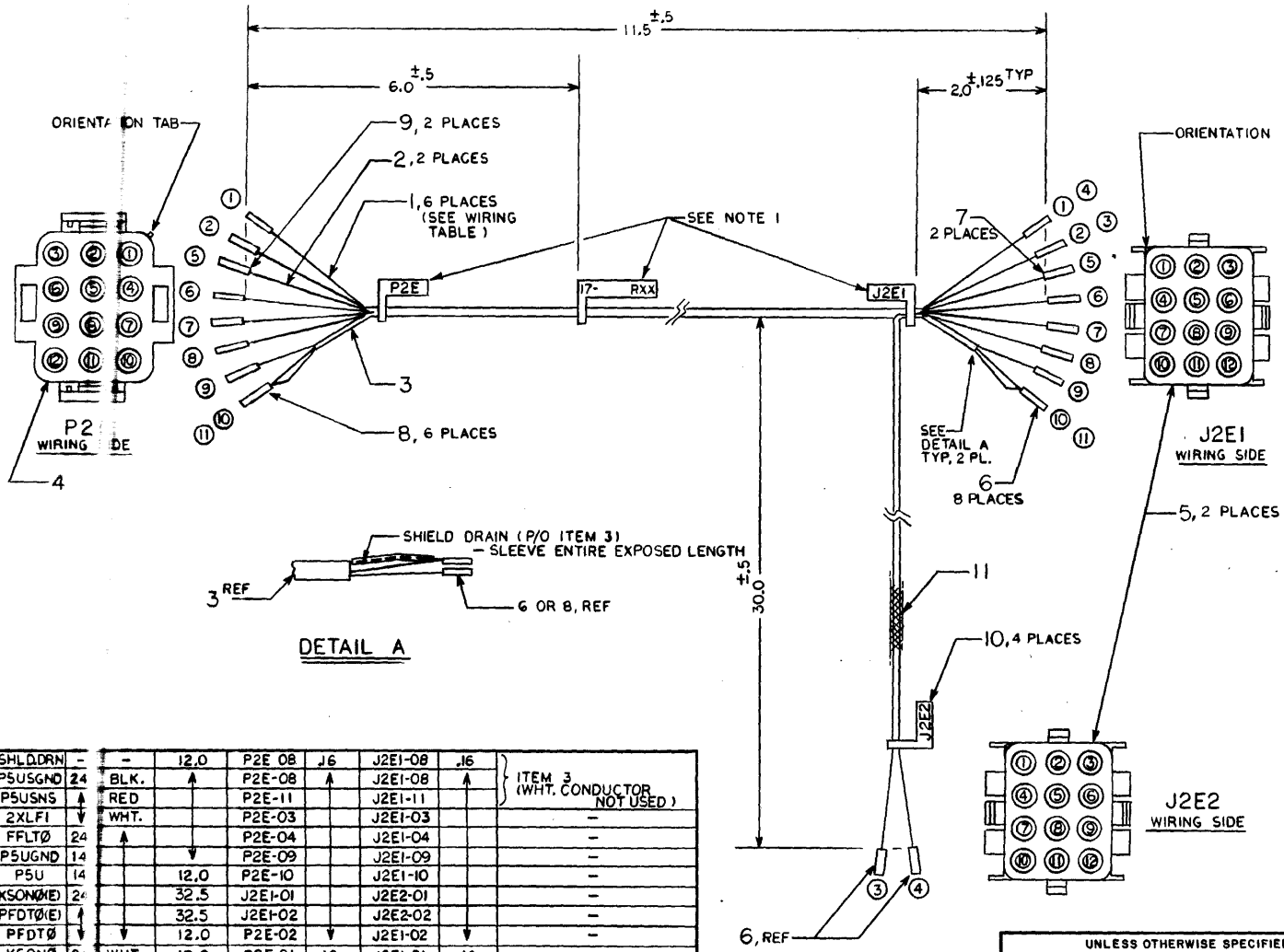
PERKIN-ELMER

Computer Systems, Division
Oceanport, N.J. 07757

TITLE ASSEMBLY
MOD 3210 SINGLE DISC EXP. CAB. OR I/O & SINGLE DISC EXP CAB.

TASK 03175 | SHT 2-2

DWG 02-755 R02 C03



DETAIL A

WIRE NO.	SIGNAL	GA	COLOR	LENGTH REF.	FROM	STRIP	TO	STRIP	REMARKS
11	SHLDDRN	-	-	12.0	P2E-08	.16	J2E1-08	.16	ITEM 3 (WHT. CONDUCTOR NOT USED)
10	P5USGND	24	BLK.	↑	P2E-08	↑	J2E1-08	↑	
9	P5USNS	↑	RED		P2E-11		J2E1-11		
8	2XLFI	↓	WHT.		P2E-03		J2E1-03		–
7	FFLTØ	24	↑		P2E-04		J2E1-04		–
6	P5UGND	14		↓	P2E-09		J2E1-09		–
5	P5U	14		12.0	P2E-10		J2E1-10		–
4	KSONØ(E)	24		32.5	J2E1-01		J2E2-01		–
3	PFDTØ(E)	↑		32.5	J2E1-02		J2E2-02		–
2	PFDTØ	↓	↓	12.0	P2E-02	↓	J2E1-02	↓	–
1	KSONØ	24	WHT.	12.0	P2E-01	.16	J2E1-01	.16	–

WIRING TABLE

NOTES 1. IDENTIFY AS SHOWN.

INCH	MM
30.5	775.
30.0	762.
12.0	305.
11.5	292.
6.0	152.
2.0	50.8
.5	12.7
.16	4.0
.125	3.2

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
DEV	[illegible]	8-28-81
PROD	MJQ	8-28-81

PER APPROVED REQUEST
AREA G3 - ADDED SLEEVING, ITEM 11. ADDED TOLERANCES TO DETAIL & MM CONV. CHART ADDED "USED IN MANUAL" NOTE.

WF	LC	–	–	12-8-81 R01

RELEASED FOR PRODUCTION
MFG. ENG. MJQ DATE 12/8/81

IN WIRING TABLE, WIRE LENGTHS OF 3 & 4 WERE 30.5 :

MH	[illegible]	5046	R	5-18-82 R02

USED IN MANUAL: 47-022

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Oceanport, N.J. 07757

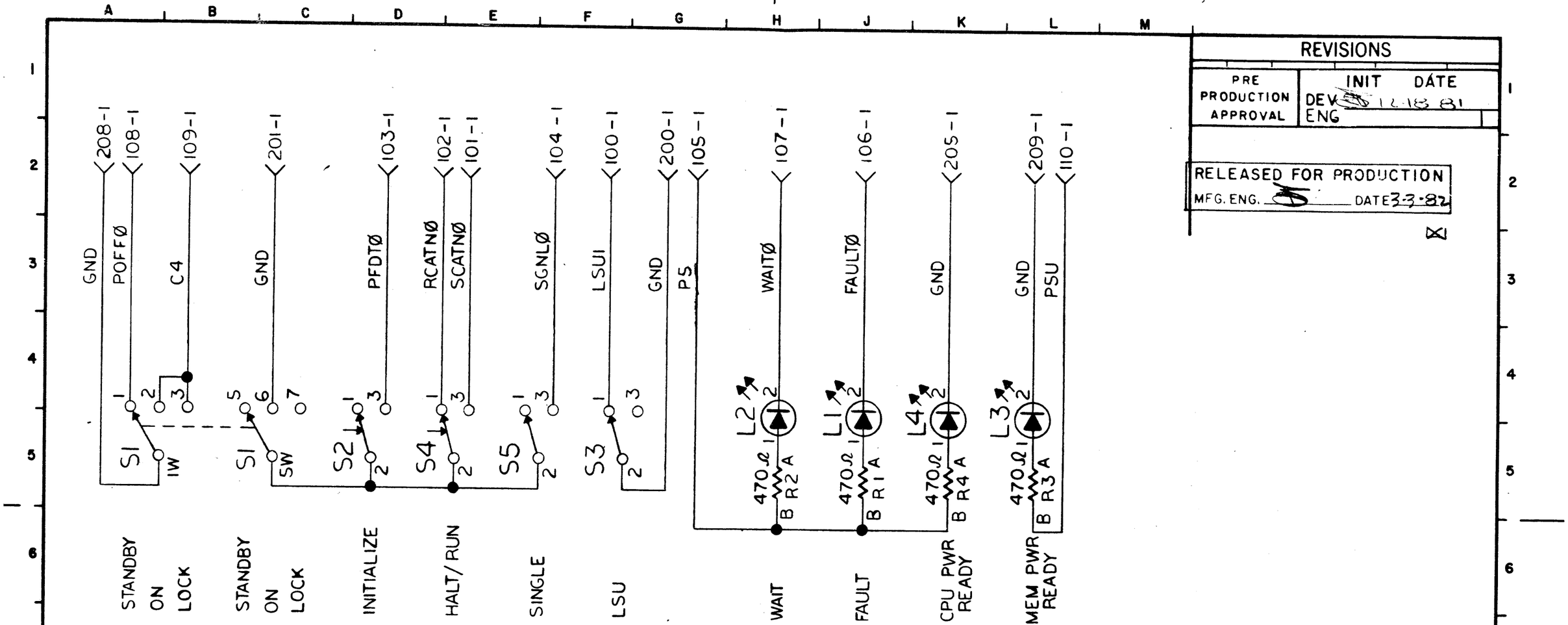
METRIC

UNLESS OTHERWISE SPECIFIED
SCALE: ~
DIMENSIONS ARE IN INCHES
TOLERANCE: INCH .XXX ±.005, .XX ±.02, .X ±.05; MM .X ±.5, X. ±.8

NAME	TITLE	DATE
W. FRASER	DES/DFT	8-7-81
R. CERO	SUPV	12-8-81
	CHK	
D. FOGGIA	ENG	12-8-81
P. ABITANTE	MGR	12-8-81
R. BARKER	QC	12-8-81

TITLE: CABLE, I/O EXP. (INTERIM)

TASK 03175 SHT 1-1
DWG 17-597 R02 C03



REVISIONS		
PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	12-18-81
	ENG	

RELEASED FOR PRODUCTION
MFG. ENG. _____ DATE 3-3-82

USED IN MANUAL : 47-022

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Computer Systems Division
Oceanport, N.J. 07757

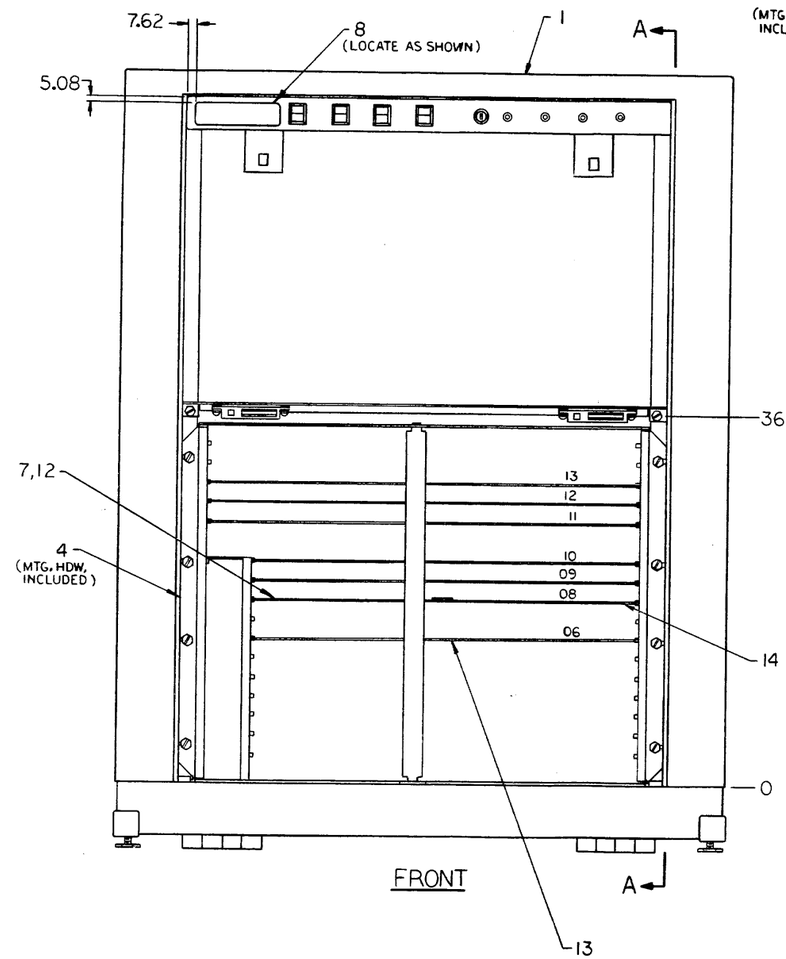
UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ± .005	.X ± .03	
	.XX ± .02	ANGLES ± 1°	
NAME		TITLE	DATE
J TAMUL		DES / DFT	11-5-81
R. CERO		SUPV	2-19-82
		CHK	
R DENGEL		ENG	2-19-82
P. ABITANTE		MGR	2-19-82
R. BAPKER.		QC	2-19-82

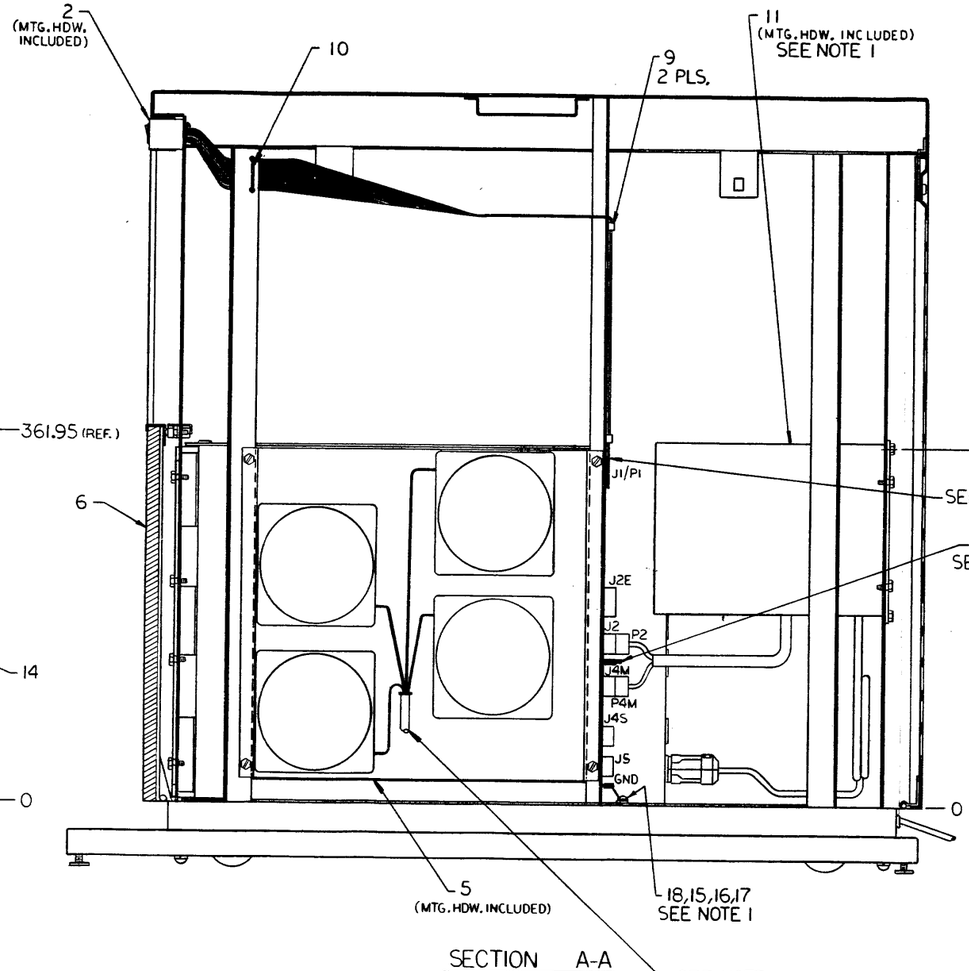
TITLE
SCHEMATIC
CONTROL PANEL

TASK 03131 | SHT 1-1
DWG 09-148 B08

NOTES

MILLIMETERS	INCHES
5.08	.20
7.62	.30
349.25	13.75
361.95	14.25





REVISIONS		
PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	9-29-81
	PROD MJA	9/25/81

IN AREA J5, FAN ASS'Y WAS PICTORIALLY SHOWN MOUNTED TO CABINET FROM INSIDE.

VT	GAF	4913	R	12-8-81	R01

RELEASED FOR PRODUCTION
MFG. ENG. MJA DATE 12/8/81

METRIC

USED IN MANUAL 47-022

UNLESS OTHERWISE SPECIFIED		
SCALE: ~	TOLERANCE: MILLIMETERS	INCHES
DIMENSIONS ARE IN MILLIMETERS	.XX ± .13 .X ± .5 X. ± .8	.XXX ± .005 .XX ± .02 .X ± .03

NAME	TITLE	DATE
J. TAMUL	DES / DFT	9-5-81
R. CERO	SUPV	12-18-81
	CHK	
D. FOGGIA	ENG	12-18-81
P. ABITANTE	MGR	12-18-81
R. BARKER	QC	12-17-81

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PART NO	DESCRIPTION
01-196F02	INTERNATIONAL
~~01-196F01~~	~~DOMESTIC~~

VARIATION TABLE

NOTES 1. SEE 01-196 D12, SHT. 3 FOR TERMINATION OF CABLES.

00	01	REV. LEVEL
D	D	SHEET SIZE

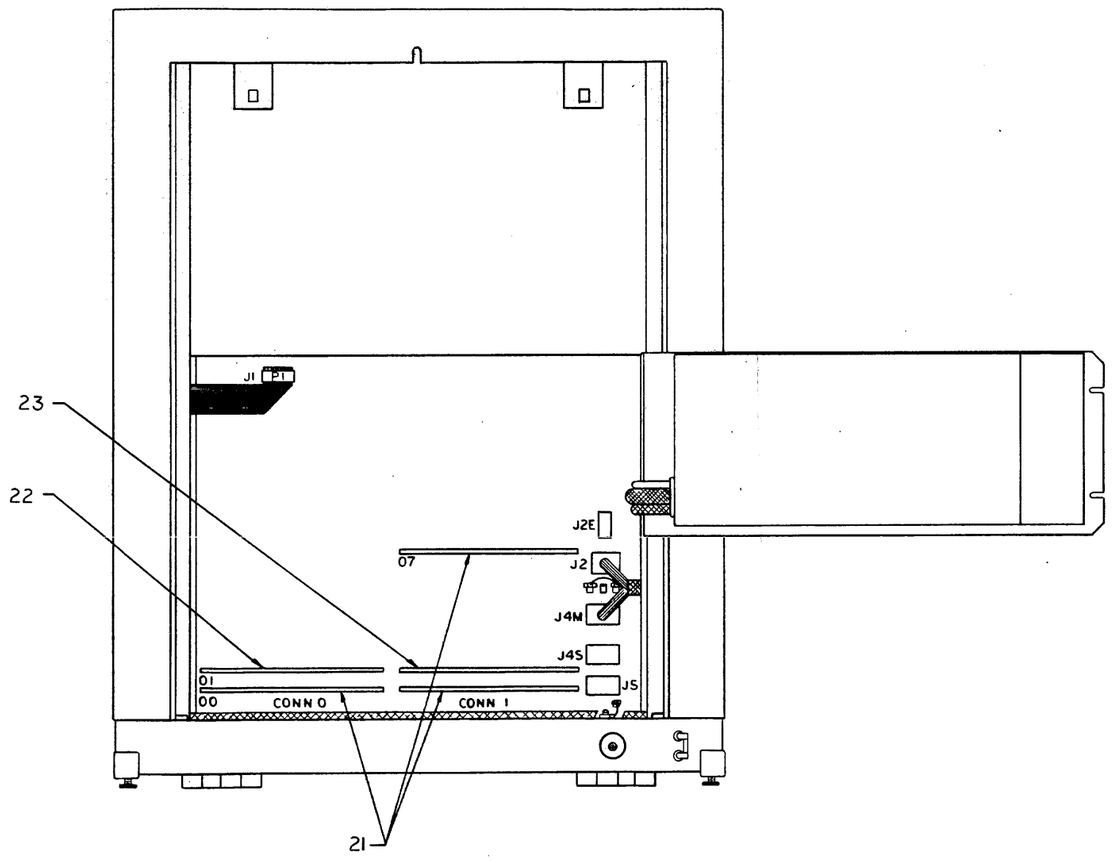
REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT

TITLE ASSEMBLY, BASIC SYSTEM CABINET W/O DFU MOD 3210, 208V

TASK	03175	SHT
DWG	01-196 R01 D03	1 - 2

IRRUNNING 44-131 40579

REVISIONS



REAR VIEW

NOTES

DRAFTER	J TAMULEVICIUS
DATE	9-2-81

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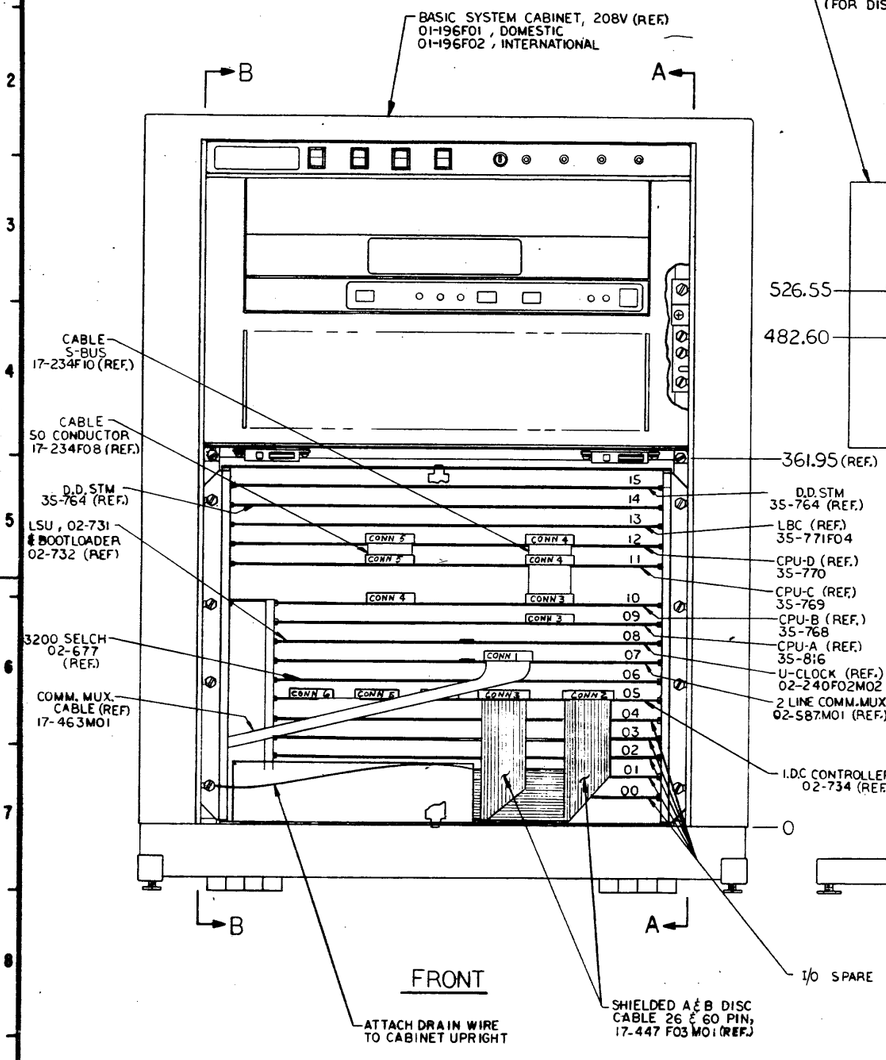
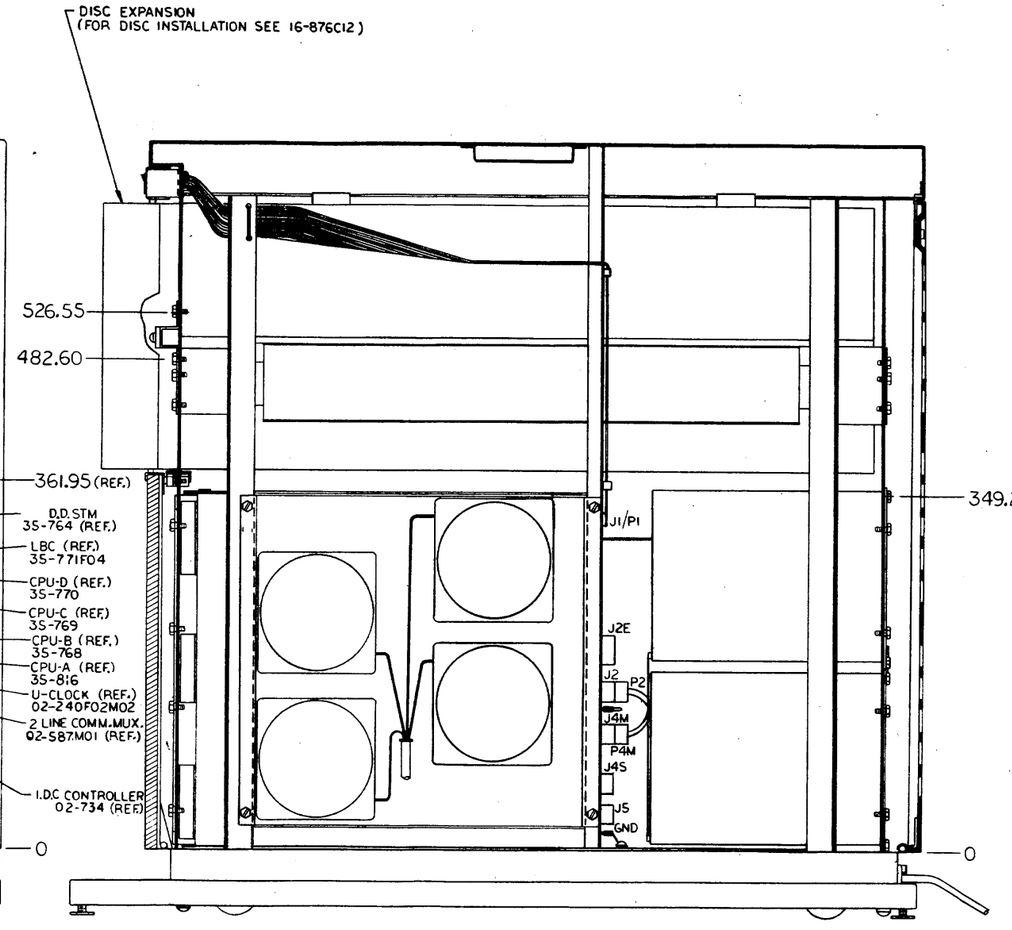
TITLE ASSEMBLY , BASIC SYSTEM CABINET W/O DFU MOD 3210 , 208V

TASK 03175		SHT 2-2
DWG 01-196	D03	

MILLIMETERS	INCHES
526.55	20.75
482.60	19.00
361.95	14.25
349.25	13.75





REVISIONS			
PRE PRODUCTION APPROVAL	INIT	DATE	
	DEV	9-25-81	
	PROD	9/25/81.	

IN AREA F6, CPU-A (REF.) WAS 35-798

VT		4803	R	12-8-81	R01

IN AREA J5, FAN. ASS'Y WAS PICTORIALLY SHOWN MOUNTED TO CABINET FROM INSIDE, REVISED SHT. 3

VT	GJF	4913	R	12-8-81	R02	X

RELEASED FOR PRODUCTION
MFG. ENG. MJG DATE 12/16/81

EXTENSIVE CHANGE MADE: SEE MICRO FILM R02: REV'D SHTS 2 & 3:

JAH	JV	5050	R	9-7-82	R03

METRIC

USED IN MAUNAL 47-022

UNLESS OTHERWISE SPECIFIED

SCALE: ~ TOLERANCE:

DIMENSIONS ARE IN MILLIMETERS

MILLIMETERS	INCHES
.XX ±.13	.XXX ±.005
.X ±.5	.XX ±.02
X ±.8	.X ±.03

NAME		TITLE	DATE
J. TAMUL		DES/DFT	9-10-81
R. CERO		SUPV	12-18-81
		CHK	
D. FOGGIA		ENG	12-18-81
P. ABITANTE		MGR	12-18-81
R. BARKER		QC	12-17-81

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BASIC CABINET

SHEET NO.	1	2	3
REV. LEVEL	3	1	2
SHEET SIZE	D	D	D

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

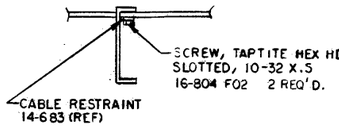
NOTES

TITLE
INFORMATION DWG.
W/O DFU
MOD 3210 , 208V

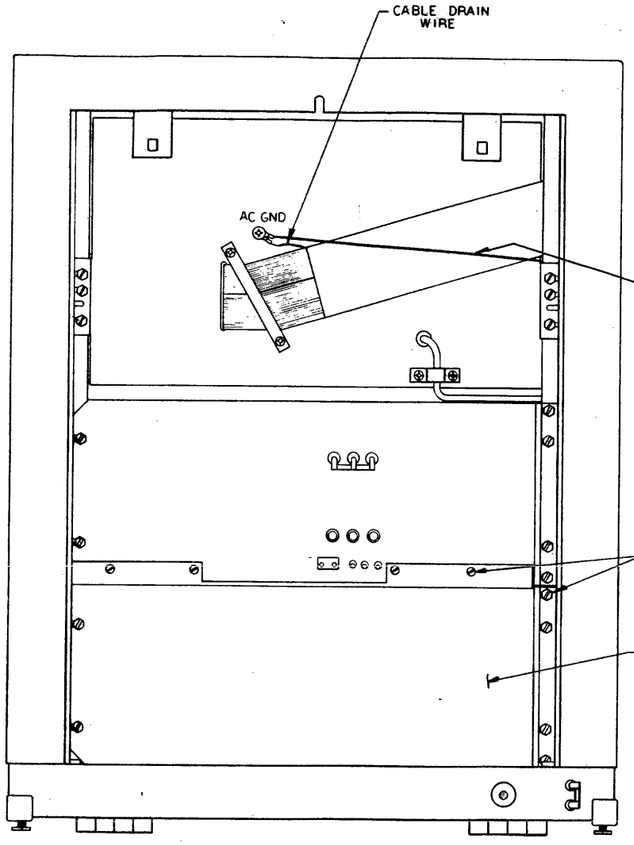
TASK 03175 SHT 1-3
DWG 01-196 R03 D12

DRAWING 44-131-4079

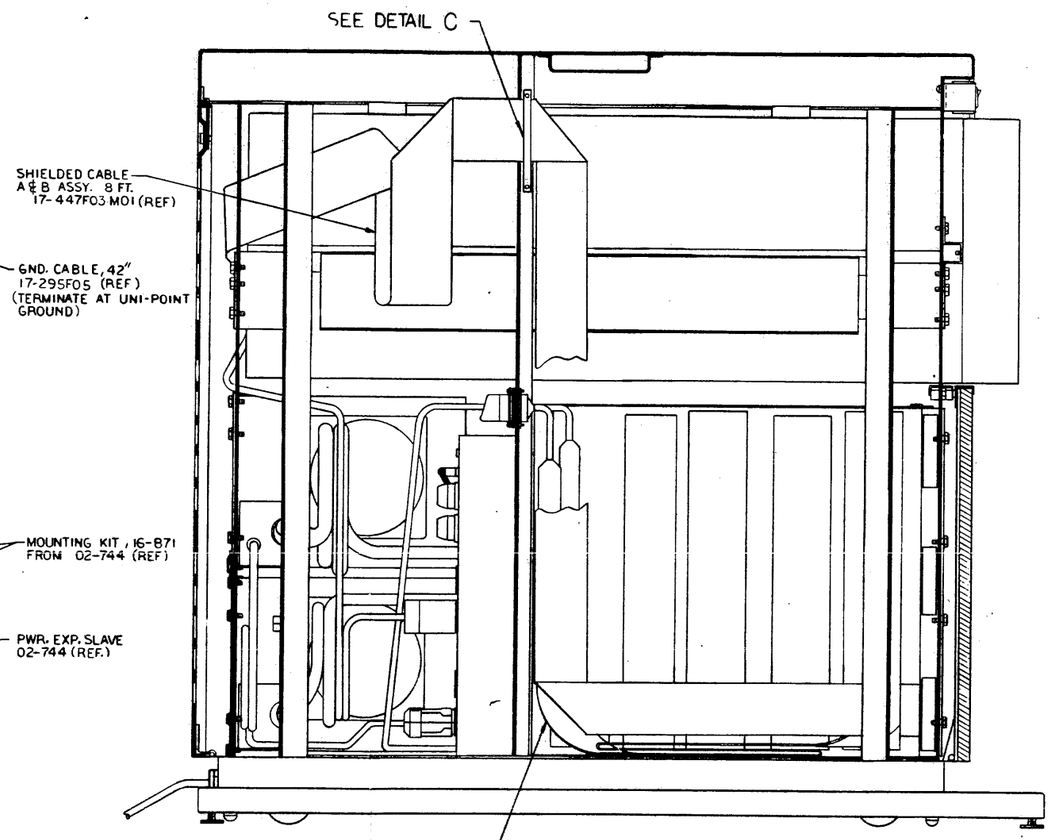
REVISIONS					
EXTENSIVE CHANGES MADE: SEE MICRO,FILM ROD:					
JAH	GJ	5050	R	4-7-82	R01



DETAIL C



REAR



SECTION B-B

BASIC CABINET

NOTES

DRAFTER	J TAMULEVICIUS
DATE	9-11-81

PERKIN-ELMER

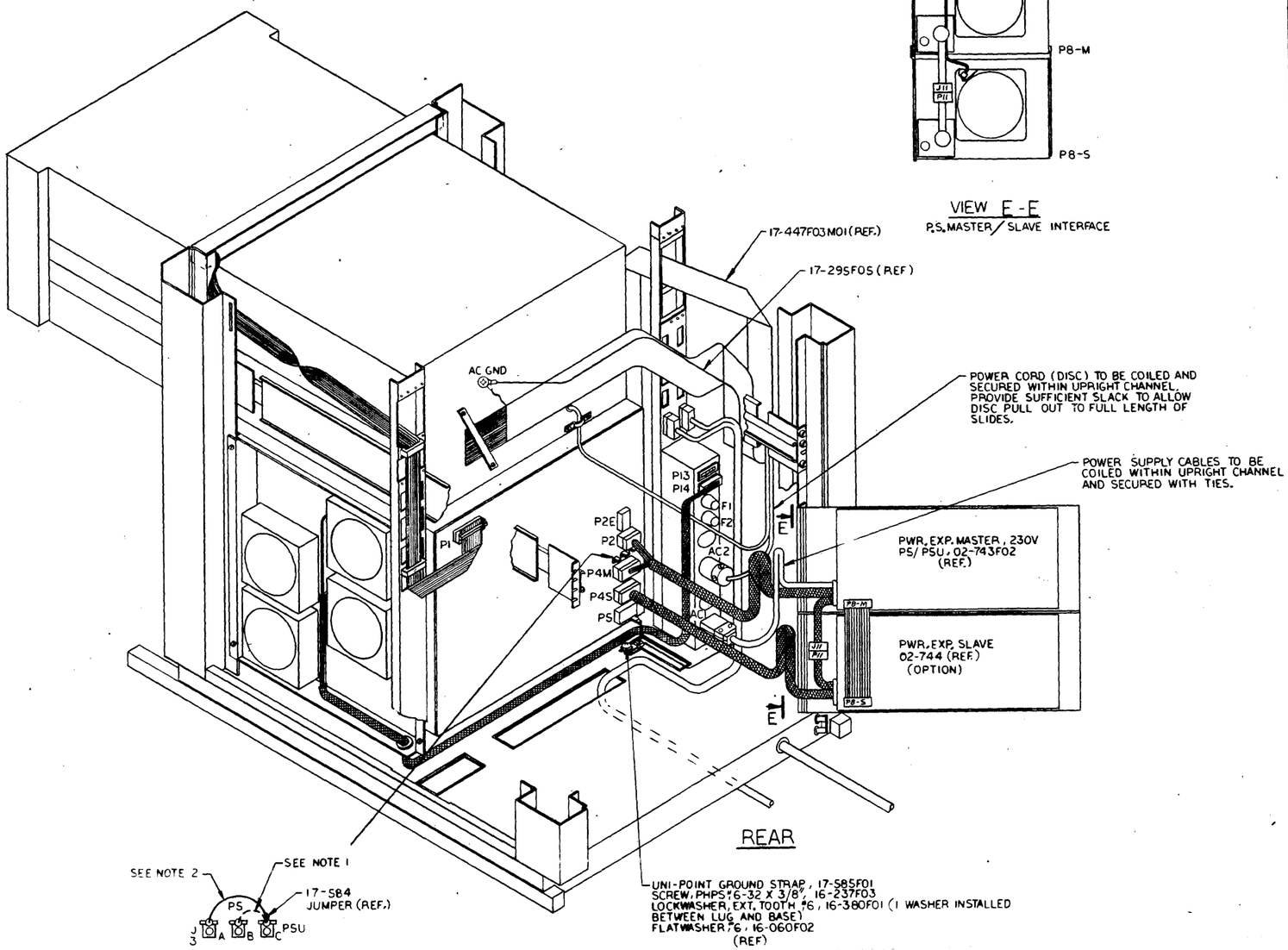
Computer Systems Division
Oceanport, N.J. 07757

TITLE
INFORMATION DWG.
MOD 3210, 208V

TASK 03175		SHT 2-3
DWG 01-196 R01	D12	

BRUNING 5-14-131 6097-2

REVISIONS						
AREA E6, FAN ASS'Y WAS PICTORIALLY SHOWN MOUNTED TO CABINET FROM INSIDE.						
VT	CJF	4913	R	12-8-81	R01	X
EXT. CHANGES MADE: SEE MICRO FILM R01						
JAH	JH	5050	R	4-7-82	R02	



VIEW E-E
P.S. MASTER / SLAVE INTERFACE

BASIC CABINET

NOTES
1. CONNECT B TO C, TO POWER PSU FROM PS IF P.S. 02-743F01 (PS ONLY) IS USED.
2. CONNECT A TO C, WHEN P.S. 02 743F02 (PS/PSU) IS USED.

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DRAFTER	J TAMULEVICIUS
DATE	9-15-81

TITLE
INFORMATION DWG.
MOD 3210, 208V

TASK	03175	SHT
DWG	01-196 R02 D12	3-3

REVISIONS		
PRE PRODUCTION APPROVAL	INIT.	DATE
	DEV	4-15-81
	PROD	4/15/81

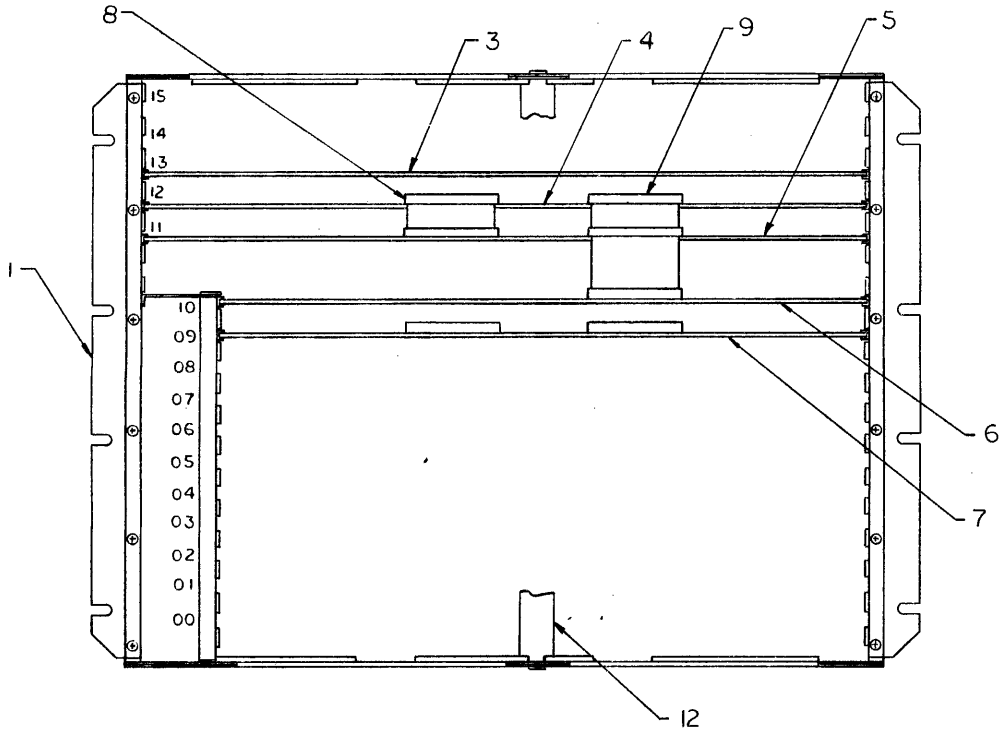
AREA C2-G2 DELETED
ITEM 2. ADDED ITEM 12

JH	WP	4715	R	5-12-81	R01

RELEASED FOR PRODUCTION
MFG. ENG. [signature] DATE 9-16-81
DO NOT MANUFACTURE W/O / UTH.

SUPERSEDED
BY PART NO. 11-298 M01
PER ECN NO. 5184
BY KR DATE 10-5-82

KR		5184	R	10-5-82	R02



FRONT VIEW

NOTES

UNLESS OTHERWISE SPECIFIED			
SCALE: ~	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ± .005 .X ± .03 .XX ± .02 ANGLES ± 1°		
NAME		TITLE	DATE
J TAMUL		DES / DFT	2-21-81
R CERO		SUPV	9-16-81
		CHK	
D FOGGIA		ENG	9-16-81
P ABITANTE		MGR	9-16-81
R BARKER		QC	9-16-81

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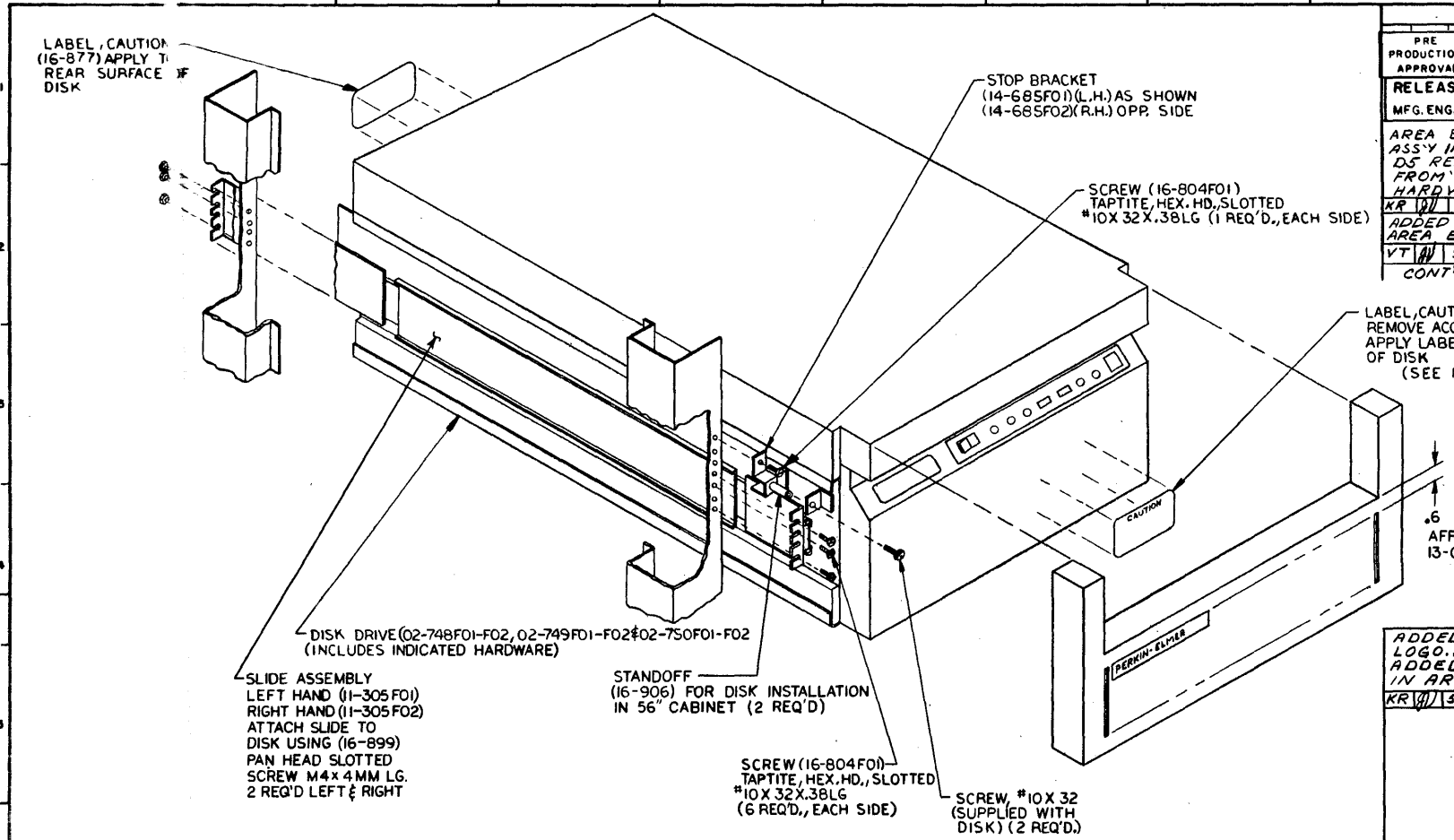
Oceanport, N.J. 07757

TITLE
ASSEMBLY, CPU CHASSIS

TASK	SHT
03175	1-1

DWG 11-298 R02 C03



REVISIONS			
PRE PRODUCTION APPROVAL		INIT	DATE
	DEV	[illegible]	7-2-81
	PROD	[illegible]	7/2/81

RELEASED FOR PRODUCTION
MFG. ENG. [illegible] DATE 12/9/81

AREA B5 ADDED SLIDE ASSY INFORMATION. AREA D5 REMOVED "SLIDES AND FROM" INCLUDES INDICATED HARDWARE.

KR	[illegible]	4970	R	3-29-82	R01

ADDED STANDOFF TO AREA E-4

VT	[illegible]	5021	R	4-22-82	R02

CONT'D IN AREA J5

ADDED DIM ".6 & AFFIX LOGO..." IN AREA J4. ADDED LOGO PLATE IN AREA H4.

KR	[illegible]	5142	R	10-7-82	R03

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NOTES
1. INSTALLATION PROCEDURE TYPICAL BOTH SIDES.
2. PRIOR TO INSTALLING DISK IN CABINET, THE 4 LEVELERS ON THE UNDERSIDE OF STABILIZER LEGS MUST BE ADJUSTED TO MAKE SECURE CONTACT WITH THE FLOOR.
3. ALL CABINETS REQUIRING THIS DISK MUST BE FITTED WITH STABILIZER LEGS (FOR 56" CABINET USE 16-832).

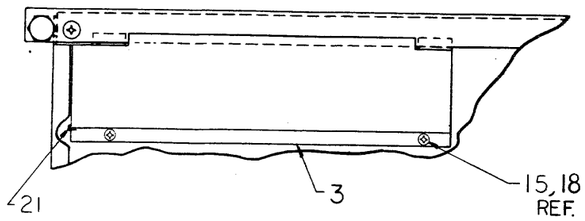
UNLESS OTHERWISE SPECIFIED
SCALE: ~
TOLERANCE: DIMENSIONS ARE IN INCHES .XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME	TITLE	DATE
J TAMUL	DES/DFT	5-14-81
R. CERO	SUPV	12-8-81
	CHK	
D. FOGGIA	ENG	12-8-81
P. ABITANTE	MGR	12-8-81
R. BARKER	QC	12-4-81

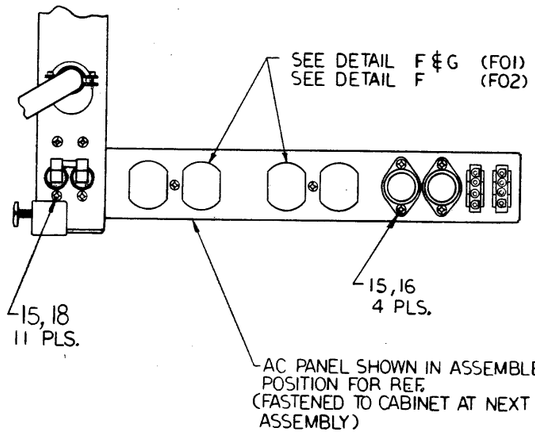
TITLE
INFORMATION DRAWING
DISK INSTALLATION

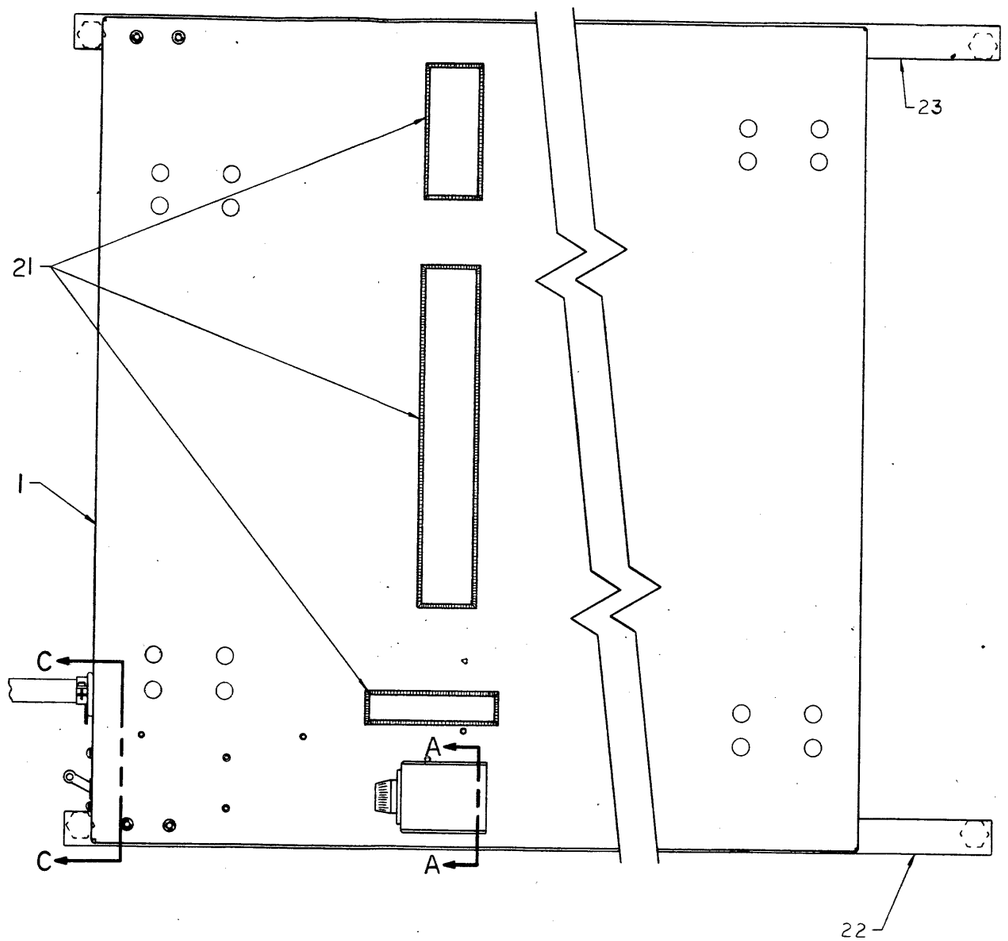
TASK 0317S SHT 1-1
DWG 16-876 R03 C12

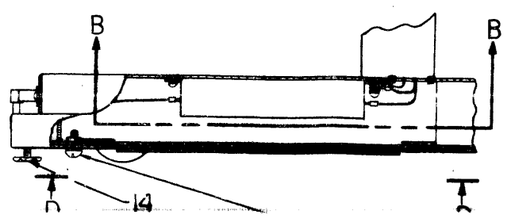
BRUNING 44-131 40579



PARTIAL VIEW D-D







REVISIONS				
PRE PRODUCTION APPROVAL	INIT	DATE		
	DEV	4-15-81		
	PROD	4/15/81		

EXTENSIVE CHANGES FOR PREVIOUS CHANGES SEE R00 MICROFILM COPY. REVISED SHT'S 2&3

JT	PHM	4783	R	8-21-81 R01

REVISED SHTS 2&3

JT	BWC	4852	R	9-16-81 R02

RELEASED FOR PRODUCTION

MFG. ENG. _____ DATE 9-17-81

REVISED SHT'S 2 & 3

EJC		4884	R	12-22-81	R03

SUPERSEDED BY 11-296 M01 D03 PER 4976 BY JAH 2/19/82

REV'D SHTS 2 & 3:

JAH		4976	R	7-19-82	R04

USED IN MANUAL 47-022

UNLESS OTHERWISE SPECIFIED			
SCALE: ~	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	J TAMUL	DES / DFT	12-30-80
R. CERO		SUPV	9-15-81
		CHK	
D. FOGGIA		ENG	9-15-81
P. ABITANTE		MGR	9-15-81
R. BARKER		QC	9-15-81

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Computer Systems Division
Oceanport, N.J. 07757

PART NO.	DESCRIPTION
	VARIATION TABLE
11-296 F02	AS SHOWN PER SHTS. 1 & 3 , INTERNATIONAL 208 V
11-296 F01	~~AS SHOWN PER SHTS. 1 & 3 , DOMESTIC 208V~~

NOTES

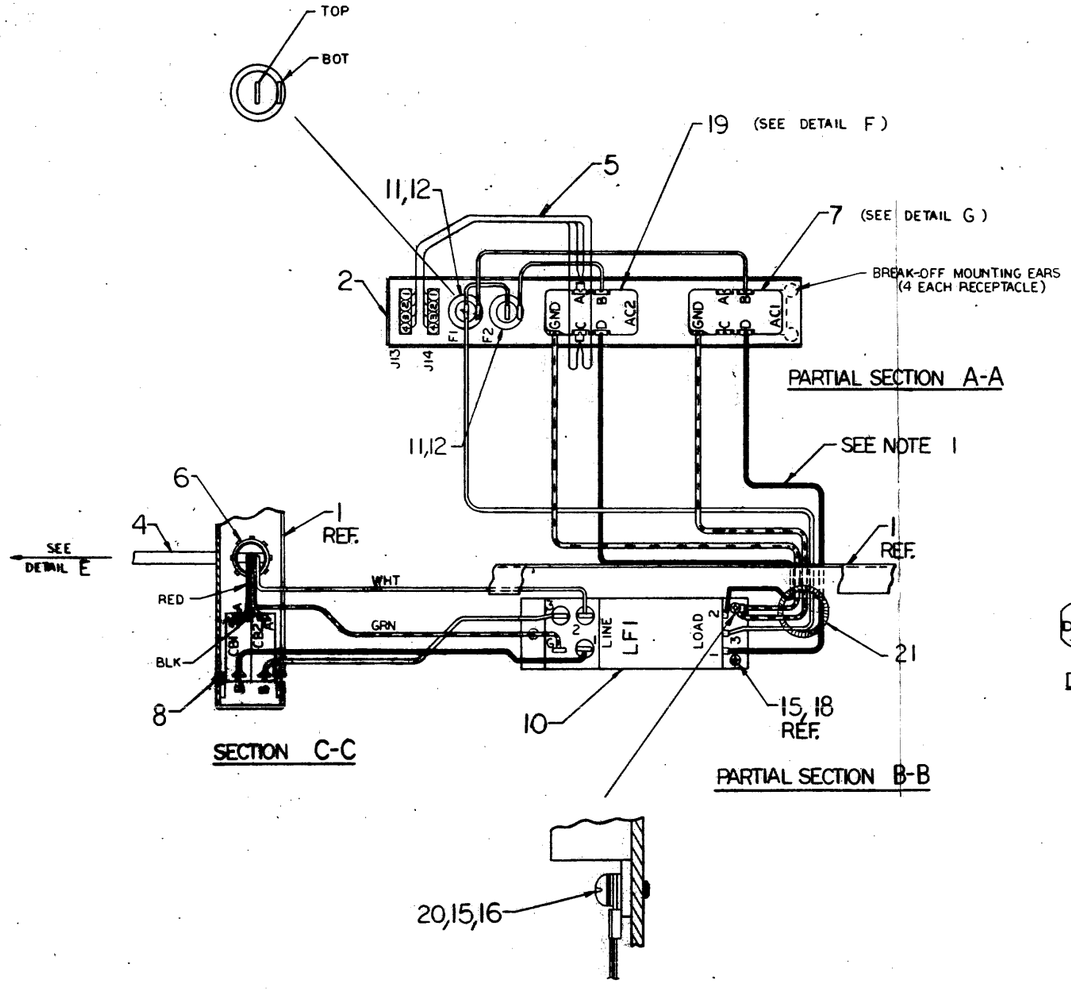
04	04	04	REV. LEVEL
D	D	D	SHEET SIZE

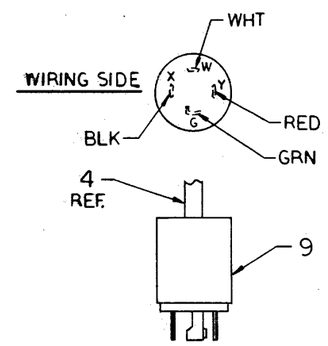
THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

TITLE
ASSEMBLY , BASE PAN

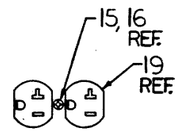
TASK 03175
DWG 11-296 R04 D03

SHT 1-3

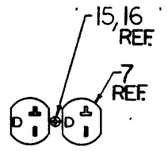




DETAIL E



DETAIL F
(115 VAC)



DETAIL G
(250 VAC)

REVISIONS					
EXTENSIVE CHANGES FOR PREVIOUS CHANGES SEE R00 MICROFILM COPY					
		4783	R		R01
AREA C2, ADDED VIEW OF F1 CHANGED WIRING LF1-3 WAS TO F1-BOT, AC1-B WAS TO F1-TOP, AC2-B WAS TO F2-TOP, F1-TOP TO F2-TOP WAS F1-BOT TO F2-BOT CHANGED DETAIL E					
JT	BWL	4852	R	9-16-81	R02
F1 AT E3 WERE ITEMS 11 & 13 F2 AT E3, DUPLICATE CALL-OUT OF ITEM 11 & 12 WAS REMOVED.					
ECO	JH	4884	R	12-22-81	R03 X
SUPERSEDED 11-296 M01 D23 4976 JAH 7-19-82					
JAH	JH	4976	R	7-19-82	R04 X

208V (DOMESTIC)
11-296F01

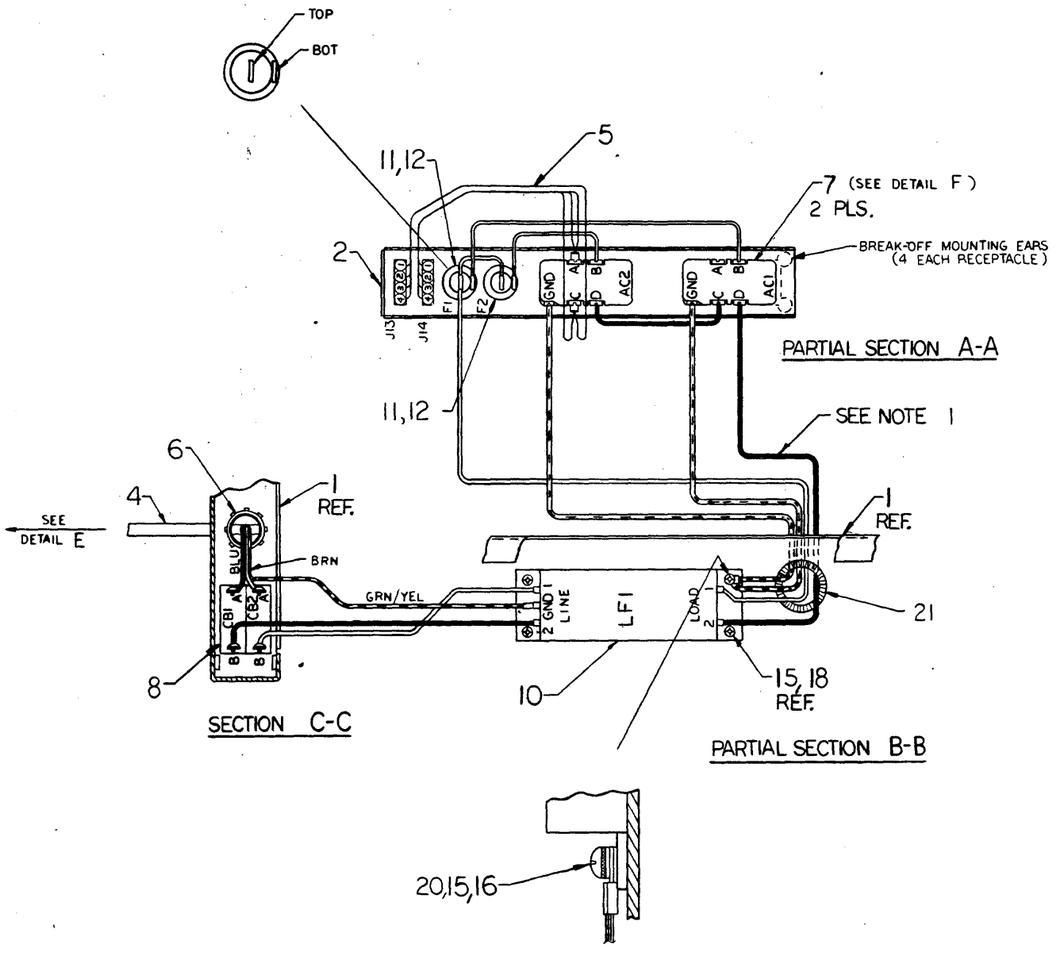
NOTES
1. ALL WIRES SHOWN ARE PART OF ITEM 4, UNLESS OTHERWISE SPECIFIED.

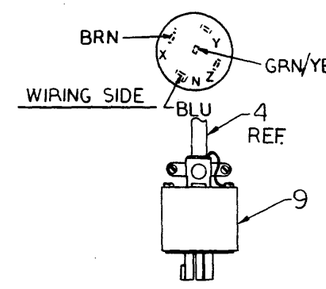
DRAFTER	J TAMULEVICIUS
DATE	12-30-80

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

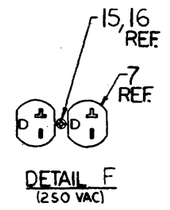
TITLE
ASSEMBLY, BASE PAN

TASK 03175		SHT
DWG 11-296 R04	D03	2 - 3





DETAIL E



DETAIL F
(250 VAC)

208V (INTERNATIONAL)
11-296F02

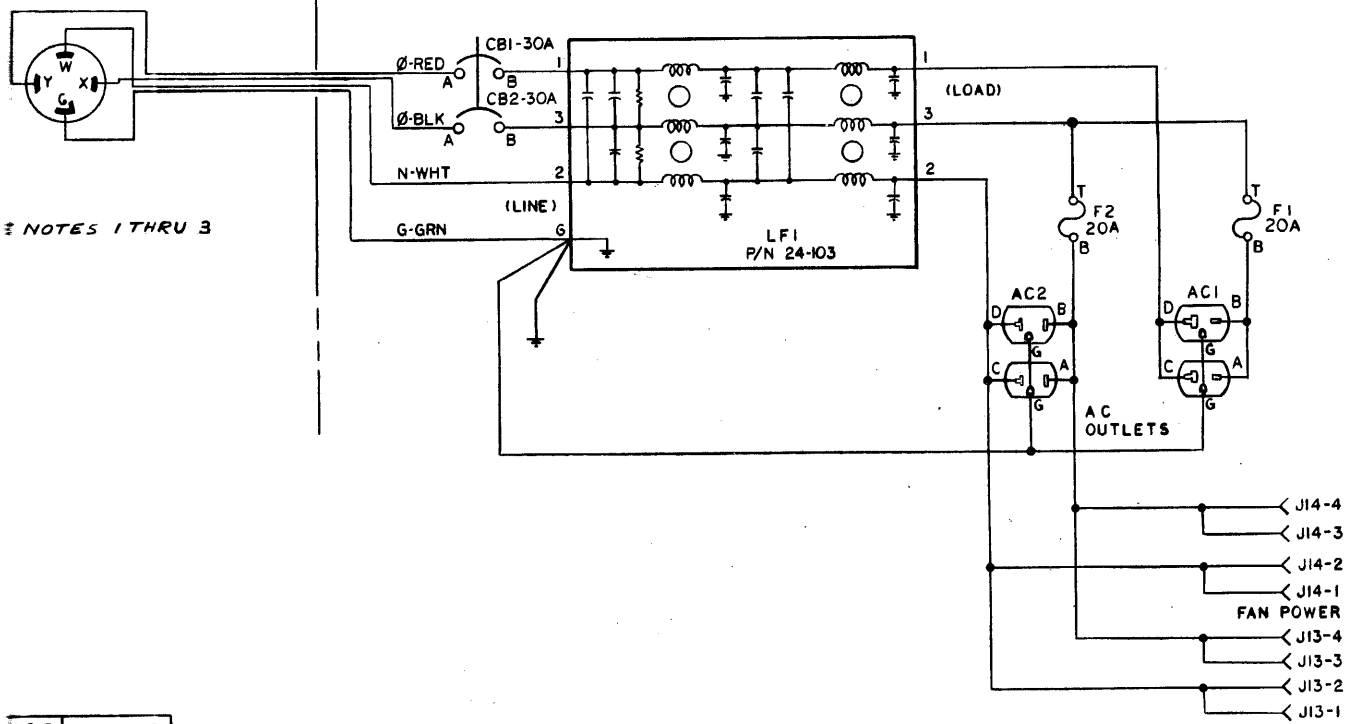
REVISIONS					
EXTENSIVE CHANGES FOR PREVIOUS CHANGES SEE ROO MICROFILM COPY					
	4783	R			R01
AREA C1, ADDED VIEW OF F1, CHANGED WIRING LF1-1 WAS TO F1-BOT, AC1-B WAS TO F1-TOP, AC2-B WAS TO F2-TOP, F1-TOP TO F2-TOP WAS F1-BOT TO F2-BOT, CHANGED DETAIL E					
JT	BWC	4852	R	9-16-81	R02
F1 AT E3 WERE ITEMS 11 & 13.					
EC J	GV	4884	R	12-22-81	R03 X
SUPERSEDED 11-296 MDI.023 4976 JAH 7/19/82					
JAH	GV	4976	R	7-19-82	R04 X

NOTES
1. ALL WIRES SHOWN ARE PART OF ITEM 4 , UNLESS OTHERWISE SPECIFIED.

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE
ASSEMBLY , BASE PAN

DRAFTER	TASK	SHT
J. TAMULEVICIUS	03175	3 - 3
DATE	DWG 11-296R04 D03	
12-30-80		



SEE NOTES 1 THRU 3

	P-E PART NUMBER	SIMILAR ITEM
F1	24-0 F02	SC-20A
F2	24-0 F02	SC-20A

DOMESTIC MODEL, (11-296 F01)

11-296 F02	INTERNATIONAL	SHEET 2
11-296 F01	DOMESTIC	SHEET 1
PART #	DESCRIPTION	SCHEMATIC ON

VARIATION TABLE

REV LEVEL	3
SHT NO	1

NOTES
1. PLUG EQUIPED IS NEMA TYPE L14-30P.
2. PLUG EQUIPED IS HUBBELL #2711 OR EQUIVALENT (FOR REF. ONLY).
3. THIS PANEL IS INTENDED FOR APPLICATIONS POWERED BY A 120/208 VAC, 60HZ, 3 POLE, 4 WIRE GROUNDING SOURCE.

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
DEV	C&C	6/5/81
PROD	MJA	6/12/81

AREAS G4 & H4, REVISED SHOWING OF AC1 & AC2. AREA A6, ADDED VIEW "A-A". AREA A7, ADDED REV TABLE. AREA K6, ADDED NOTE.

REVISED SHEET 2.

JRB	BNL	4806	M	8-18-81	R01

AREA B3 CHANGED VIEW OF PLUG ADDED T AND B TO F1 AND F2, F2 WAS 15A, REVISED SHT. 2

JT	BNL	4852	R	9-16-81	R02

RELEASED FOR PRODUCTION
DEV. ENG. C&C DATE 9/18/81

F1 AT H3 WAS 15A.
INFO. TABLE AT B6 WAS:
F1, 24-105 F02 FNW 15A
F2, 24-105 F03 FNW 20A

EC	91	4884	R	12-22-81	R03

USED IN MANUAL 47-022

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

UNLESS OTHERWISE SPECIFIED
SCALE: NONE
TOLERANCE: .XXX ± .003 .X ± .03 .XX ± .02 ANGLES ± 1°
DIMENSIONS ARE IN INCHES

NAME	TITLE	DATE
W. FRASER	DES / DFT	6-10-81
R. CERO	SUPV	9-15-81
	CHK	
E. CENTOFANTI	ENG	9-15-81
P. LIOIO	MGR	9-15-81
R. BARKER	QC	9-15-81

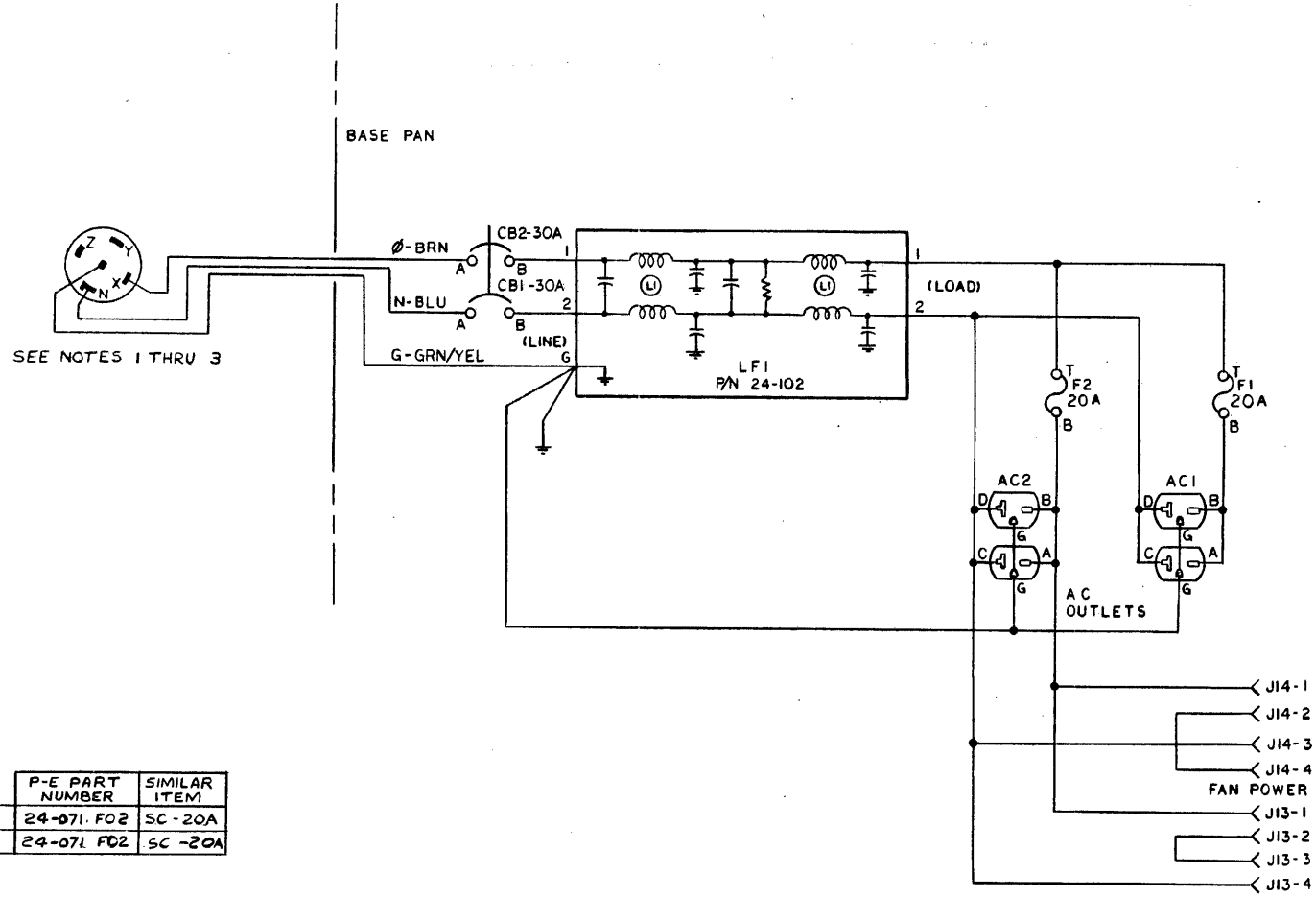
PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE
SCHEMATIC
BASE PAN ASS'Y
(DOMESTIC MDL)

TASK 03175
DWG 11-296 R03 C08
SHT 1 - 2

BRUNING 44-131 40579

REVISIONS					
AREA A3 & A4, ADDED SECTION A-A & REVISED VIEW TO REFLECT WIRING VIEW.					
BWL	JAB	4806	M	8-19-81	R01
AREA B3 CHANGED VIEW OF PLUG. ADDED T AND B TO F1 AND F2, F2 WAS 15A.					
JT	BWL	4852	R	9-16-81	R02
F1 AT H3 WAS 15A. INFO. TABLE AT B6 WAS: F1, 24-105 F02 FNW 15A F2, 24-105 F03 FNW 20A					
EJ		4884	R	12-22-81	R03 X



	P-E PART NUMBER	SIMILAR ITEM
F1	24-071. F02	SC-20A
F2	24-071 F02	SC-20A

INTERNATIONAL MODEL, (11-296 F02)

NOTES
1. PLUG EQUIPPED IS NOT A NEMA STANDARD
2. PLUG EQUIPPED IS HUBBELL #4511S OR EQUIVALENT (FOR REF ONLY).
3. THIS PANEL IS INTENDED FOR APPLICATIONS POWERED BY A 200 TO 240 VAC, 50 HZ., 2 POLE, 3 WIRE GROUNDING SOURCE.

UNLESS OTHERWISE SPECIFIED			
SCALE: NONE	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ± .003 .XX ± .02	.X ± .03 ANGLES ± 1°	
NAME		TITLE	DATE
W. FRASER		DES / DFT	6-10-81
R. CERO		SUPV	9-15-81
		CHK	
E. CENTOFANTI		ENG	9-15-81
P. LIOIO		MGR	9-15-81
R. BARKER		QC	9-15-81

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE SCHEMATIC
BASE PAN ASS'Y.
(INT'N'L. MDL.)

TASK 03175 SHT 2-2

DWG 11-296 R03 C08

BRUNING 44-131 40579

MILLIMETER	INCHES
38.70	1.5
162.56	6.4
2.54	0.1

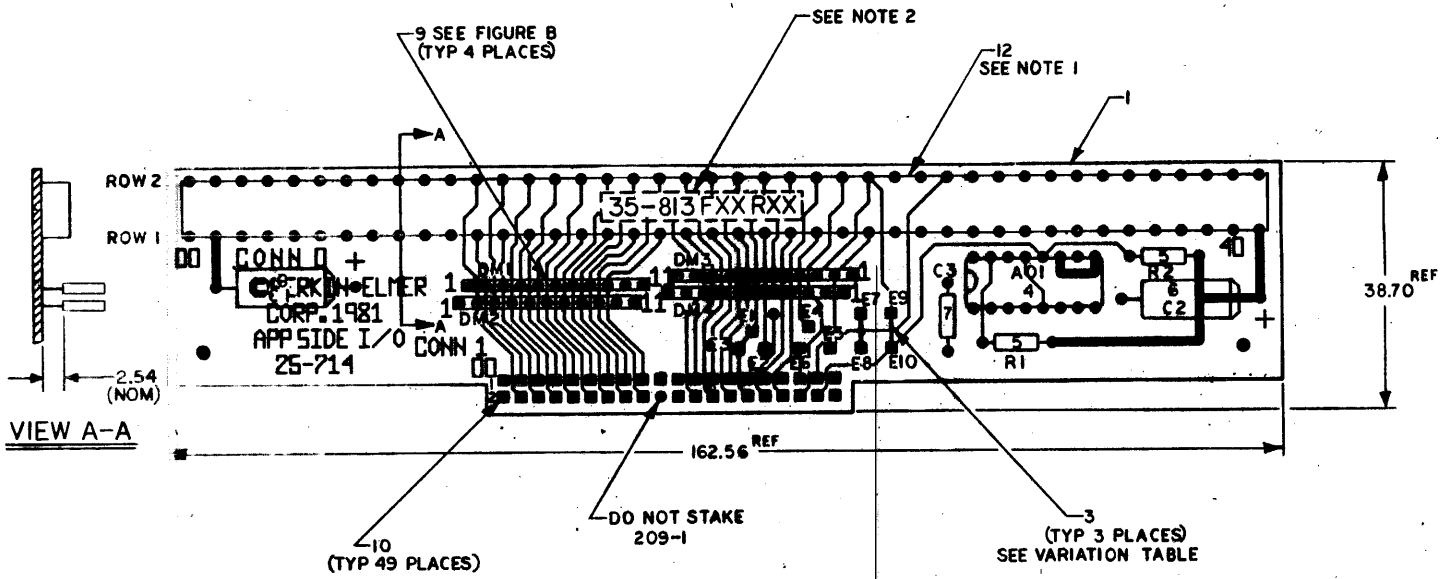
REVISIONS		
	INIT	DATE
PRE-PRODUCTION APPROVAL	DEV	7-21-81
	PROD	7/24/81

RELEASED FOR PRODUCTION
MFG. ENG. _____ DATE 9-16-81

DO NOT MANUFACTURE W/O AUTH.

SUPERSEDED
B. PART NO. 35-813 M01
PER ECN NO. 5043
BY KR DATE 5-7-82

KR	5043	R	5-7-82	R01



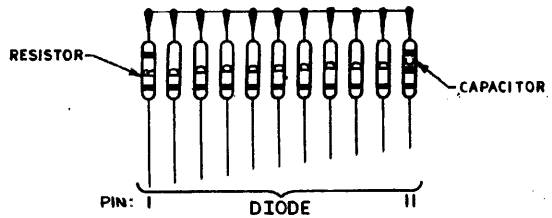


FIGURE B

METRIC

USED IN MANUAL: 47-022

F02	AS SHOWN, STRAP E1-E3 ONLY
F01	AS SHOWN LESS ITEMS 4&5, STRAP E7-E8, E9-E10 ONLY

VARIATION TABLE

NOTES:
1. BEND PINS CLOSEST TO EDGE OF BOARD INWARD PRIOR TO SOLDERING
2. FOR BOARD IDENTIFICATION SEE SSP 002-0D

TOLERANCE IN MILLIMETERS	
X	± .8
.X	± .5
.XX	± .13

UNLESS OTHERWISE SPECIFIED

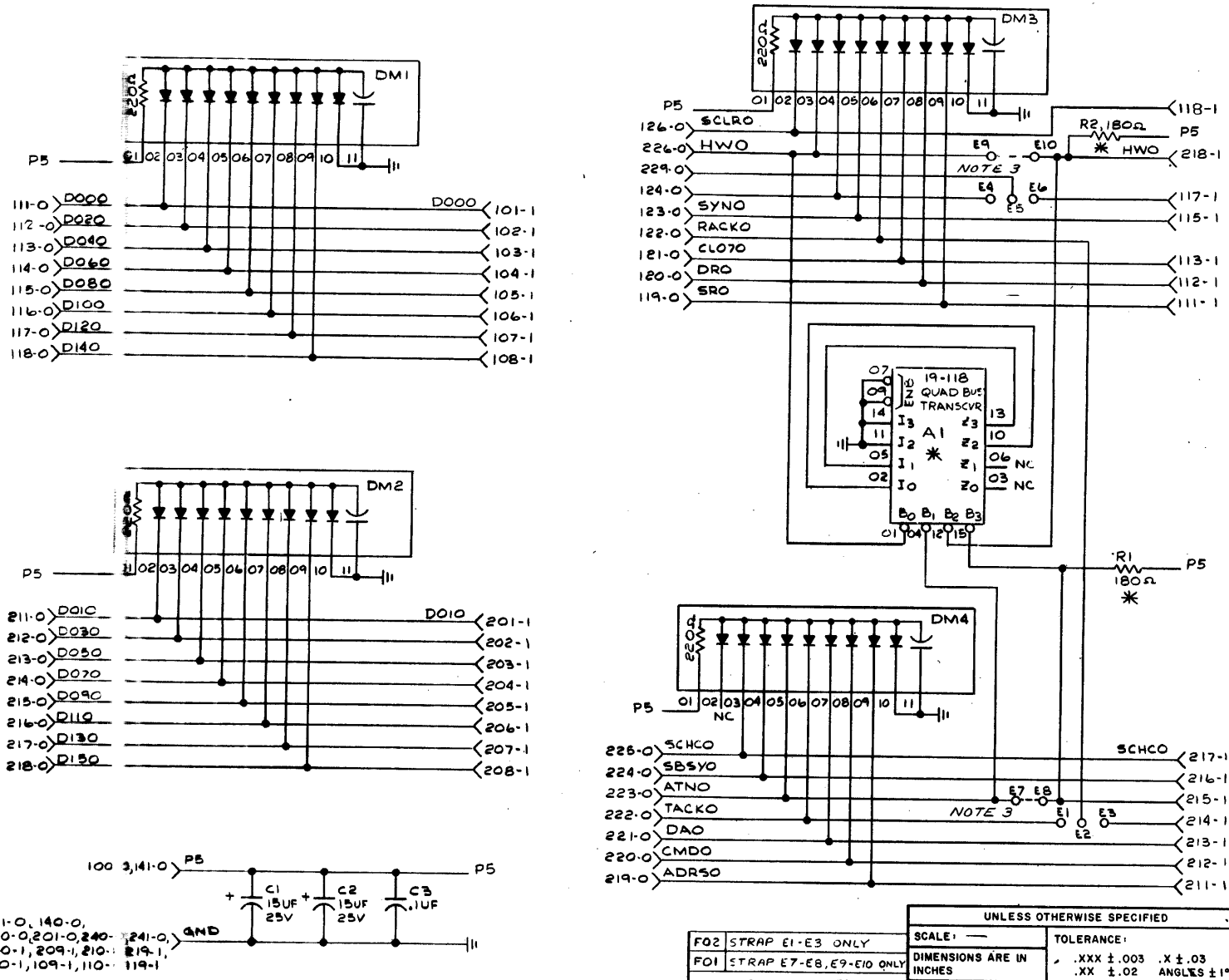
UNLESS OTHERWISE SPECIFIED	
SCALE: 2/1	TOLERANCE IN INCHES
DIMENSIONS ARE IN MILLIMETERS	.XXX ± .005 .X ± .03 .XX ± .02 ANGLES ± 1°

NAME		TITLE	DATE
B.GRAY		DES/DFT	6-17-81
R.CERO		SUPV	9-15-81
		CHK	
M.MANGIONE		ENG	9-15-81
P.OBRDA		MGR	9-15-81
R.BARKER		QC	9-15-81

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE ASSEMBLY
PRINTED CIRCUIT BOARD
I/O
TERM. BOARD

TASK	SHT
03179	1-1
DWG 35-813 R01 C03	



REVISIONS			
PRE PRODUCTION APPROVAL	DEV	INIT MJM	DATE 7-24-81
	ENG		

RELEASED FOR PRODUCTION
DEV. ENG. [signature] DATE 7/11/

DO NOT MANUFACTURE W/O AUTH.

SUPERSEDED
BY PART NO. 35-813 M01
PER ECN NO. 5043
BY KR DATE 5-7-82

KR	5093	R	5-7-82	R01

BOARDS BUILT TO THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL:

35-813	F01	R00
35-813	F02	R00
P/N	FUNCT. VARI.	REVISION

USED IN MANUAL: 47-022

STRAPPING TABLE	
F02	STRAP E1-E3 ONLY
F01	STRAP E7-E8, E9-E10 ONLY

NOTES
1. DIODE MODULES ARE 23-062 F01
2. * DENOTES COMPONENTS USED ON F02 ONLY.
3. STRAPPING FOR F01 ONLY

UNLESS OTHERWISE SPECIFIED
SCALE: —
DIMENSIONS ARE IN INCHES
TOLERANCE: .XXX ±.003 .X ±.03 .XX ±.02 ANGLES ±1°

NAME	TITLE	DATE
B. GRAY	DES / DFT	5-21-81
R. LERO	SUPV	7-15-81
M. CUCINELLI	CHK	7-15-81
M. MANGIONE	ENG	7-15-81
P. DERUA	MGR	7-15-81
R. FERRARA	QC	7-15-81

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

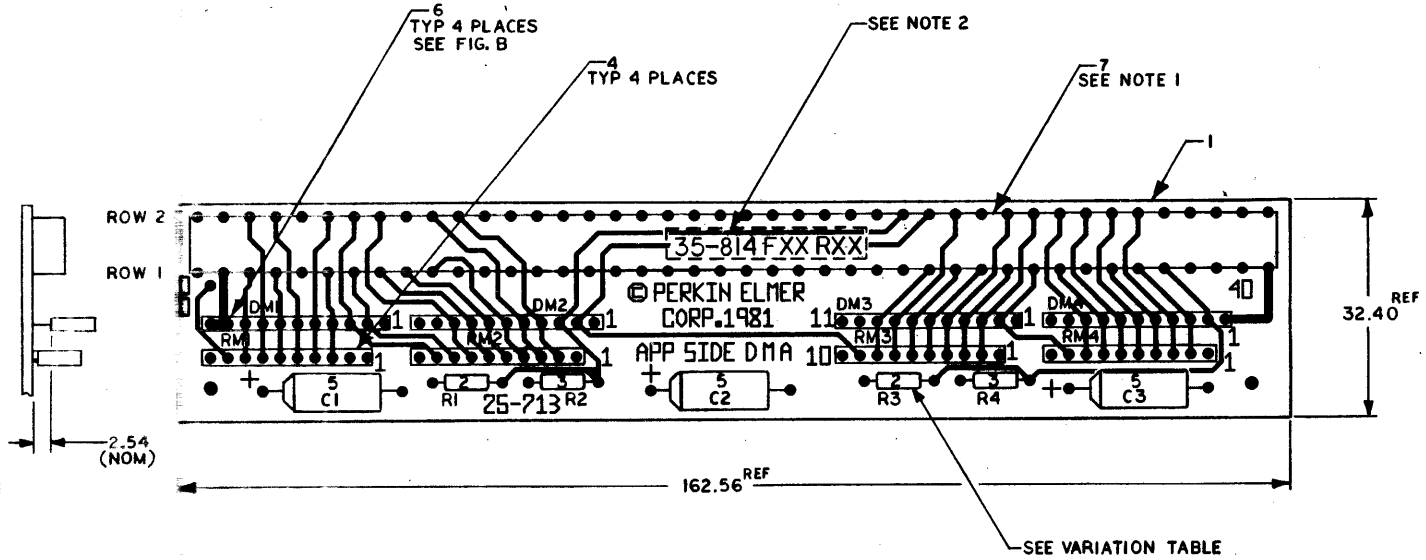
TITLE SCHEMATIC
I/O TERM BOARD

TASK 03179 SHT 1-1
DWG 35-813 R01 C08

BRUNING 44-131 40579

MILLIMETER	INCHES
162.56	6.4
32.40	1.27
2.54	0.1

REVISIONS		
	INIT	DATE
PRE PRODUCTION APPROVAL	DEV MJM	7-24-81
	PROD [illegible]	7/24/81
RELEASED FOR PRODUCTION		
MFG. ENG. [illegible]	DATE 8-10-81	



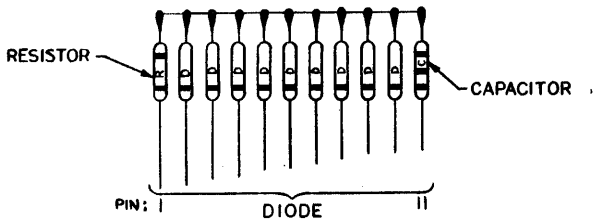


FIGURE B

METRIC

USED IN MANUAL: 47-022

F02	AS SHOWN
F01	LESS DM1, RM1, RM2, R1-R4
VARIATION TABLE	

NOTES:
1. BEND PIN 1 CLOSEST TO EDGE OF BOARD INWARD PRIOR TO SOLDERING
2. FOR BOARD IDENTIFICATION SEE SSP 002-0D

TOLERANCE IN MILLIMETERS	
X	± .8
.X	± .5
.XX	± .13
UNLESS OTHERWISE SPECIFIED	

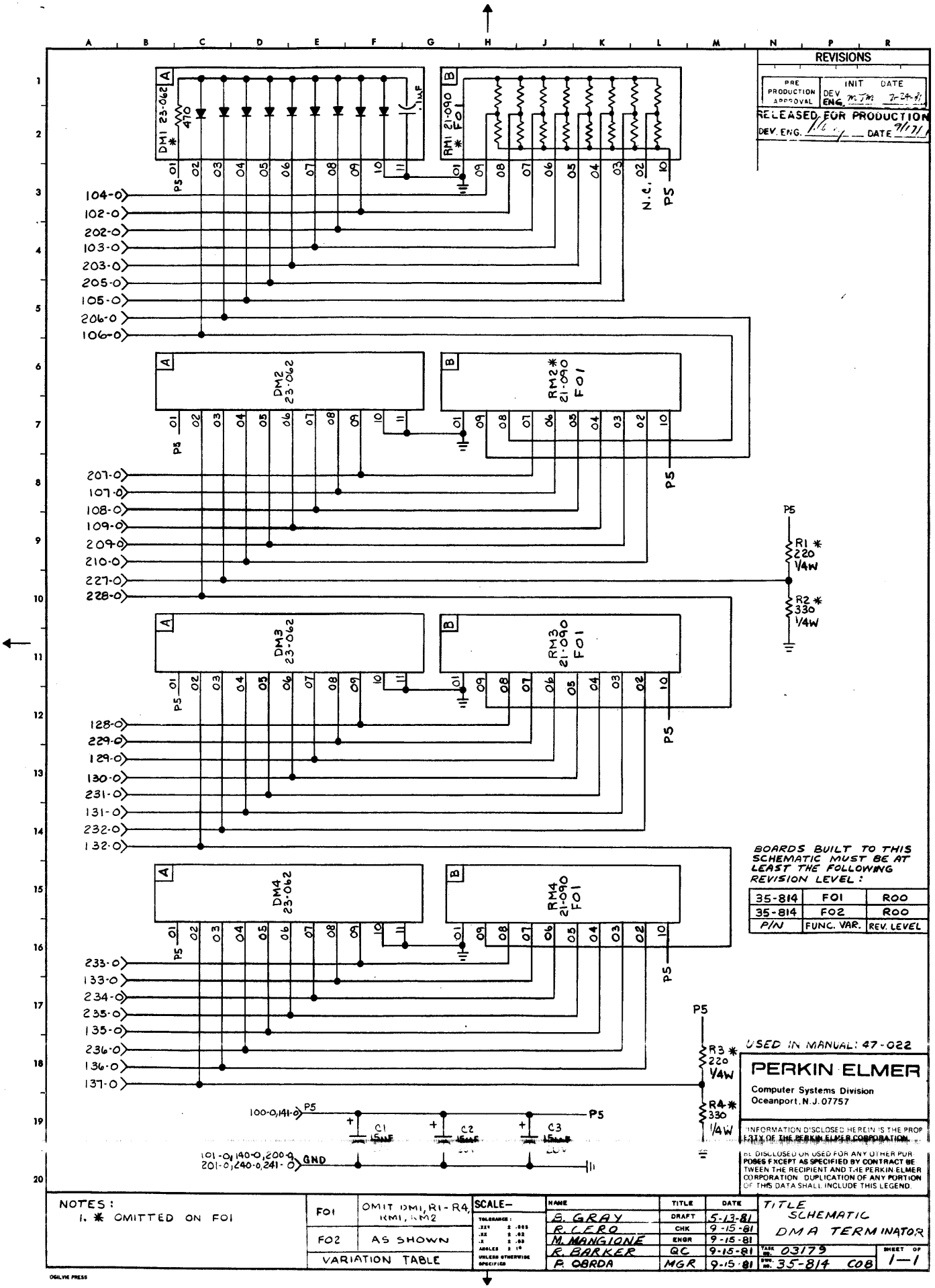
UNLESS OTHERWISE SPECIFIED	
SCALE: 2/1	TOLERANCE IN INCHES
DIMENSIONS ARE IN MILLIMETERS	.XXX ± .005 .X ± .03 .XX ± .02 ANGLES ± 1°

NAME	TITLE	DATE
B.GRAY	DES / DFT	6-12-81
R.CERO	SUPV	9-15-81
	CHK	
M.MANCIONE	ENG	9-15-81
P. OBRDA	MGR	9-16-81
R. BARKER	QC	9-15-81

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE: ASSEMBLY
PRINTED CIRCUIT BOARD
DMA
TERM. BOARD

TASK 03179 | SHT 1-1
DWG 35-814 C03


REVISIONS
PRE PRODUCTION APPROVAL
INIT DATE
DEV. ENG. 7-24-81
RELEASED FOR PRODUCTION
DEV. ENG. DATE 9/17/81
DM1 23-062
RM1 21-090 F01
DM2 23-062
RM2* 21-090 F01
DM3 23-062
RM3 21-090 F01
DM4 23-062
RM4 21-090 F01
P5
N.C.
104-0
102-0
202-0
103-0
203-0
205-0
105-0
206-0
106-0
207-0
107-0
108-0
109-0
209-0
210-0
227-0
228-0
128-0
229-0
129-0
130-0
231-0
131-0
232-0
132-0
233-0
133-0
234-0
235-0
135-0
236-0
136-0
137-0
R1 * 220 1/4W
R2 * 330 1/4W
R3 * 220 1/4W
R4 * 330 1/4W
100-0,141-0
101-0,140-0,200-0
201-0,240-0,241-0
GND
C1
C2
C3
BOARDS BUILT TO THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL :
35-814 F01 R00
35-814 F02 R00
P/N FUNC. VAR. REV. LEVEL
USED IN MANUAL: 47-022
PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757
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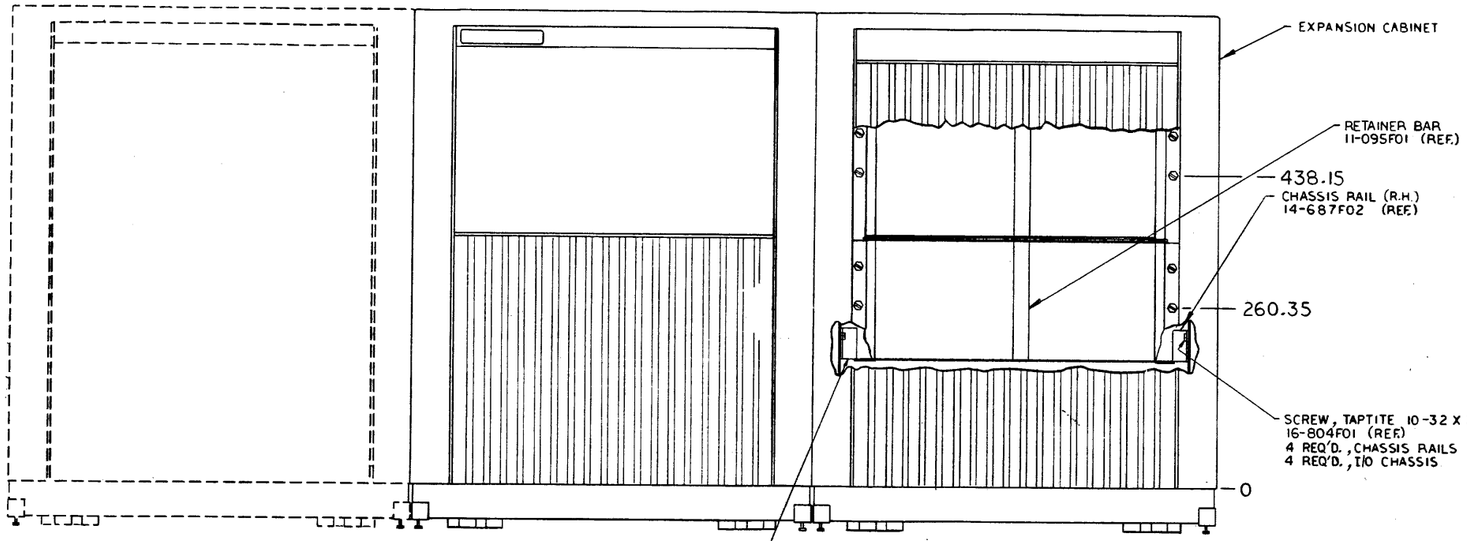
BE DISCLOSED OR USED FOR ANY OTHER PURPOSES EXCEPT AS SPECIFIED BY CONTRACT BETWEEN THE RECIPIENT AND THE PERKIN ELMER CORPORATION. DUPLICATION OF ANY PORTION OF THIS DATA SHALL INCLUDE THIS LEGEND.
NOTES:
1. * OMITTED ON F01
F01 OMIT DM1, R1-R4, RM1, RM2
F02 AS SHOWN
VARIATION TABLE
SCALE—
NAME TITLE DATE
S. GRAY DRAFT 5-13-81
R. CERO CHK 9-15-81
M. MANGIONE ENGR 9-15-81
R. BARKER QC 9-15-81
P. OBRDA MGR 9-15-81
TITLE SCHEMATIC DMA TERMINATOR
TASK NO. 03179
DWG. NO. 35-814 C08
SHEET OF 1—1
OGILVIE PRESS

MILLIMETERS	INCHES
260.35	10.25
438.15	17.25



DISC EXPANSION CABINET

CPU CABINET (FRONT VIEW)

MULTI-I/O CHASSIS EXPANSION CABINET (PREFERRED LOCATION)

REVISIONS					
PRE PRODUCTION APPROVAL	INIT	DATE			
	DEV				
	PROD. MJQ	8/28/81			
EXTENSIVE CHANGES FOR PREVIOUS REV. SEE R00 MICROFILM COPY. REVISED SHT'S. 2,3,4 & 5					
JT	W.P.	4868	R	10-15-81	R01
REVISED SHT'S. 2,3,4,5 & 6 ADDED SHT 7					
JT	CAF	4913	R	12-3-81	R02
RELEASED FOR PRODUCTION MFG. ENG. MJQ DATE 12/9/81					
REV'D SHTS 1 & 4.					
JAH		5122	R	10-5-82	R03
AREA G,H-8, DELETED SECTION A-A: REV'D SHTS 1 & 4.					
JAH		5001	R	10-27-82	R04

METRIC

USED IN MANUAL 47-022

UNLESS OTHERWISE SPECIFIED			
SCALE: 1/4	TOLERANCE: MILLIMETERS / INCHES		
DIMENSIONS ARE IN MILLIMETERS	.XX ± .13	.XXX ± .005	
	.X ± .5	.XX ± .02	
	X. ± .8	.X ± .03	
NAME		TITLE	DATE
J TAMUL		DES/DFT	6-8-81
R CERO		SUPV	12-8-81
		CHK	
R DENGEL		ENG	12-8-81
P ABITANTE		MGR	12-8-81
R BARKER		QC	12-4-81

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

PART NO.	DESCRIPTION
02-752	30" CABINET, SEE SHTS. 1,2 & 3
02-752F01	30" CABINET SEE SHTS. 4,5 & 6

NOTES

02-752 , 30" CABINET

7	6	5	4	3	2	SHEET NO.
00	01	02	04	02	02	REV. LEVEL
D	D	D	D	D	D	SHEET SIZE

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

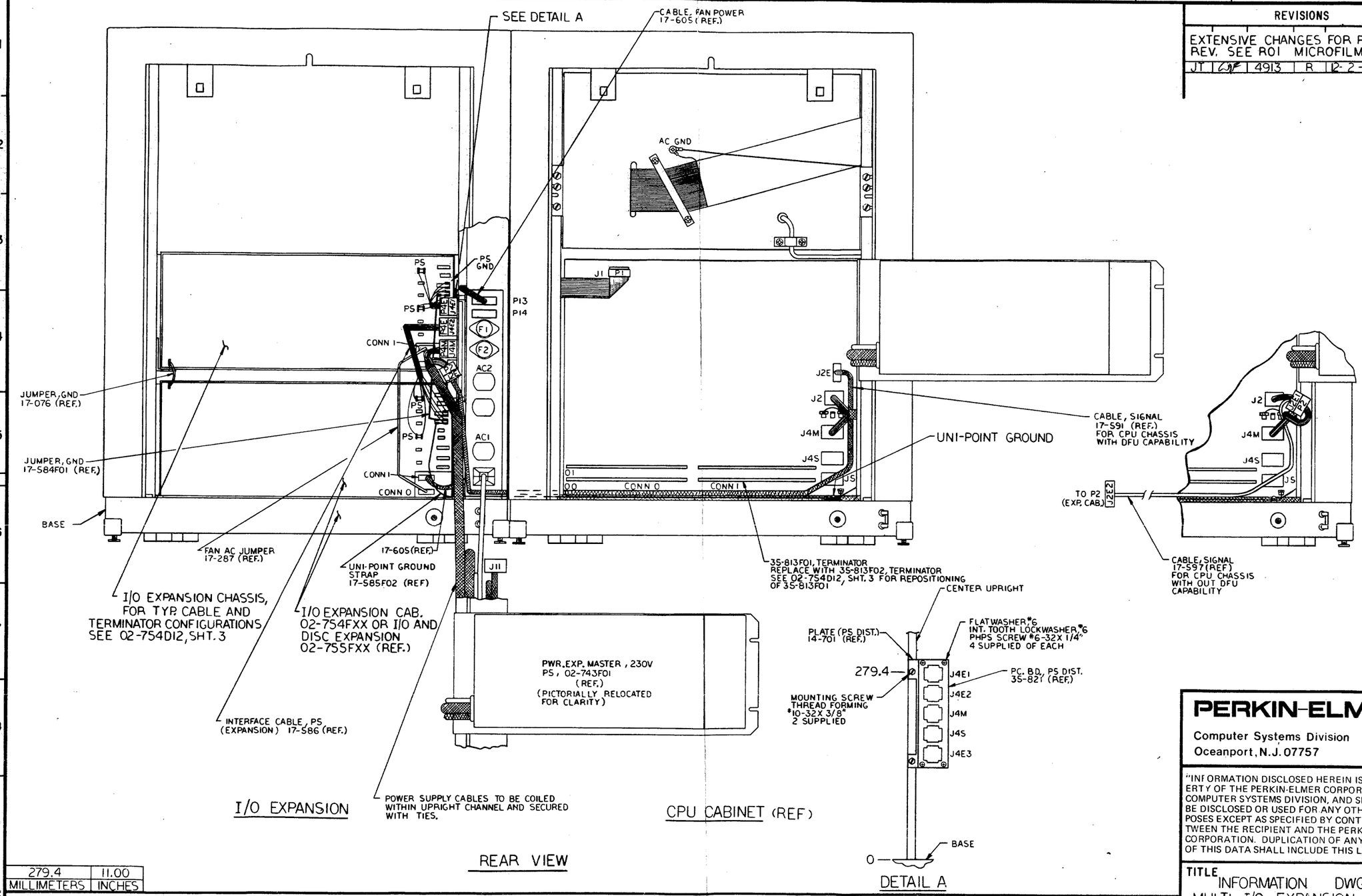
TITLE
INFORMATION DWG.
MULTI- I/O EXPANSION
MOD 3210 , 208V

TASK 03175 SHT 1-7

DWG 02-752 R04 D12

DRAWING 44-131-405/9

REVISIONS				
EXTENSIVE CHANGES FOR PREVIOUS REV. SEE R01 MICROFILM COPY.				
JT	CJF	4913	R	12-2-81 R02



279.4	11.00
MILLIMETERS	INCHES

NOTES

DRAFTER	
J TAMULEVICIUS	
DATE	
7-29-81	

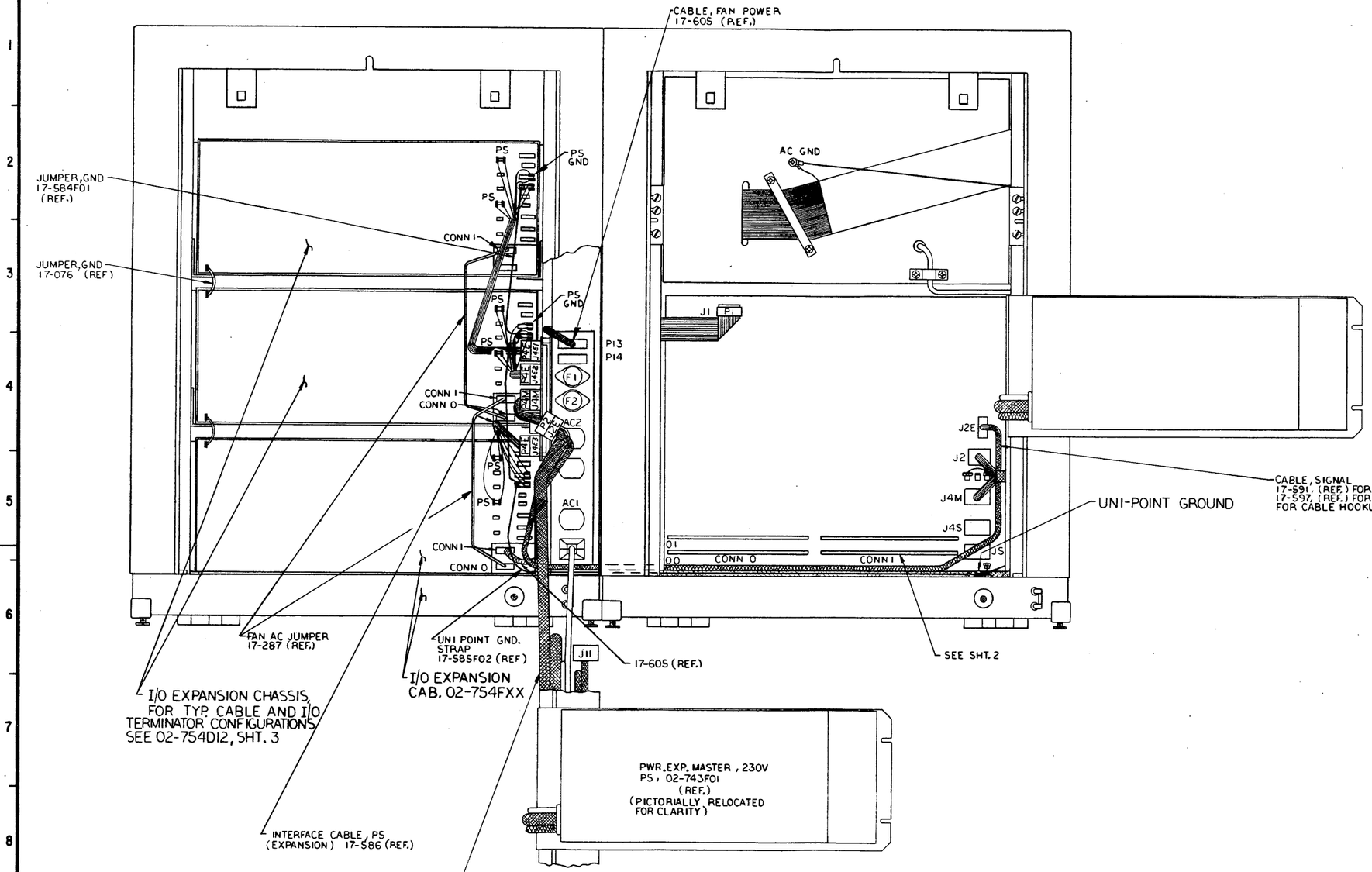
PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE
INFORMATION DWG.
MULTI-I/O EXPANSION
MOD 3210, 208V

TASK 03175	SHT
DWG 02-752 R02 D12	2-7

REVISIONS				
EXTENSIVE CHANGES FOR PREVIOUS REV. SEE R01 MICROFILM COPY.				
JT	DF	4913	R	12-2-81 R02



REAR VIEW

NOTES

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

DRAFTER	J TAMULEVICIUS
DATE	7-29-81

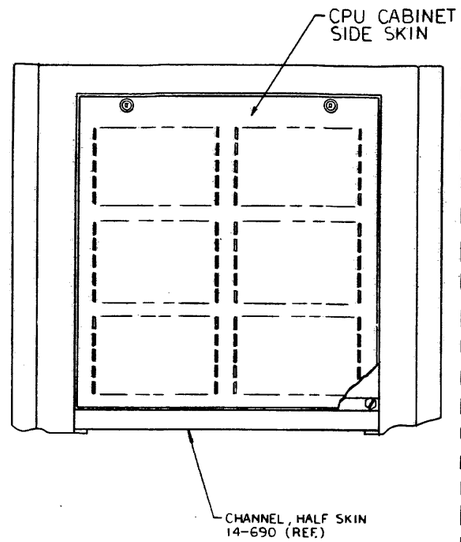
TITLE INFORMATION DWG.
MULTI-I/O EXPANSION
MOD 3210, 208V

TASK 03175 | SHT 3-7

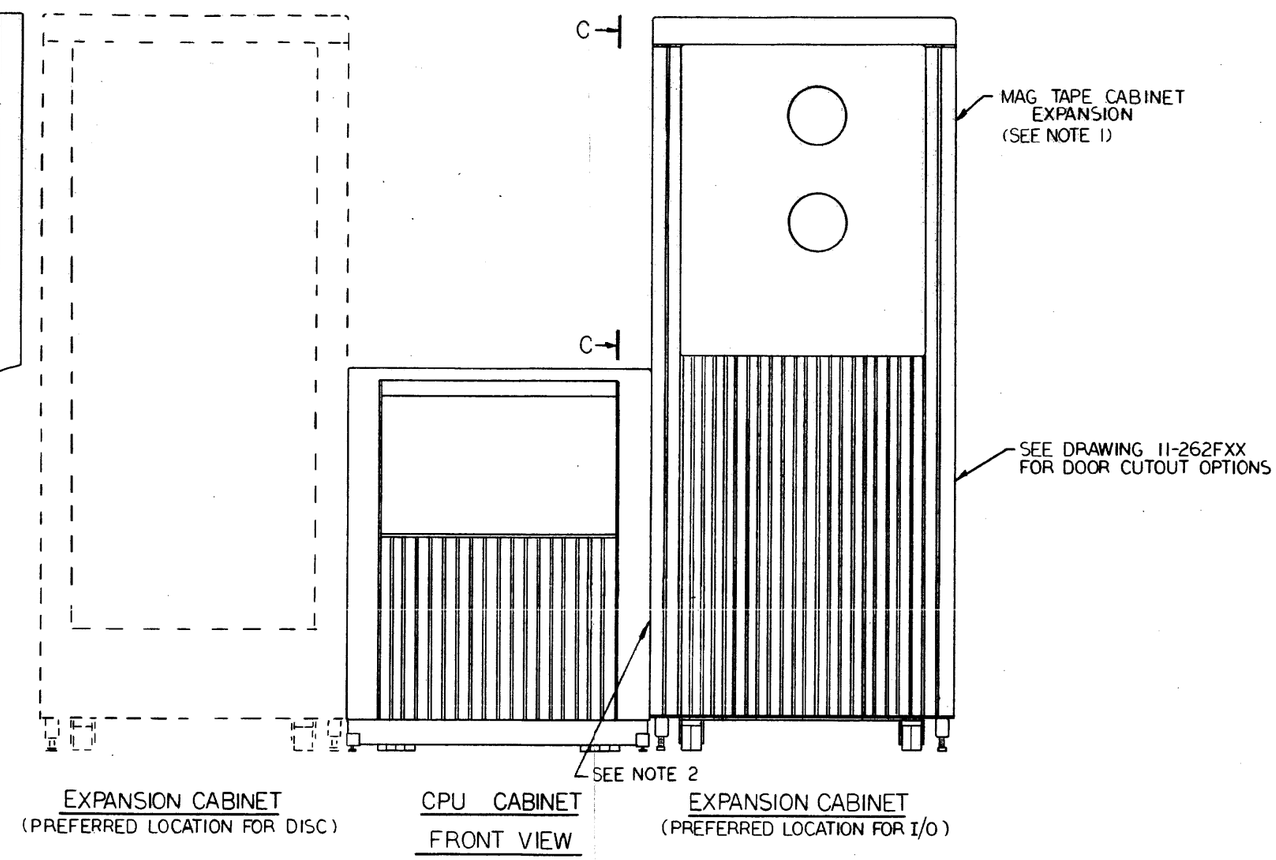
DWG 02-752 R02 D12

SRUNING 44-131 40592

REVISIONS					
EXTENSIVE CHANGES FOR PREVIOUS REV. SEE R00 MICROFILM COPY					
JT	V.J.P.	4868	R	10-15-81	R01
SHT. 4 OF 7 WAS 4 OF 6					
JT	CJF	4913	R	12-3-81	R02
ADDED NOTE 1.					
JAH	GJV	5122	R	10-5-82	R03
DELETED SECTION B-B & REF TO B-B, AREA H-G, ADDED "SEE NOTE2". ADDED NOTE 2.					
JAH	GJV	5001	R	10-27-82	R04



VIEW C-C
SEE NOTE 1



EXPANSION CABINET (PREFERRED LOCATION FOR DISC)

CPU CABINET FRONT VIEW

EXPANSION CABINET (PREFERRED LOCATION FOR I/O)

02-752F01 , 56" CABINET

NOTES 1. INVERT MAG TAPE MOUNTING RAILS ON BOTH SIDES WHEN INSTALLING A 75 I.P.S MAG TAPE AND HALF SKIN CHANNEL.

2. REMOVE APPROPRIATE SIDE SKINS. PLACE CPU CABINET SIDE SKIN PER VIEW C-C ON EXPANSION CABINET.

BRUNING 44-131 40579

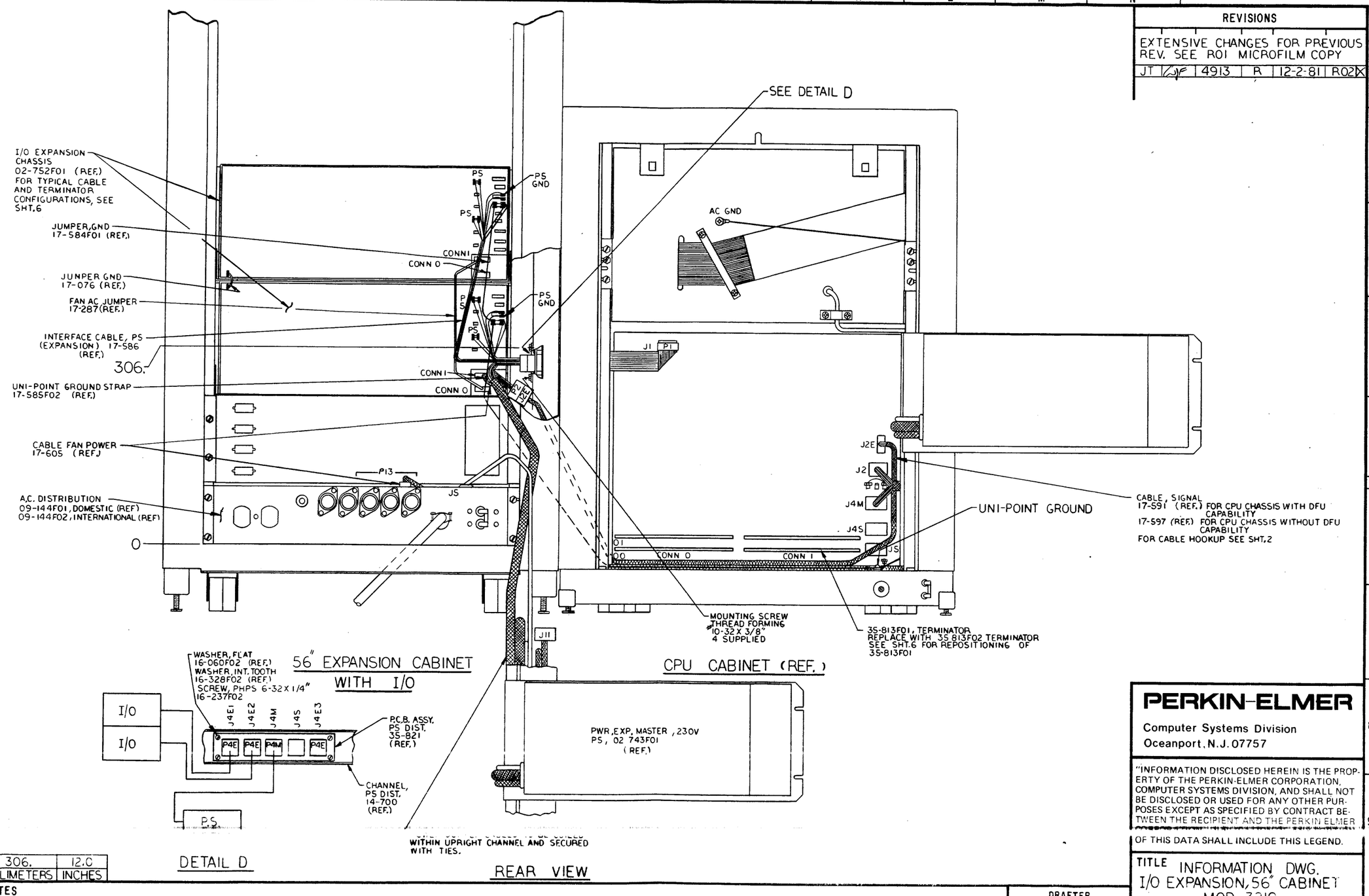
PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE INFORMATION DWG.
I/O EXPANSION, 56" CABINET
MOD 3210

TASK 03175 | SHT 4-7
DWG 02-752 R04 D12

REVISIONS
EXTENSIVE CHANGES FOR PREVIOUS REV. SEE R01 MICROFILM COPY
JT |6/F| 4913 | R | 12-2-81 | R02



306.	12.0
MILLIMETERS	INCHES

NOTES

DRAFTER	
J TAMULEVICIUS	
DATE	
8-25-81	

PERKIN-ELMER

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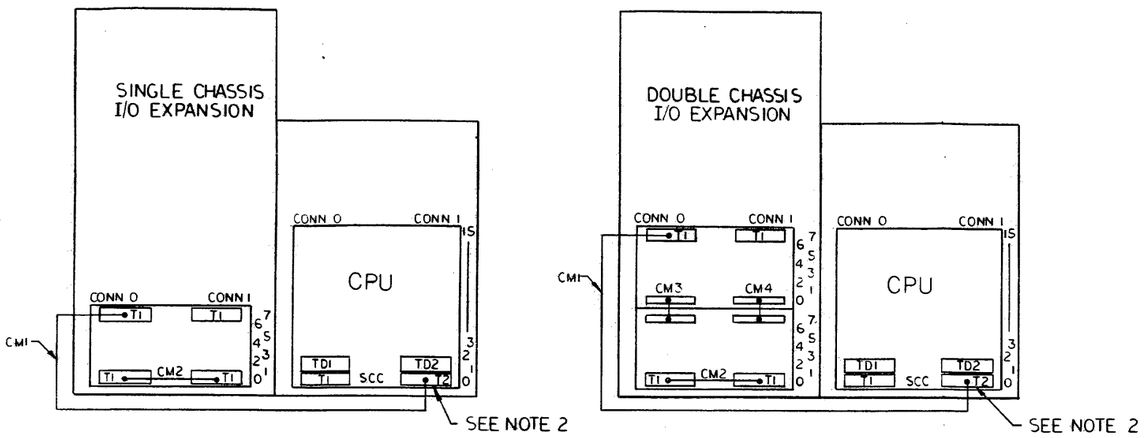
Oceanport, N.J. 07757

TITLE INFORMATION DWG. I/O EXPANSION, 56" CABINET MOD 3210

TASK	SHT
03175	5 - 7
DWG 02-752R02 D12	

REVISIONS					
AREAS D3, H3, D8, H8 & M8, CPU. CONN 1 T2 WAS T1. ADDED T2 TO AREA R4. ADDED NOTE 2 SHT. 6 OF 7 WAS 6 OF 6					
JT	[illegible]	4913	R	12-3-81	R01



TYPICAL I/O EXPANSION CABLE INTERFACE

TERMINATORS

TERMINATOR	PART NO. REF.
T1	35-813F01
T2	35-813F02
TD1	35-814F01
TD2	35-814F02

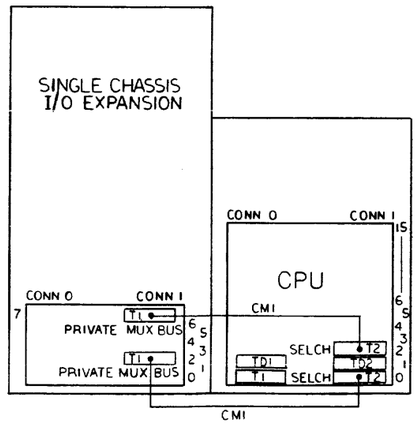
T = MUX BUS TERMINATOR
TD=DMA TERMINATOR

CABLES

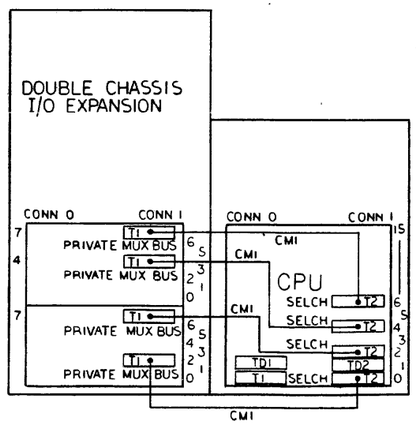
CABLE	PART NO. REF.
CM1	17-464F04
CM2	17-464F02
CM3	17-193M02
CM4	17-194M02

CM= CABLE (MUX)

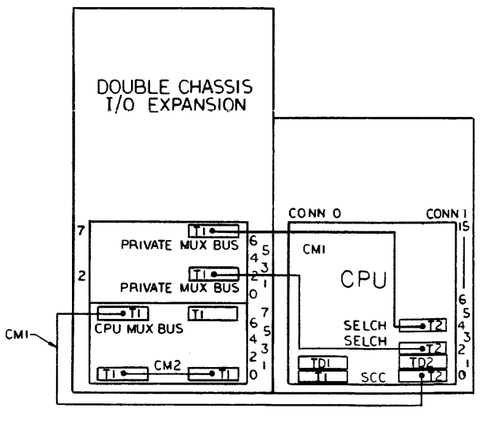
SCC=SUB CHANNEL CONTROLLER
SELCH = SELECTOR CHANNEL



TYPICAL
I/O EXPANSION WITH SELCH
PRIVATE MUX BUSSES



TYPICAL
I/O EXPANSION WITH SELCH
PRIVATE MUX BUSSES



TYPICAL
I/O EXPANSION WITH CPU MUX BUS AND SELCH
PRIVATE MUX BUSSES

REAR VIEWS

NOTES
1. REF. SELCHES IN CPU CABINET ARE SHOWN FOR CONFIGURATIONS WITHOUT DFU. UP TO 3 SELCHES ARE OFFERED FOR CONFIGURATIONS WITH DFU.
2. T2 NOTED REPLACES T1 SUPPLIED WITH CPU CHASSIS. T1 IS RELOCATED IN I/O CHASSIS.

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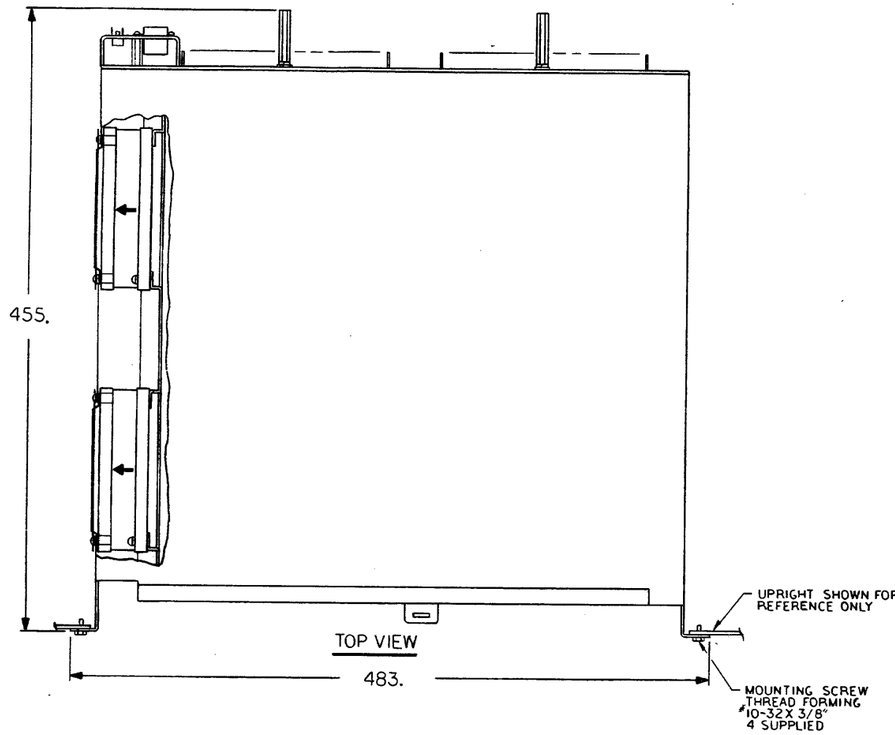
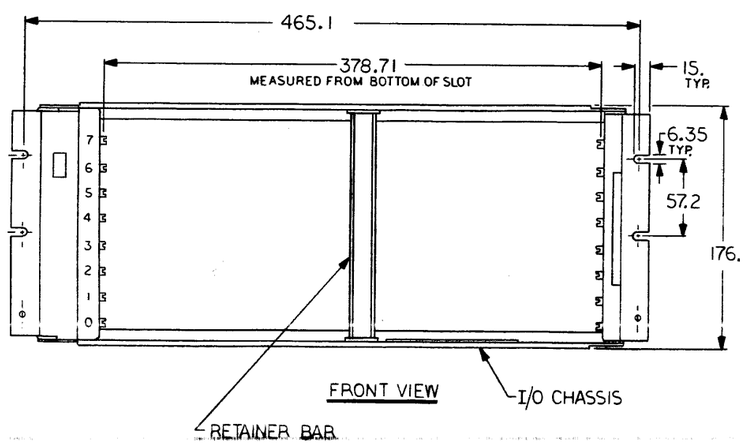
Oceanport, N.J. 07757

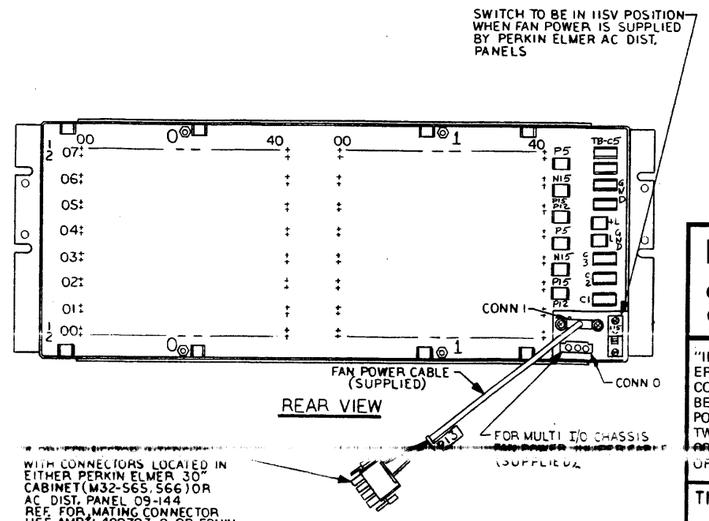
DRAFTER	J TAMULEVICIUS
DATE	8-21-81

TITLE INFORMATION DWG.
I/O EXPANSION, 56" CABINET
MOD 3210

TASK	03175	SHT
DWG	02-752 R01 D12	6-7







6.35	250
15.	.6
57.2	2.25
176.	6.9
378.71	14.910
455.	17.9
465.1	18.31
483.	19.0
MILLIMETERS	INCHES

REVISIONS

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE
INFORMATION DWG.
I/O CHASSIS

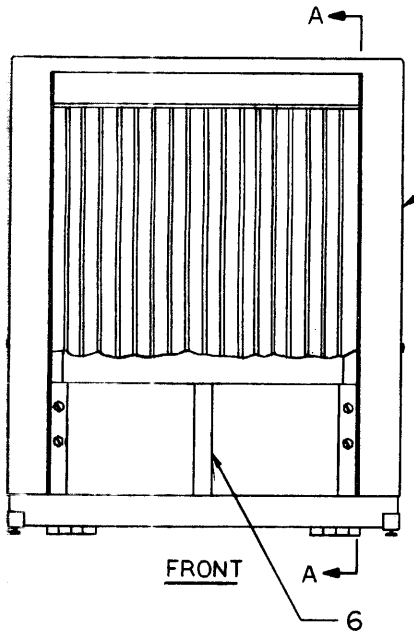
NOTES

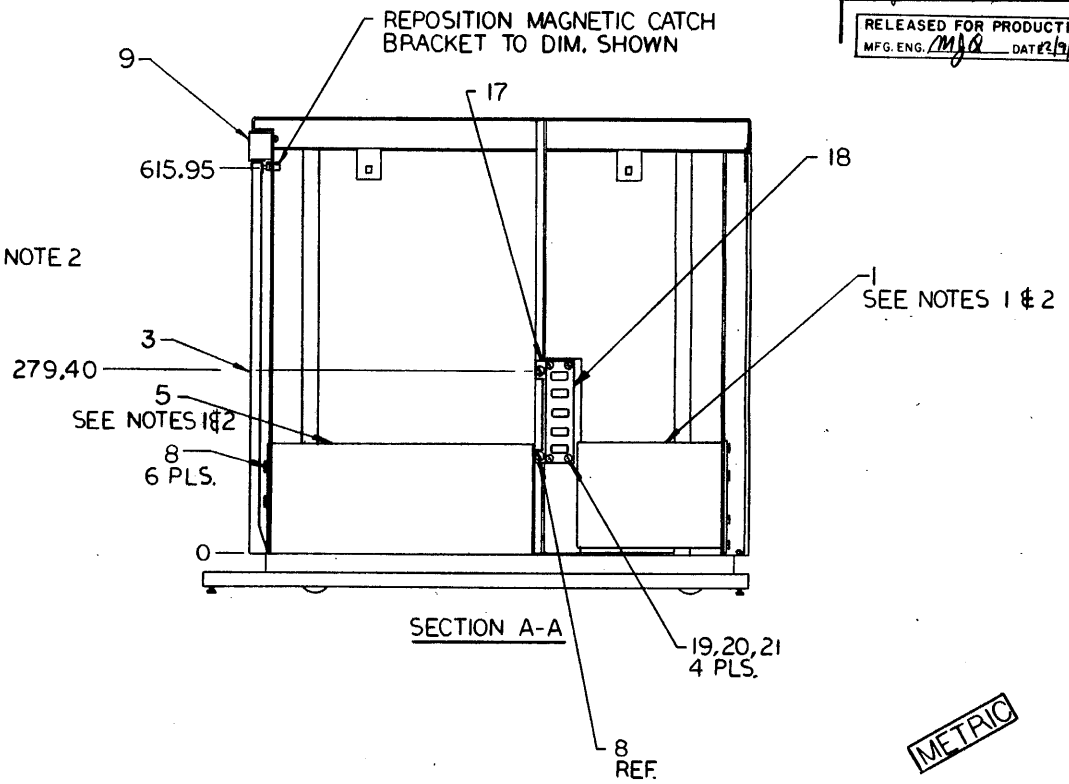
DRAFTER	J TAMULEVICIUS
DATE	10-23-81
TASK	03131
DWG	02-752 D12
SHT	7-7

MILLIMETERS	INCHES
615.95	24.25
279.40	11.00

REVISIONS					
PRE PRODUCTION APPROVAL	INIT	DATE			
	DEV	8.28.81			
	PROD	8/27/81			
AREA D4, RMVD. ITEM 13,4 PLS, AREA J4, RMVD. ITEM 4 CHANGED ITEM 2 PICTORIALLY AREA E4, ADDED DIM. 279.40					
JT		4868	R	10-15-81	R01
ADDED ITEMS 23-26 TO NOTE 2					
JT		4913	R	12-3-81	R02

RELEASED FOR PRODUCTION
MFG. ENG. MJ DATE 12/9





METRIC

USED IN MANUAL: 47-022

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

PART NO	DESCRIPTION
02-754 F02	INTERNATIONAL, 208V
02-754 F01	DOMESTIC, 208V

VARIATION TABLE

NOTES
1. FOR TERMINATION OF CABLES SEE 02-754 D12
2. ITEMS 10-12,14-16,22-26 TO BE INSTALLED PER 02-754D12

UNLESS OTHERWISE SPECIFIED			
SCALE: 3/16	MILLIMETERS	INCHES	
DIMENSIONS ARE IN MILLIMETERS	.XX ± .13 .X ± .5 X, ± .8	.XXX ± .005 .XX ± .02 .X ± .03	
NAME		TITLE	DATE
J TAMUL		DES / DFT	6-5-81
R CERO		SUPV	12-8-81
		CHK	
R DENGEL		ENG	12-8-81
P ABITANTE		MGR	12-8-81
R BARKER		QC	12-7-81

TITLE: ASSEMBLY MOD 3210 I/O EXPANSION CABINET

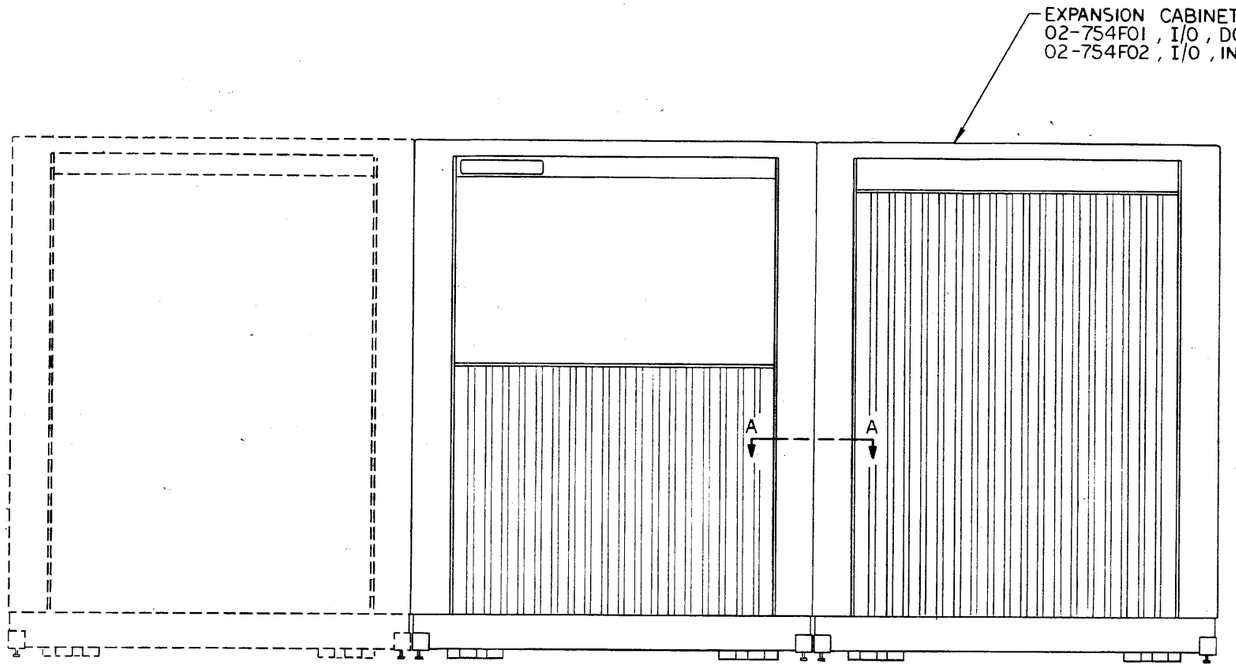
TASK 03175 | SHT 1 - 1

DWG 02-754R02 C03

BRUNING 44-131 40579

REVISIONS					
PRE PRODUCTION APPROVAL	INIT	DATE			
	DEV	8-28-81			
	PROD	8/28/81			
EXTENSIVE CHANGES FOR PREVIOUS REV. SEE R00 MICROFILM COPY. REVISED SHT. 2					
JT	DJP	4868	R	10-15-81	R01
REVISED SHT'S, 2&3					
JT	CMF	4913	R	12-3-81	R02 X

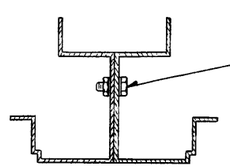
RELEASED FOR PRODUCTION
MFG. ENG. MJG DATE 12/9/81



DISC EXPANSION CABINET

CPU CABINET (FRONT VIEW)

PREFERRED LOCATION FOR I/O EXPANSION CABINET



WHEN BOLTING CABINETS TOGETHER;
REMOVE APPROPRIATE HOLE PLUGS AND SIDE SKINS.
BOLT TOGETHER WITH:
1 EA, 5/16-18 X 3/4" HEX HEAD BOLT, 16-410F01
2 EA, 5/16 EXTERNAL TOOTH LOCKWASHER, 16-380F05
1 EA, 5/16-18 HEX NUT, 16-058F05

SECTION A-A

USED IN MANUAL: 47-022

UNLESS OTHERWISE SPECIFIED	
SCALE: 1/4	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
	J TAMUL	DES/DFT	6-8-81
R CERO		SUPV	12-8-81
		CHK	
R DENGEL		ENG	12-8-81
P ABITANTE		MGR	12-8-81
R BARKER		QC	12-7-81

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

3	2	SHEET NO.
01	02	REV. LEVEL
D	D	SHEET SIZE

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

NOTES

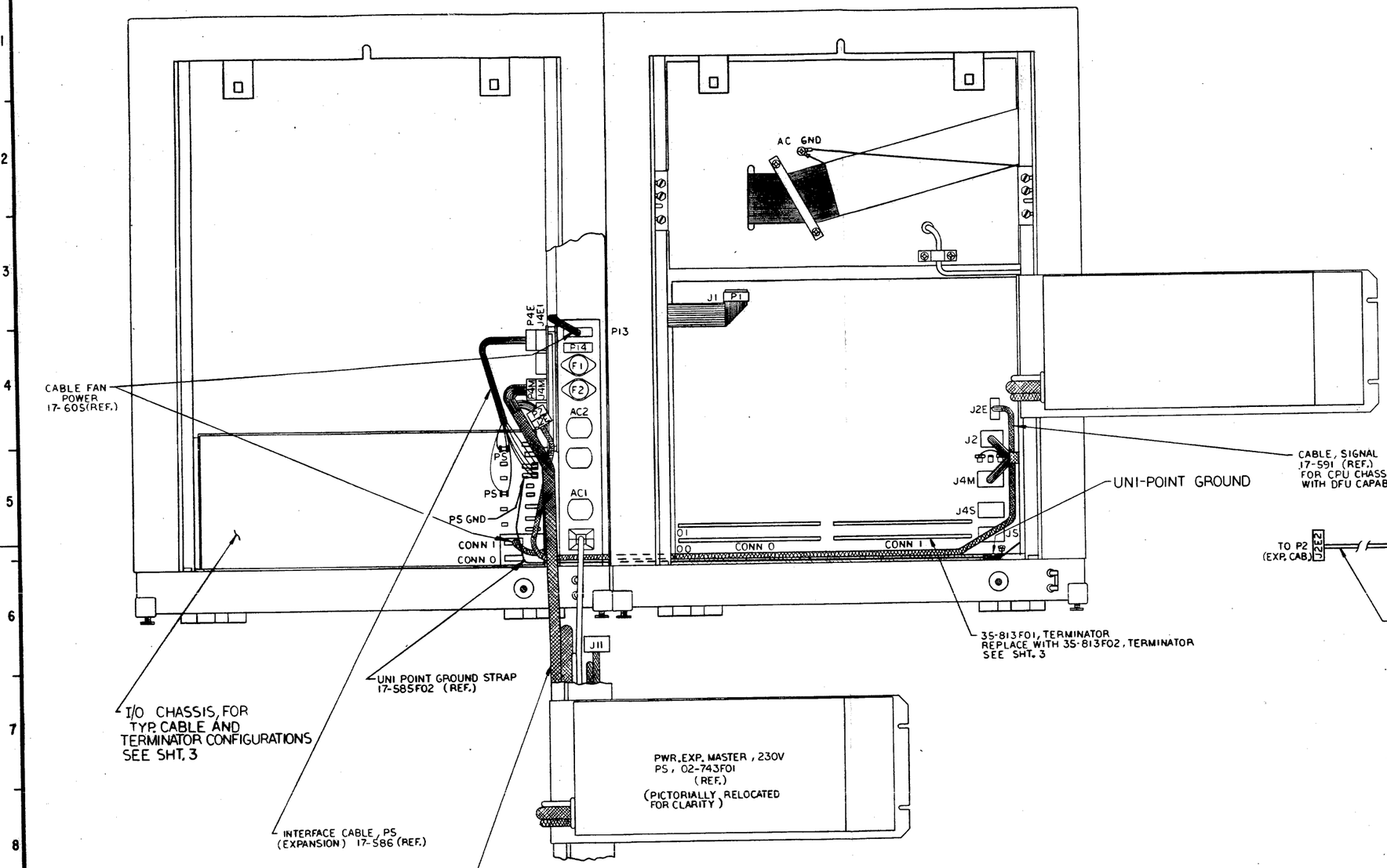
TITLE: INFORMATION DWG. I/O EXPANSION CABINET MOD 3210 , 208V

TASK 03175 SHT 1-3

DWG 02-754R02 D12

BRUNING 44 151 405 79

REVISIONS					
EXTENSIVE CHANGES FOR PREVIOUS REV. SEE R01 MICROFILM COPY.					
JT	GJF	4913	R	12-3-81	R02 X



REAR VIEW

NOTES

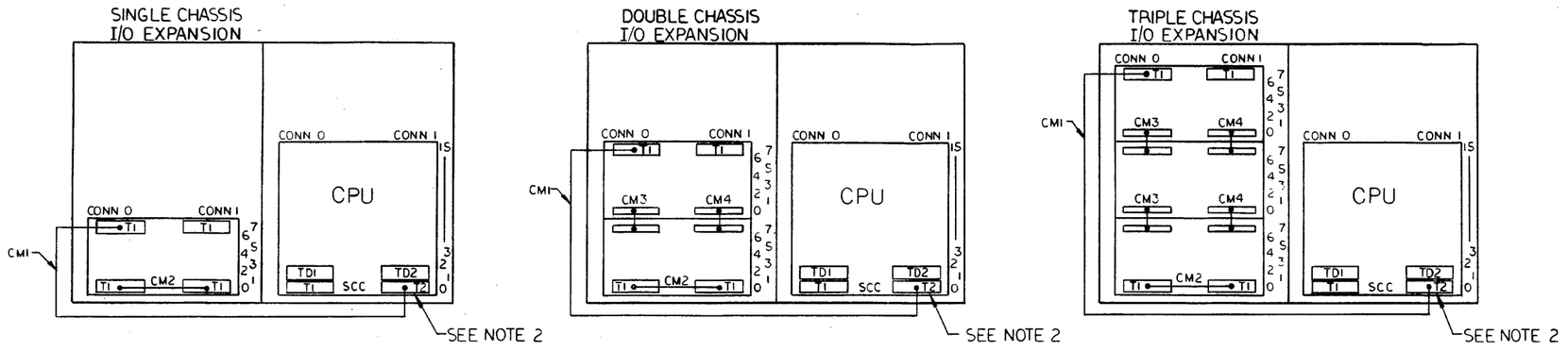
DRAFTER	J TAMULEVICIUS
DATE	5-13-81

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE	INFORMATION DWG. I/O EXPANSION CABINET MOD 3210, 208V	
TASK	03175	SHT 2-3
DWG	02-754R02 D12	

REVISIONS					
AREAS D3, H3, M3, D8, H8 & M8, CPU CONN 1, T2 WAS T1. ADDED T2 TO AREA R4. ADDED NOTE 2					
JT	GJF	4913	R	12-3-81	R01



TYPICAL I/O EXPANSION CABLE INTERFACE

TERMINATORS

TERMINATOR	PART NO. REF.
T1	35-813F01
T2	35-813F02
TD1	35-814F01
TD2	35-814F02

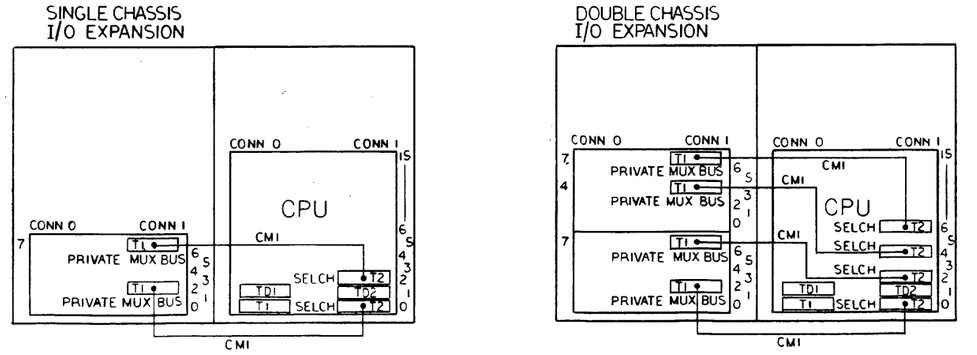
T = MUX BUS TERMINATOR
TD = DMA TERMINATOR

CABLES

CABLE	PART NO. REF.
CM1	17-464F04
CM2	17-464F02
CM3	17-193M02
CM4	17-194M02

CM = CABLE (MUX)

SCC = SUB CHANNEL CONTROLLER
SELCH = SELECTOR CHANNEL



TYPICAL
I/O EXPANSION WITH SELCH
PRIVATE MUX BUSSES

TYPICAL
I/O EXPANSION WITH SELCH
PRIVATE MUX BUSSES

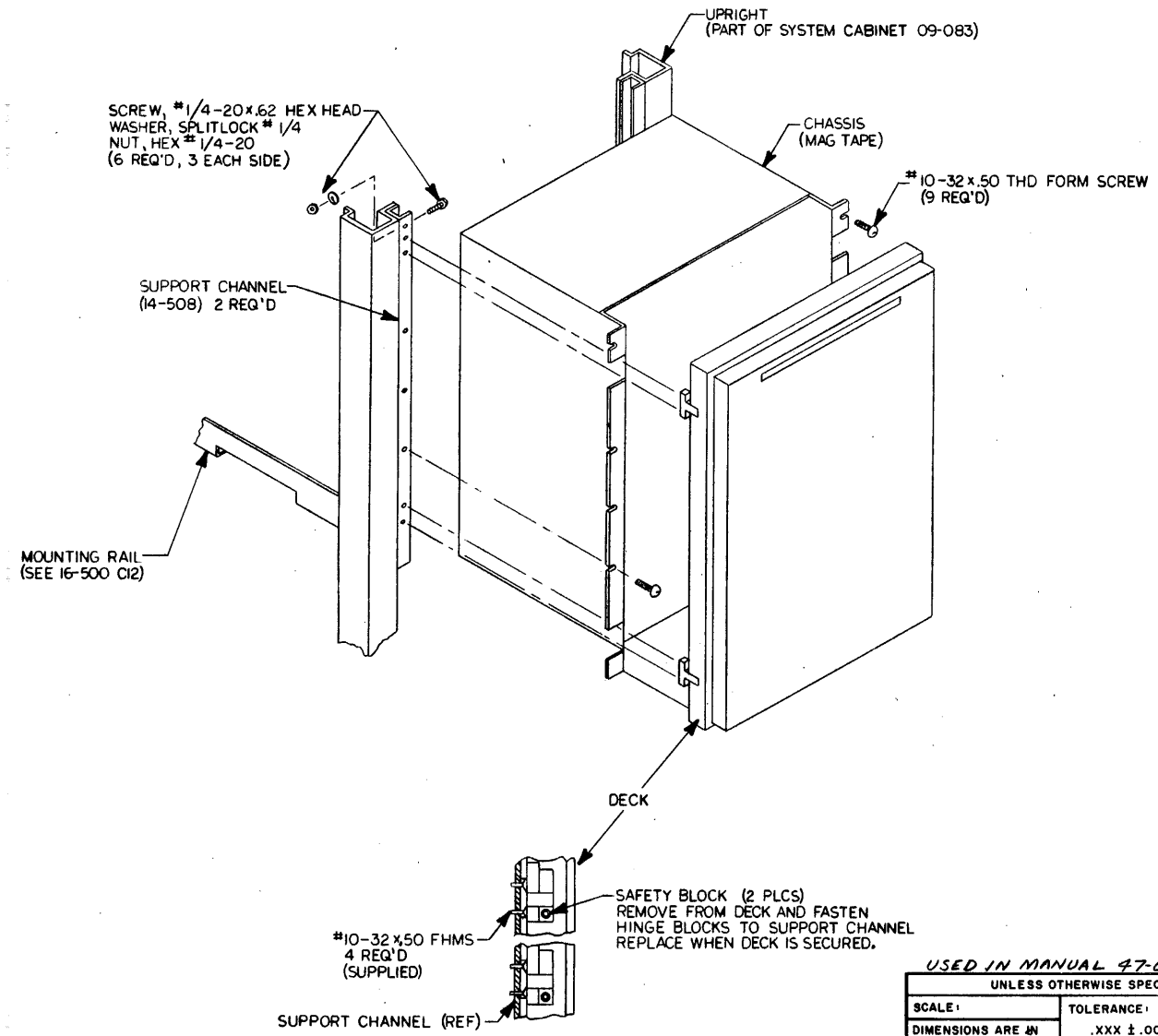
TYPICAL
I/O EXPANSION WITH CPU MUX BUS AND SELCH
PRIVATE MUX BUSSES

REAR VIEWS

NOTES
1. REF., SELCHES IN CPU CABINET ARE SHOWN FOR CONFIGURATIONS WITHOUT DFU. UP TO 3 SELCHES ARE OFFERED FOR CONFIGURATIONS WITH DFU.
2. T2 NOTED REPLACES T1 SUPPLIED WITH CPU CHASSIS. T1 IS RELOCATED IN I/O CHASSIS.

DRAFTER	J TAMULEVICIUS
DATE	8-21-81
TITLE	INFORMATION DWG. I/O EXPANSION CAB. MOD 3210 208V
TASK	03175
DWG	02-754 R01 D12
SHT	3-3

REVISIONS					
EXTENSIVE CHANGES TO SHT 1, COMPLETELY RE-DRAWN. SEE VOIDED R00 IN FILE					
KR	GJ	4888	MS	10-22-81	R01



USED IN MANUAL 47-022

SHEET NO.	2
REV LEVEL	00
SHEET SIZE	C

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.003 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	K. REED	DES / DFT	10-19-81
G. MILLER		SUPV	
J. VIGILANTE		CHK	
D FOGGIA		ENG	
P ABITANTE		MGR	
R BARKER		QC	

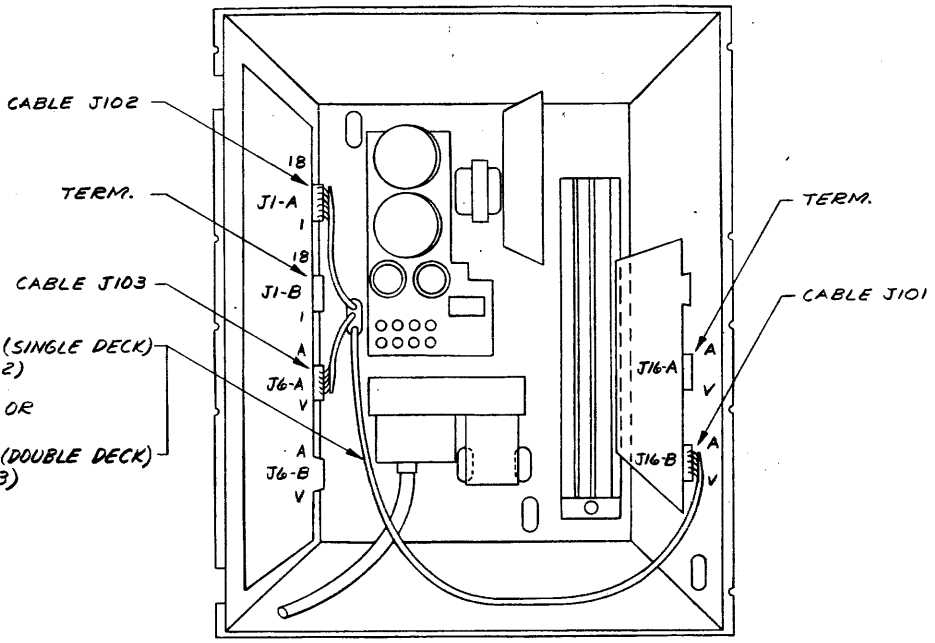
PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE
INFORMATION DRAWING
WANGCO, 1175, 800 BPI
MAG TAPE SYSTEM

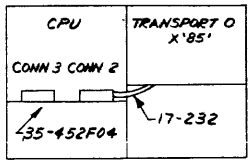
TASK	03175	SHT
DWG	02-766 R01 C12	1 - 2

PERKIN ELMER

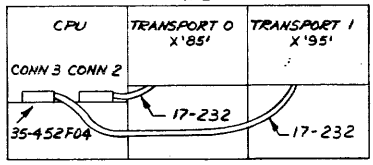
REVISIONS



1 X 1



1 X 2



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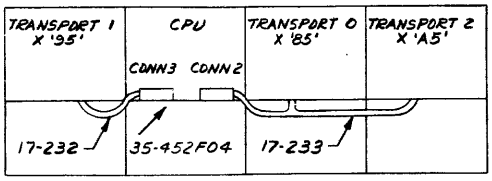
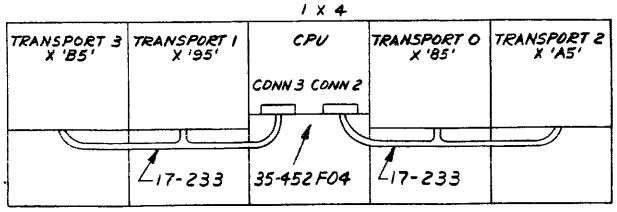


1 X 4



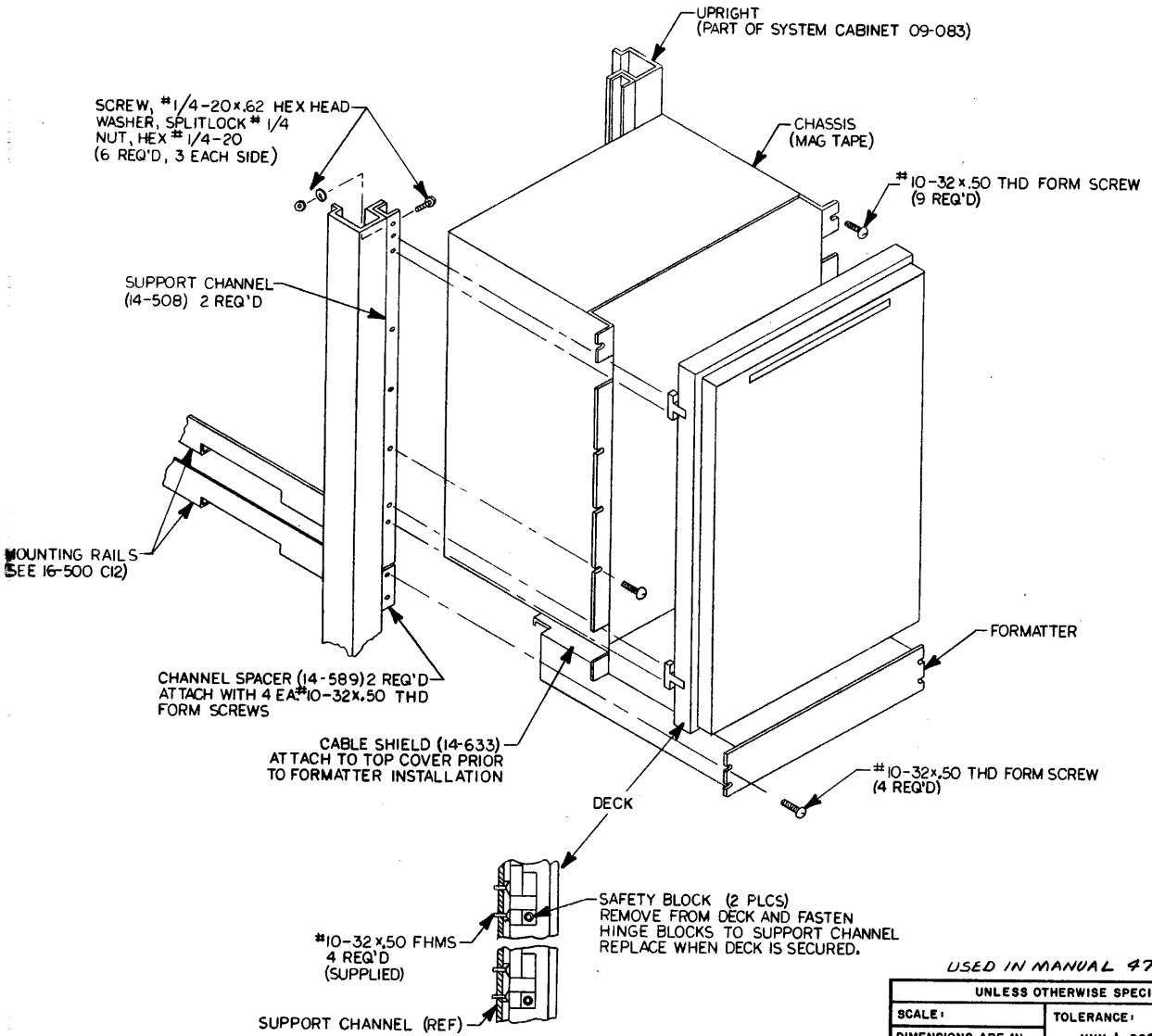
SCALE- ∞	NAME	TITLE	DATE
TOLERANCE: .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	J. TAMUL	DRAFT	
		CHK	
		ENGR	

TITLE
INFORMATION
WANGCO 1175 800 BPI
MAG TAPE SYSTEM

TASK NO. 03175 SHEET OF 2 — 2
DWG. NO. 02-766 C12

OGILVIE PRESS

REVISIONS					
EXTENSIVE CHANGES TO SHT 1, COMPLETELY RE-DRAWN. SEE VOIDED ROO IN FILE					
KP	AV	4888	MS	10-22-81	201



USED IN MANUAL 47-022

SHEET NO.	2
REV LEVEL	00
SHEET SIZE	C

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE: .XXX ± .005 .X ± .03 .XX ± .02 ANGLES ± 1°		
DIMENSIONS ARE IN INCHES			
NAME		TITLE	DATE
K. REED		DES / DFT	10-19-81
G. MILLER		SUPV	
J. VIGILANTE		CHK	
D FOGGIA		ENG	
P ABITANTE		MGR	
R BARKER		QC	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE
INFORMATION DRAWING
WANGCO DUAL DENSITY
MAG TAPE SYSTEM

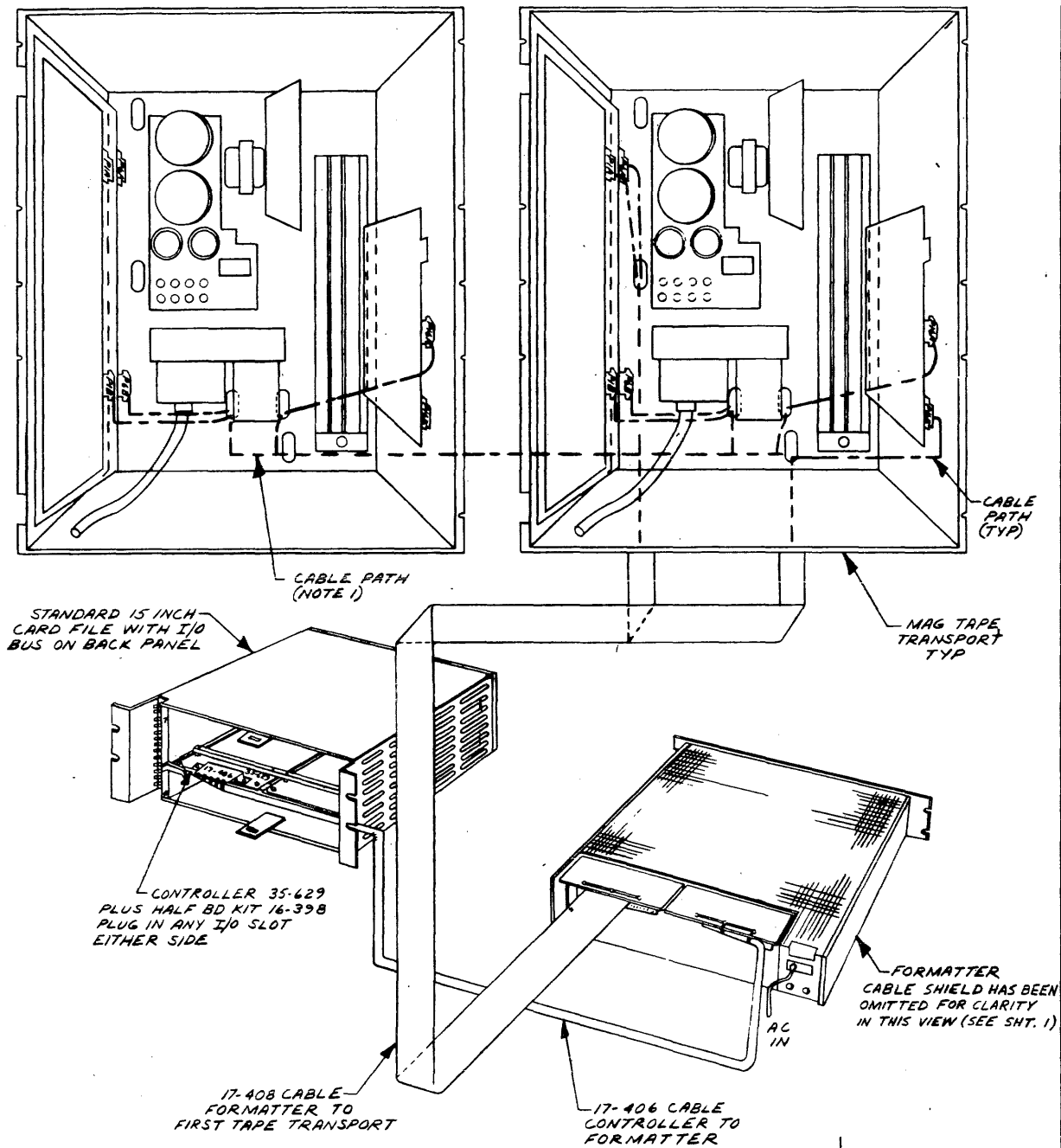
TASK 03982 (ECN 4889)	SHT
DWG 02-764 R01 C12	1 - 2

PERKIN-ELMER

REVISIONS

NOTES

1. INTRA TRANSPORT CABLE CONNECTIONS
   P1B TO P1B
   P6B TO P6B
   P16A TO P16A



CONTROL CABLING

SCALE –

NAME	TITLE	DATE
J.TAMUL	DRAFT	
	CHK	
	ENGR	

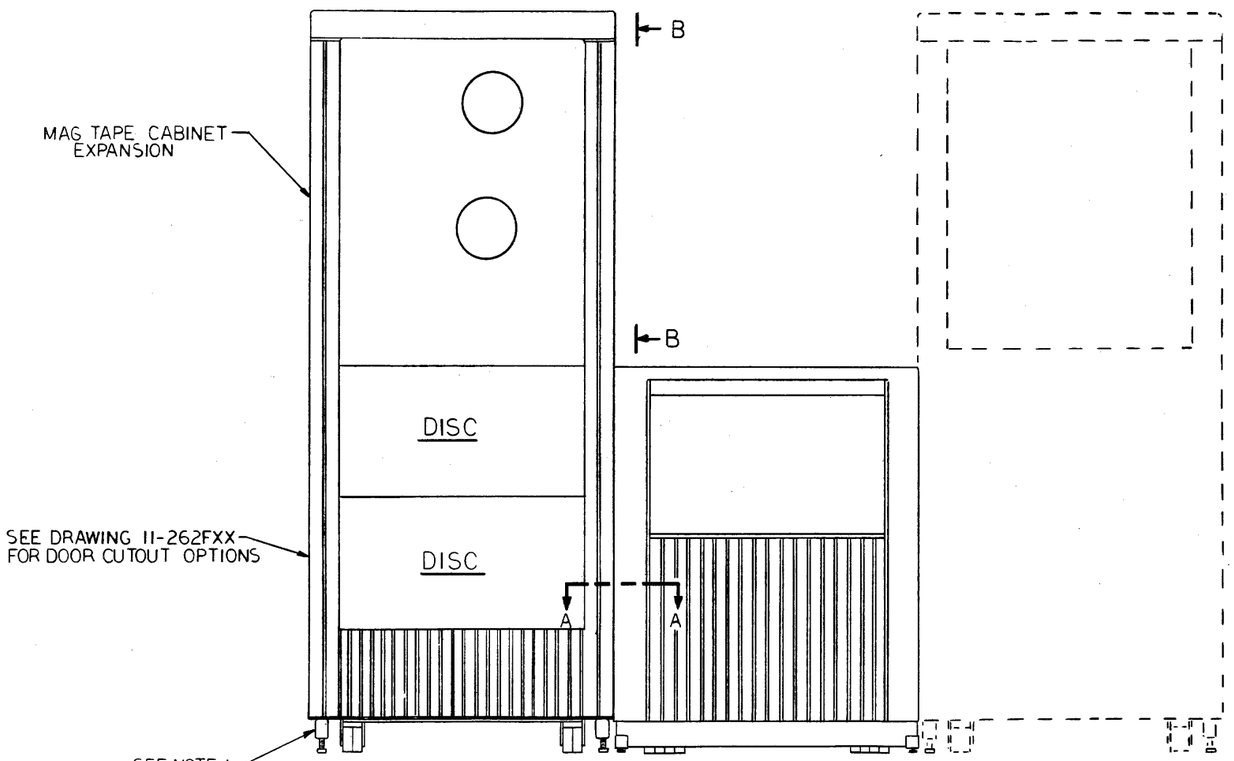
TITLE INFORMATION WANGCO DUAL DENSITY MAG TAPE SYSTEM

DWG. NO. 03175

DWG. NO. 02-764 C/E

SHEET 2 OF 2

REVISIONS					
PRE PRODUCTION APPROVAL	INIT	DATE			
	DEV	8-28-81			
	PROD	MJQ 8/28/81			
EXTENSIVE CHANGES FOR PREVIOUS REV. SEE R00 MICROFILM COPY, REVISED SHT. 2					
JT	W.P.	4868	R	10-15-81	R01
RELEASED FOR PRODUCTION MFG. ENG. MJQ DATE 12/9/81					
REVISED SHT 2.					
KR		5050	R	5-17-82	R02

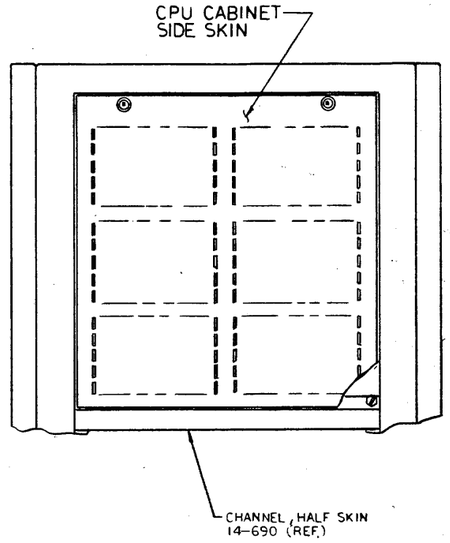


EXPANSION CABINET (PREFERRED LOCATION FOR DISC)

CPU CABINET

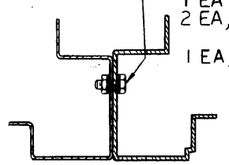
FRONT VIEW

EXPANSION CABINET (PREFERRED LOCATION FOR I/O)



VIEW B-B

WHEN BOLTING CABINETS TOGETHER; REMOVE APPROPRIATE HOLE PLUGS AND SIDE SKINS. PLACE CPU CABINET SIDE SKIN PER VIEW B-B ON EXPANSION CABINET. BOLT TOGETHER WITH:
1 EA, 5/16-18 X 3/4 HEX HD. BOLT, 16-410F01
2 EA, 5/16 EXTERNAL TOOTH LOCKWASHER, 16-380F05
1 EA, 5/16-18 HEX NUT, 16-058F05



SECTION A-A

USED IN MANUAL 47-022

UNLESS OTHERWISE SPECIFIED		
SCALE: 3/16	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME	TITLE	DATE
J.TAMUL	DES/DFT	8-10-81
R.CERO	SUPV	12-8-81
	CHK	
R.DENGEL	ENG	12-8-81
P. ABITANTE	MGR	12-8-81
R.BARKER	QC	12-4-81

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

NOTES
1. STABILIZER LEGS ARE REQUIRED FOR ALL DISC EXPANSION 56" CABINETS. SEE INSTALLATION DRAWING 16-832

REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

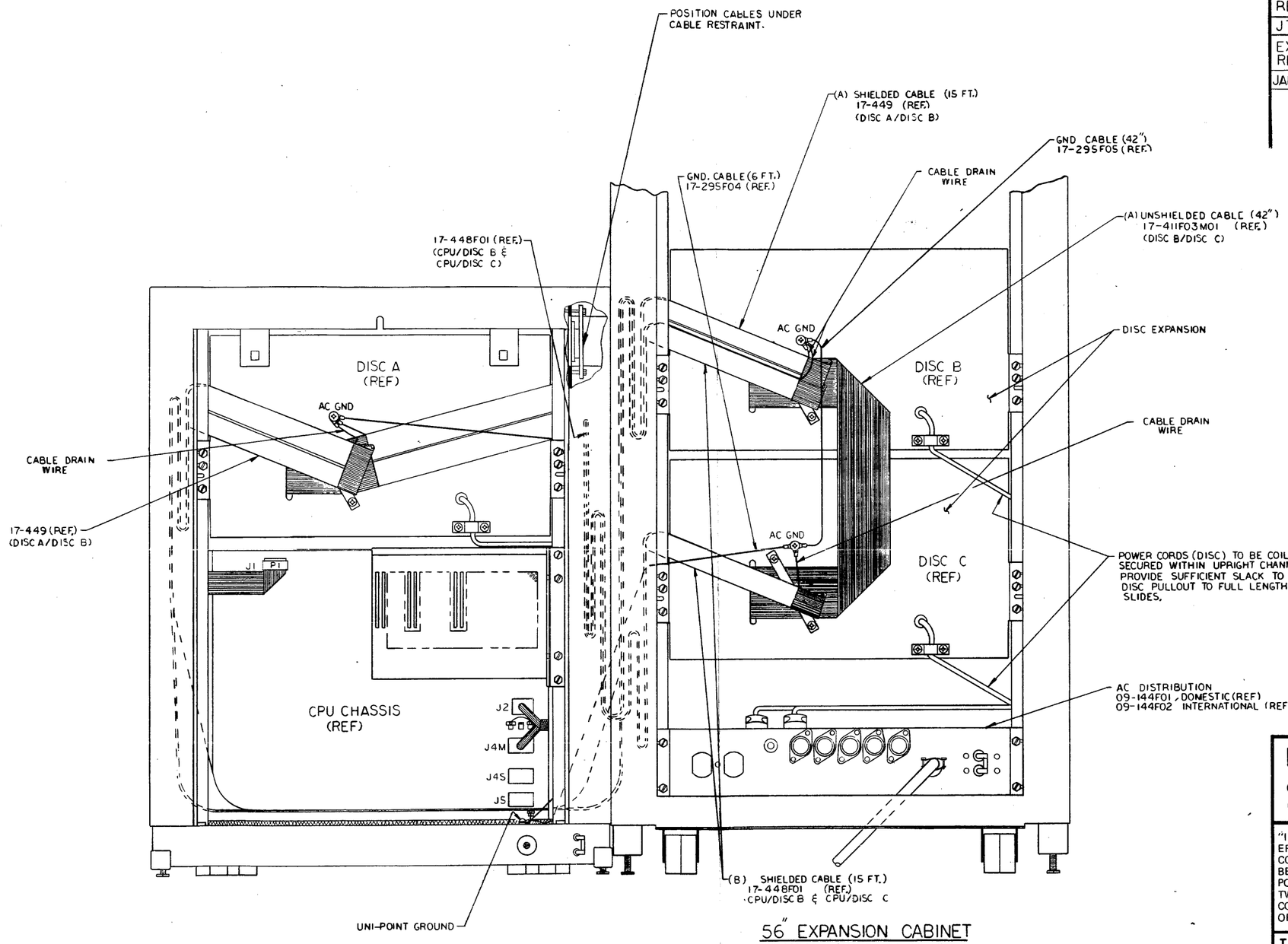
2	SHEET NO.
02	REV LEVEL
D	SHEET SIZE

TITLE INFORMATION DWG.
DISC EXPANSION, 56" CABINET
MOD 3210

TASK 03175	SHT
DWG 02-761R02 D12	1-2

BRUNING 44-131 40979

REVISIONS					
EXTENSIVE CHANGES FOR PREVIOUS REV SEE R00 MICROFILM COPY.					
JT	U.J.P.	4868	R	10-15-81	R01
EXTENSIVE CHANGES FOR PREVIOUS REV SEE R01 MICROFILM COPY.					
JAI		5050	F	4 12 82	R02



CPU CABINET (REF.) REAR VIEW

56" EXPANSION CABINET WITH DOUBLE DISC

NOTES

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Computer Systems Division
Oceanport, N.J. 07757

TITLE
INFORMATION DWG.
56" CABINET EXP.

DRAFTER	
J. TAMULEVICIUS	
DATE	
6-29-81	

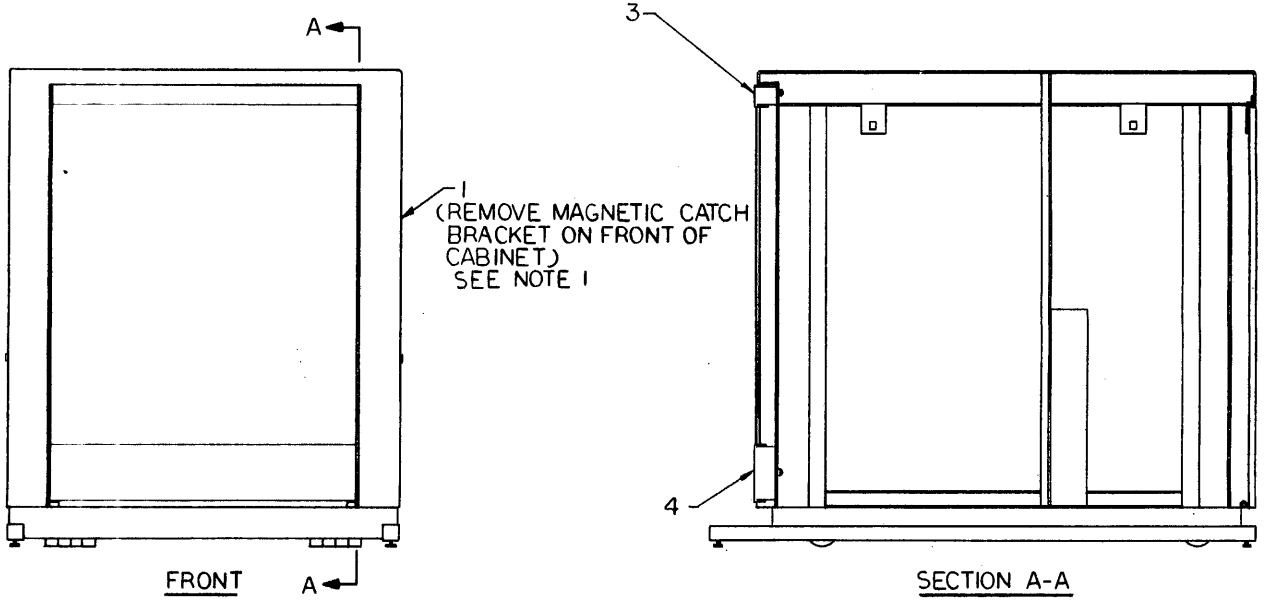
TASK 03175	SHT
DWG 02-761R02 D12	2-2

REVISIONS			
PRE PRODUCTION APPROVAL		UNIT	DATE
	DEV		8-28-81
	PROD	MJQ	8/28/81

AREA D4, RMVD. ITEM 7, 4 PLS.
AREA J2, RMVD. ITEM 2
CHANGED ITEM 1 PICTORIALLY

JT	USP	9868	R	10-15-81	ROT

RELEASED FOR PRODUCTION
MFG. ENG. MJQ DATE 12/9/81



USED IN MANUAL 47-022

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

PART NO	DESCRIPTION
02-756 F02	INTERNATIONAL, 208V
02-756 F01	DOMESTIC, 208V

VARIATION TABLE

NOTES
1. ITEMS 3—10 TO BE INSTALLED PER 02-756 D12, SHEET 2

UNLESS OTHERWISE SPECIFIED			
SCALE: 3/16	TOLERANCE: .XXX ± .005 .X ± .03 .XX ± .02 ANGLES ± 1°		
DIMENSIONS ARE IN INCHES			
NAME		TITLE	DATE
J TAMUL		DES / DFT	6-5-81
R CERO		SUPV	12-8-81
		CHK	
R DENGEL		ENG	12-8-81
P ABITANTE		MGR	12-8-81
R BARKER		QC	12-4-81

TITLE ASSEMBLY
MOD 3210 DOUBLE DISC EXPANSION CABINET

TASK 03175 SHT 1 - 1
DWG 02-756R01 C03

REVISIONS		
PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	8-28-81
	PROD MJQ	8/28/81

EXTENSIVE CHANGES FOR PREVIOUS REV. SEE R00 MICROFILM COPY. REVISED SHEET 2

JT	UHP.	4868	R	10-15-81	R01

RELEASED FOR PRODUCTION

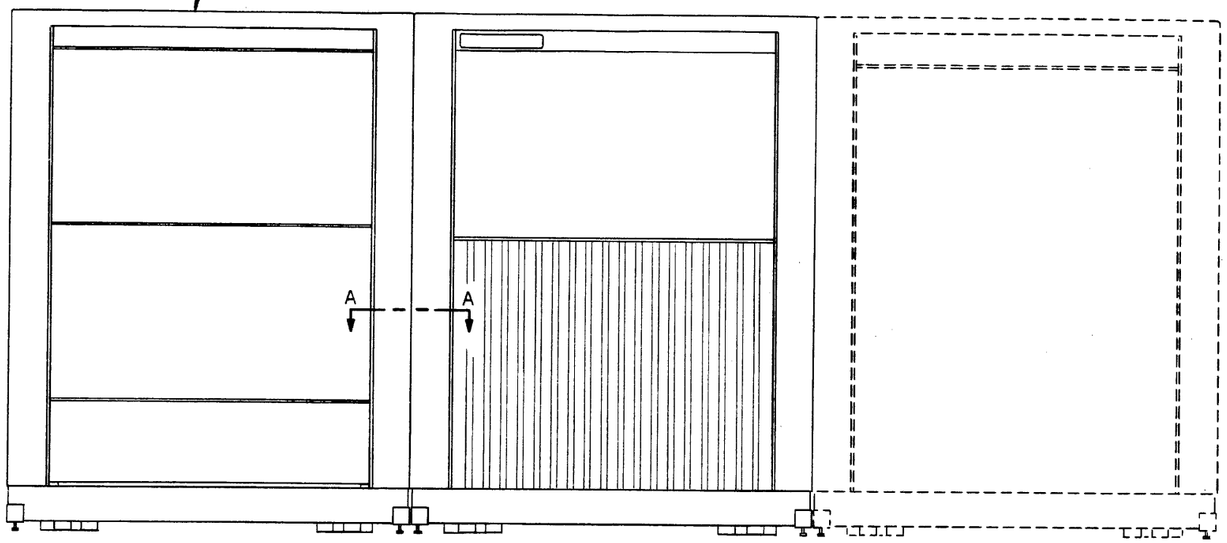
MFG. ENG. MJQ DATE 12/1/81

REVISED SHT 2.

KR	JT	5050	R	5-17-82	R02 X

USED IN MANUAL 47-022

EXPANSION CABINET
02-756F01, DOUBLE DISC, DOMESTIC
02-756F02, DOUBLE DISC, INTERNATIONAL

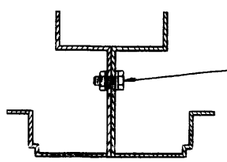


PREFERRED LOCATION FOR DOUBLE DISC EXPANSION CABINET

CPU CABINET

I/O EXPANSION CABINET

FRONT VIEW



WHEN BOLTING CABINETS TOGETHER;
REMOVE APPROPRIATE HOLE PLUGS AND SIDE SKINS.
BOLT TOGETHER WITH:
1 EA. 5/16-18 X 3/4 HEX HEAD BOLT, 16-410F01
2 EA. 5/16 EXTERNAL TOOTH LOCKWASHER, 16-380F05
1 EA. 5/16-18 HEX NUT, 16-058F05

SECTION A-A

UNLESS OTHERWISE SPECIFIED	
SCALE: 1/4	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
	J TAMUL	DES/DFT	6-8-81
R CERO		SUPV	12-8-81
		CHK	
R DENGEL		ENG	12-8-81
P ABITANTE		MGR	12-8-81
R BARKER		QC	12-4-81

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Oceanport, N.J. 07757

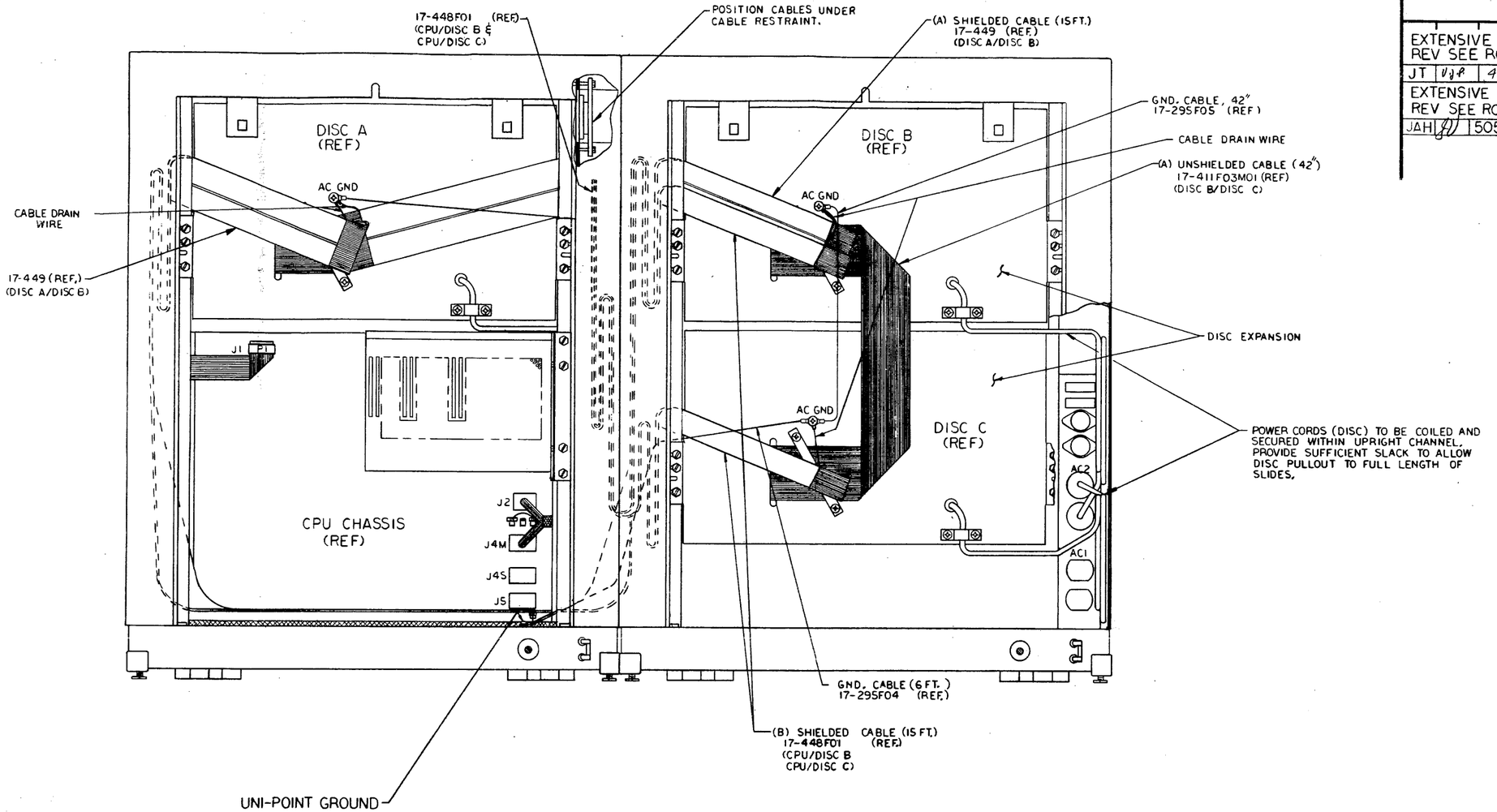
NOTES

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

12 SHEET NO.
C REV. LEVEL
D SHEET SIZE

TITLE INFORMATION DWG.
DOUBLE DISC EXPANSION
MOD 3210 , 208V

TASK	SHT
03175	1 - 2
DWG 02-756 R02 D12	



CPU CABINET (REF)

DOUBLE DISC EXPANSION CABINET

REAR VIEW

REVISIONS					
EXTENSIVE CHANGES FOR PREVIOUS REV SEE R00 MICROFILM COPY.					
JT	4868	R	10-15-81	R01	
EXTENSIVE CHANGES FOR PREVIOUS REV SEE R01 MICROFILM COPY					
JAH	5050	R	4 8 82	R02	

NOTES

DRAFTER	J. TAMULEVICIUS
DATE	6-9-81

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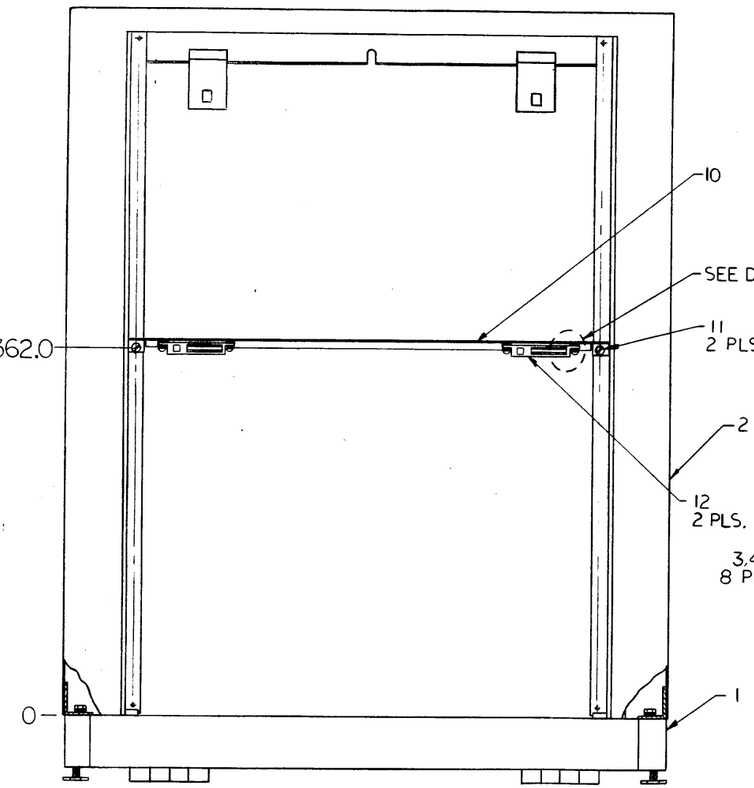
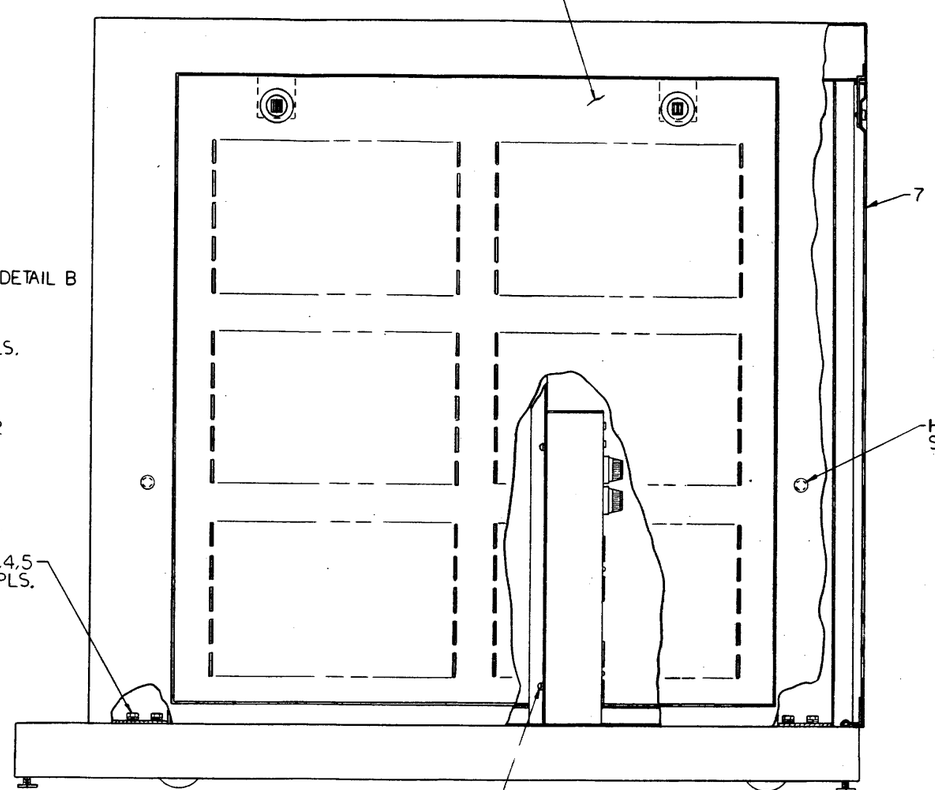
Computer Systems Division
Oceanport, N.J. 07757

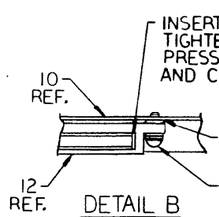
TITLE INFORMATION DWG.
DOUBLE DISC EXPANSION
MOD 3210 , 208V.

TASK	SHT
03175	2-2
DWG 02-756R02 D12	



FRONT





DETAIL B

09-142F02	AS SHOWN (400V INTERNATIONAL)
09-142F01	AS SHOWN (208V DOMESTIC)
PART NO.	DESCRIPTION
VARIATION TABLE	

MILLIMETERS	INCHES
362.0	14.25

NOTES

BRUNING 44-131 4079

REVISIONS		
PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	7-29-81
	PROD	9/25/81

RELEASED FOR PRODUCTION

MFG. ENG. _____ DATE 12/1/81

EXTENSIVE CHG'S MADE. SEE ROD MICROFILM:

JAH		9476	R	1-19-82	R01

METRIC

USED IN MANUAL: 47-022

UNLESS OTHERWISE SPECIFIED		
SCALE: 3/8	TOLERANCE:	
	INCHES	MILLIMETERS
DIMENSIONS ARE IN MILLIMETERS	.XXX ±.005 .XX ±.02 .X ±.03	.XX ± .13 .X ± .5 X ± .8

NAME	TITLE	DATE
J. TAMUL	DES/DFT	9-2-81
R. CERO	SUPV	12-8-81
	CHK	
D. FOGGIA	ENG	12-8-81
P. ABITANTE	MGR	12-8-81
R. BARKER	QC	12-7-81

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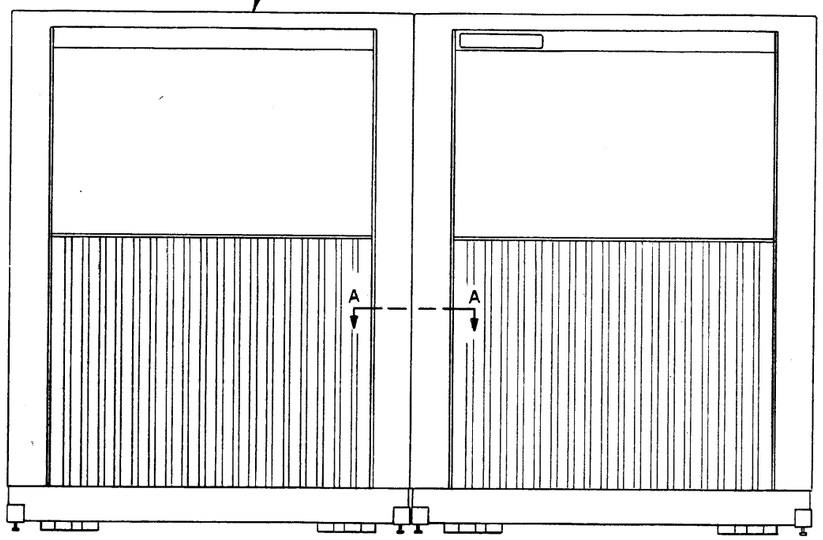
Oceanport, N.J. 07757

TITLE ASSEMBLY BASIC CABINET (REMOVABLE SIDE SKINS)

TASK	03175	SHT
DWG	09-142 R01 D03	1 - 1

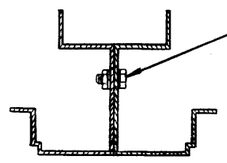
EXPANSION CABINET (REF.)
02-755F01, SINGLE DISC, DOMESTIC
02-755F02, SINGLE DISC, INTERNATIONAL
02-755F03, I/O & SINGLE DISC, DOMESTIC
02-755F04 I/O & SINGLE DISC, INTERNATIONAL



FRONT VIEW

PREFERRED LOCATION FOR SINGLE DISC EXPANSION OR I/O & SINGLE DISC EXPANSION CABINET

CPU CABINET



SECTION A-A

WHEN BOLTING CABINETS TOGETHER; REMOVE APPROPRIATE HOLE PLUGS AND SIDE SKINS.
BOLT TOGETHER WITH:
1 EA, 5/16-18 X 3/4" HEX HEAD BOLT, 16-410F01
2 EA, 5/16 EXTERNAL TOOTH LOCKWASHER, 16-380F05
1 EA, 5/16-18 HEX NUT, 16-058F05

NOTES

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

2	SHEET NO.
05	REV. LEVEL
D	SHEET SIZE

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
DEV		8-28-81
PROD		8/28/81

EXTENSIVE CHANGES FOR PREVIOUS REV. SEE R00 MICROFILM COPY. REVISED SHT. 2

JT	WJA	4868	R	10-15-81	R01
REVISED SHT. 2					
JT	MF	4913	R	12-3-81	R02 X

RELEASED FOR PRODUCTION
MFG. ENG. MJO DATE 12/9/81

REVISED SHT 2

KR		5050	R	5-17-82	R03 X

USED IN MANUAL 47-022

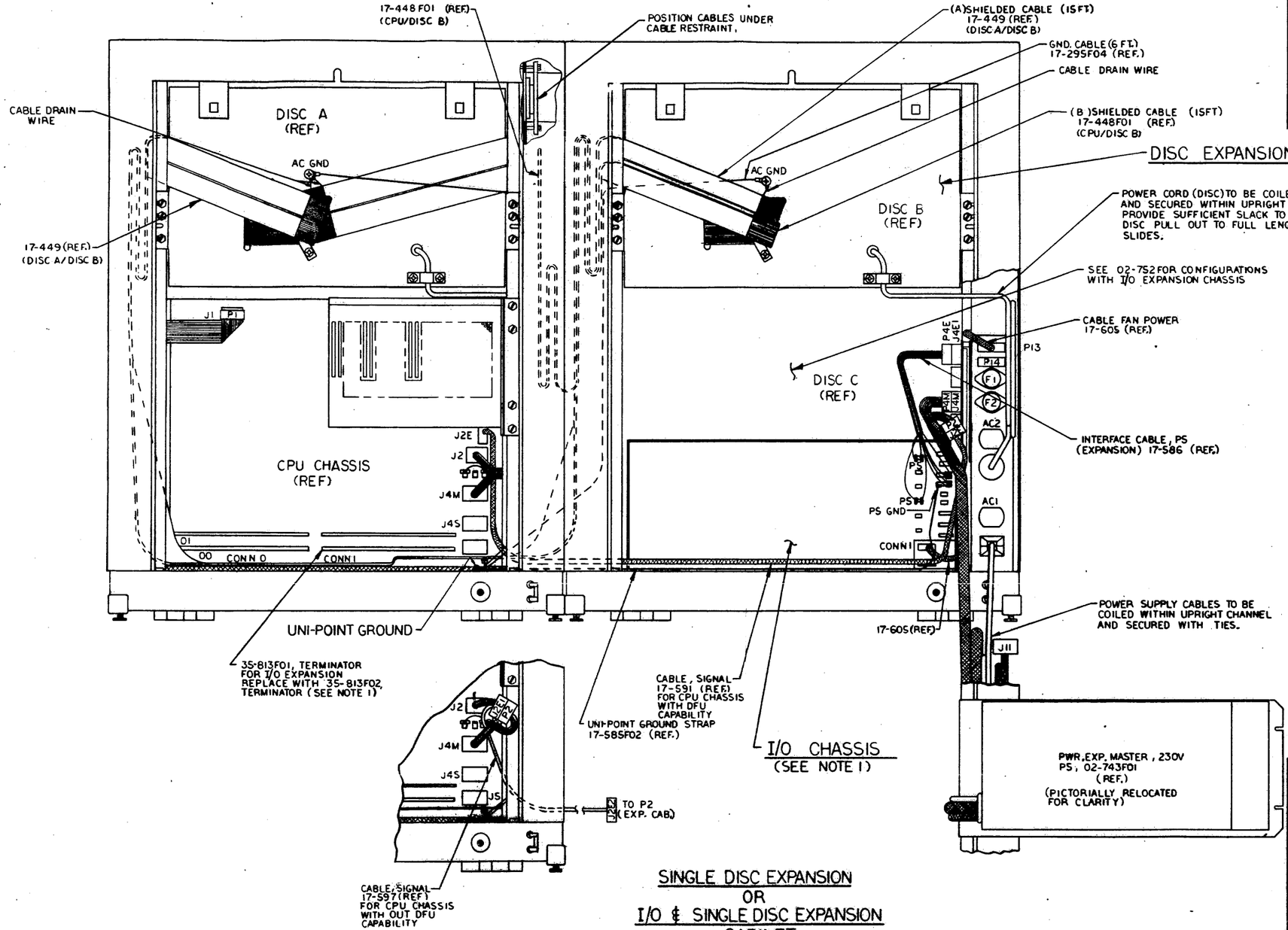
UNLESS OTHERWISE SPECIFIED			
SCALE: 1/4	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
	J TAMUL	DES/DFT	6-8-81
R CERO		SUPV	12-8-81
		CHK	
R DENGEL		ENG	12-8-81
P ABITANTE		MGR	12-8-81
R BARKER		QC	12-4-81

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE
INFORMATION DWG.
SINGLE DISC EXPANSION OR I/O & SINGLE DISC EXPANSION CABINET
MOD 3210 , 208V

TASK	03175
DWG	02-755R03 D12
SHT	1-2

REVISIONS				
EXTENSIVE CHANGES FOR PREVIOUS REV. SEE R01 MICROFILM COPY.				
JT	[illegible]	4913	R	12-3-81 R02
EXTENSIVE CHANGES FOR PREVIOUS REV. SEE R02 MICROFILM COPY.				
JAH	[illegible]	5050	R	4-8-82 R03



NOTES 1. SEE 02-754 D12, SHT. 3 FOR TYPICAL I/O CABLE AND TERMINATOR CONFIGURATIONS.

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Oceanport, N.J. 07757

DRAFTER	J TAMULEVICIUS
DATE	6-9-81

TITLE INFORMATION DWG. SINGLE DISC EXPANSION OR I/O & SINGLE DISC EXPANSION CABINET MOD 3210, 208V

TASK 03175 | SHT 2-2

DWG 02-755 R03 D12

REVISIONS		
PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	8 28 81
	PROD MJQ	8/28/81

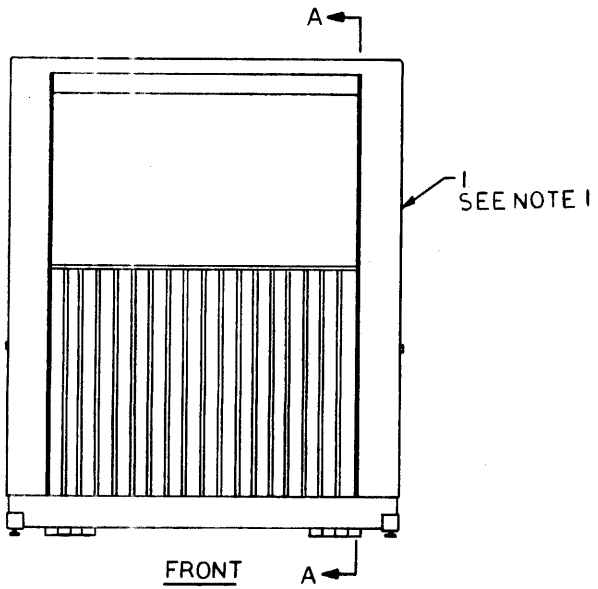
AREA D4, RMVD. ITEM 6, 4 PLS.
AREA J4, RMVD. ITEM 3
CHANGED ITEM 1, PICTORIALLY
REVISED SHEET 2

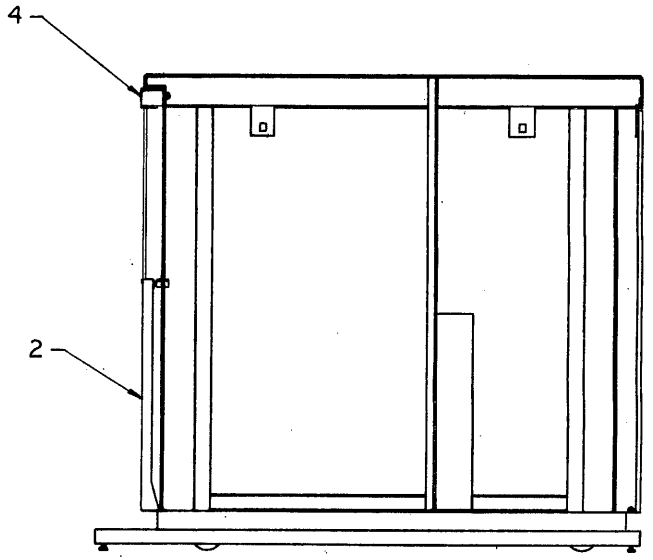
JT	D.P.	4868	R	10-15-81 R01

REVISED SHT. 2

JT	DF	4913	R	12 3 81 R02

RELEASED FOR PRODUCTION
MFG. ENG. MJQ DATE 12/9/81





SECTION A-A

METRIC

USED IN MANUAL 47-022

VARIATION TABLE	
PART NO	DESCRIPTION
02-755 F01	AS SHOWN, SHT. 1 (SINGLE DISC, DOMESTIC, 208V)
02-755 F02	AS SHOWN, SHT. 1 (SINGLE DISC, INTERNATIONAL, 208V)
02-755 F03	AS SHOWN, SHT. 2 (I/O & SINGLE DISC, DOMESTIC, 208V)
02-755 F04	AS SHOWN, SHT. 2 (I/O & SINGLE DISC, INTERNATIONAL, 208V)

NOTES
1. ITEMS 7- TO BE INSTALLED PER 02-755 D12

2	SHEET NO
02	REV LEVEL
C	SHEET SIZE

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

UNLESS OTHERWISE SPECIFIED
SCALE: 3/16
DIMENSIONS ARE IN MILLIMETERS

	MILLIMETERS	INCHES
	.XX ± .13	.XXX ± .005
	.X ± .5	.XX ± .02
	.X ± .8	.X ± .03

NAME	TITLE	DATE
J TAMUL	DES/DFT	6-5-81
R CERO	SUPV	12-8-81
	CHK	
R DENGEL	ENG	12-8-81
P ABITANTE	MGR	12-8-81
R BARKER	QC	12-4-81

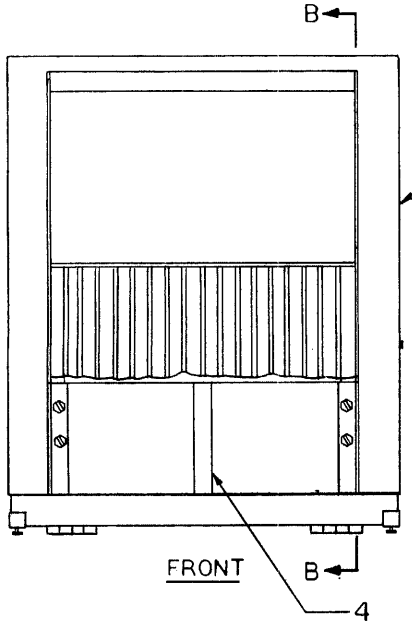
PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

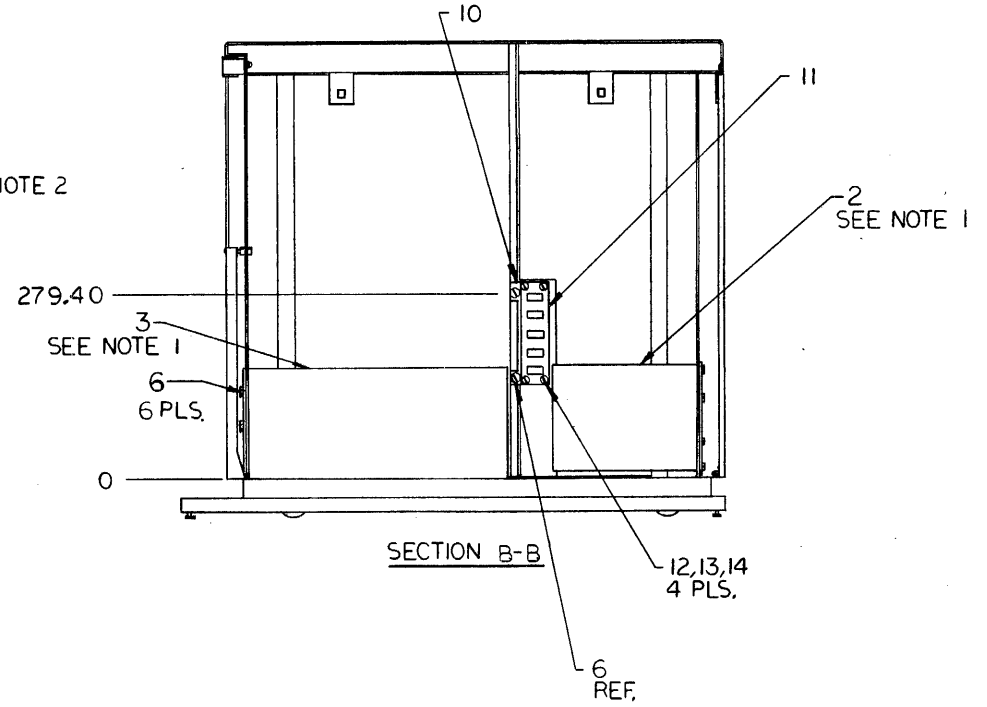
TITLE ASSEMBLY
MOD 3210 SINGLE DISC EXP. CAB. OR I/O & SINGLE DISC EXP. CAB.

TASK 03175
DWG 02-755 R02 C03
SHT 1-2

MILLIMETERS	INCHES
279.40	11.00

REVISIONS				
CHANGED ITEM 1 PICTORIALLY ADDED DIM. AREA GS, SECTION B-B WAS A-A				
JT	4868	R	10-15-81	R01
ADDED ITEMS 15-19 TO NOTE 2				
JT	4913	R	12-3-81	R02





NOTES

1. FOR TERMINATION OF CABLES SEE 02-755 D12
2. ITEMS 7-9,15-19 TO BE INSTALLED PER 02-755D12, SHT. 2

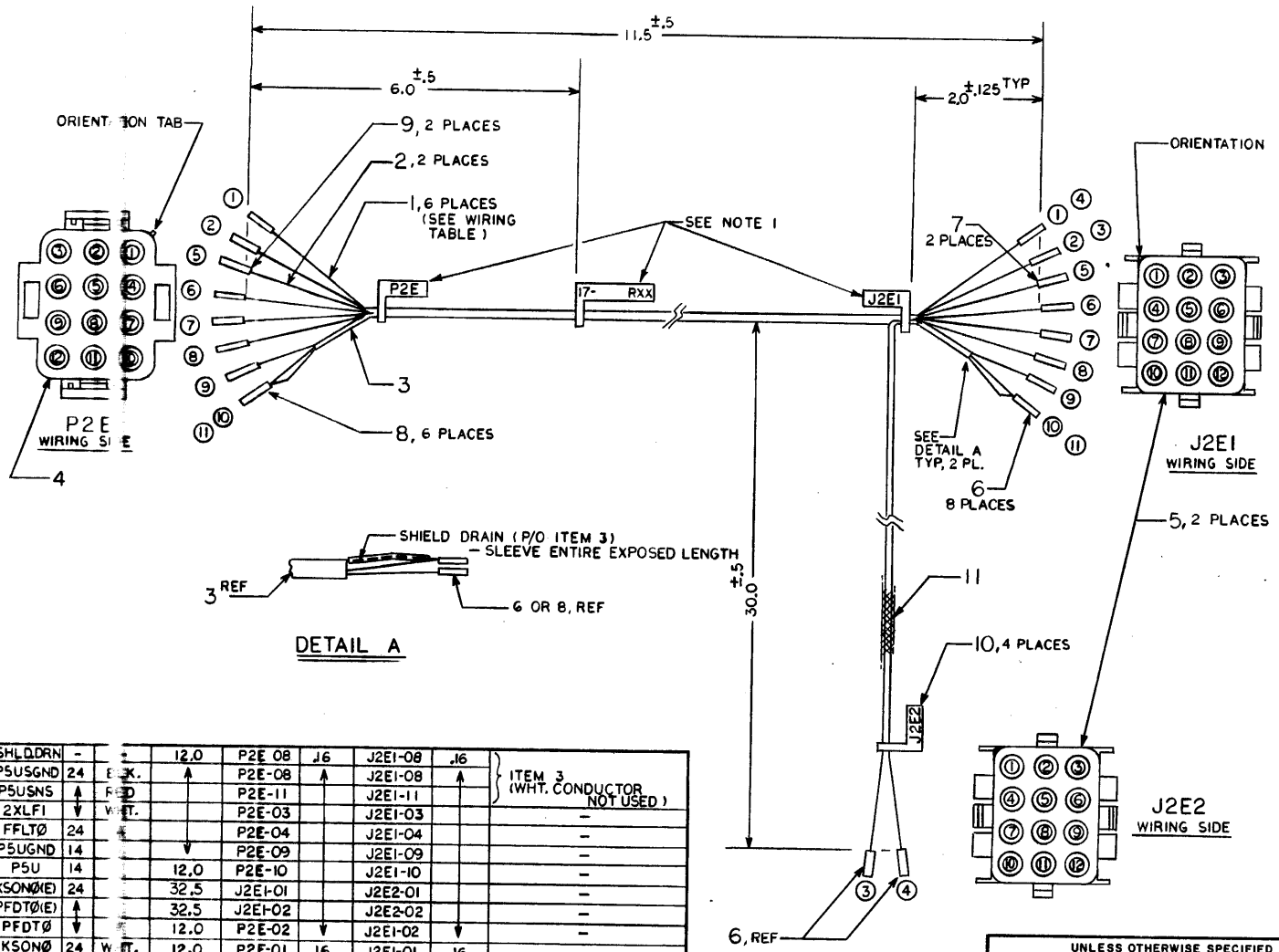
NAME		TITLE	DATE
	J TAMUL	DES / DFT	6-5-81
R CERO		SUPV	
		CHK	
R DENGEL		ENG	
P ABITANTE		MGR	
R BARKER		QC	

PERKIN-ELMER

Computer Systems, Division
Oceanport, N.J. 07757

TITLE ASSEMBLY
MOD 3210 SINGLE DISC EXP. CAB. OR I/O & SINGLE DISC EXP. CAB.

TASK 03175 | SHT 2-2
DWG 02-755 R02 C03



WIRE NO.	SIGNAL	GA.	COLOR	LENGTH REF.	FROM	STRIP	TO	STRIP	REMARKS
11	SHLDDRN	-		12.0	P2E 08	.16	J2E1-08	.16	ITEM 3 (WHT. CONDUCTOR NOT USED)
10	P5USGND	24	BLK.		P2E-08		J2E1-08		
9	P5USNS		RED		P2E-11		J2E1-11		
8	2XLFI		WHT.		P2E-03		J2E1-03		–
7	FFLTØ	24			P2E-04		J2E1-04		–
6	P5UGND	14			P2E-09		J2E1-09		–
5	P5U	14		12.0	P2E-10		J2E1-10		–
4	KSONØ(E)	24		32.5	J2E1-01		J2E2-01		–
3	PFDTØ(E)			32.5	J2E1-02		J2E2-02		–
2	PFDTØ			12.0	P2E-02	.16	J2E1-02	.16	–
1	KSONØ	24	WHT.	12.0	P2E-01	.16	J2E1-01	.16	–

WIRING TABLE

NOTES 1. IDENTIFY AS SHOWN.

30.5	775.
30.0	762.
12.0	305.
11.5	292.
6.0	152.
2.0	50.8
.5	12.7
.16	4.0
.125	3.2
INCH	MM

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	8-1-81
	PROD MJQ	8/28/81

PRE APPROVAL PRINTS

AREA G5 - ADDED SLEEVING, ITEM 11. ADDED TOLERANCES TO DETAIL & MM CONV. CHART ADDED "USED IN MANUAL" NOTE.

WF		-	-	12-8-81	R01

RELEASED FOR PRODUCTION
MFG. ENG. MJQ DATE 12/8/81

IN WIRING TABLE, WIRE LENGTHS OF 3 & 4 WERE 30.5 :

MH		5046	R	5-18-82	R02

METRIC

USED IN MANUAL: 47-022

UNLESS OTHERWISE SPECIFIED

SCALE: NONE

TOLERANCE:

DIMENSIONS ARE IN INCHES	INCH	MM
	.XXX ±.005	.X ±.5
	.XX ±.05	X. ±.8
	.X ±.05	

NAME	TITLE	DATE
W. FRASER	DES / DFT	8-7-81
R. CERO	SUPV	12-8-81
	CHK	
D. FOGGIA	ENG	12-8-81
P. ABITANTE	MGR	12-8-81
R. BARKER	QC	12-8-81

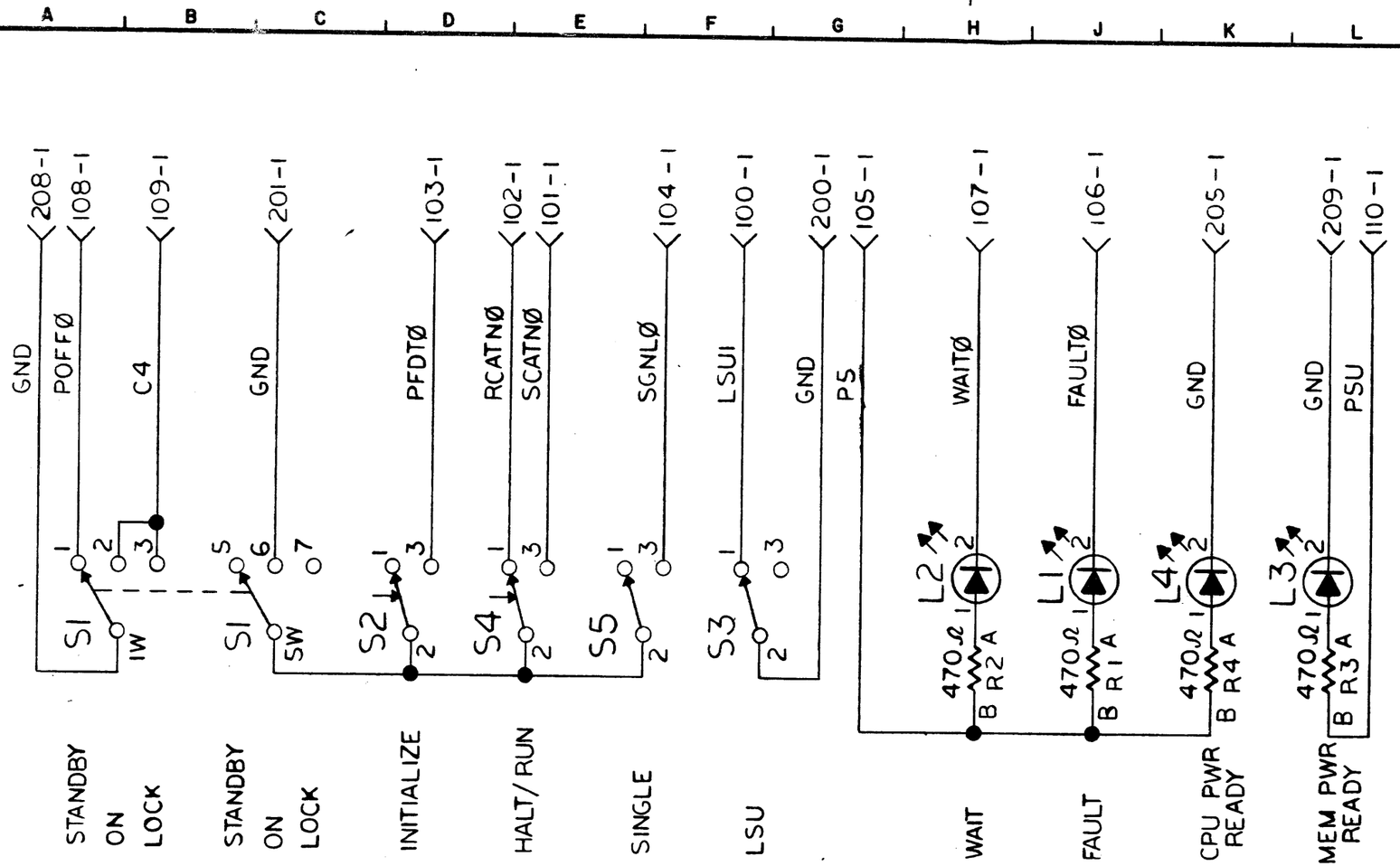
PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE CABLE, I/O EXP.
(INTERIM)

TASK 03175 | SHT 1 - 1

DWG 17-597 R02 C03

BRUNING 44-131 40579



REVISIONS		
PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	12-18-81
	ENG	

RELEASED FOR PRODUCTION
MFG. ENG. _____ DATE 3-3-82

USED IN MANUAL : 47-022

NOTES

UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ± .005 .X ± .03 .XX ± .02 ANGLES ± 1°	
NAME	TITLE	DATE
J TAMUL	DES / DET	11-5-81
R. CERO	SUPV	2-19-82
	CHK	
R DENGEL	ENG	2-19-82
P. ABITANTE	MGR	2-19-82
R. BAPKER.	QC	2-19-82

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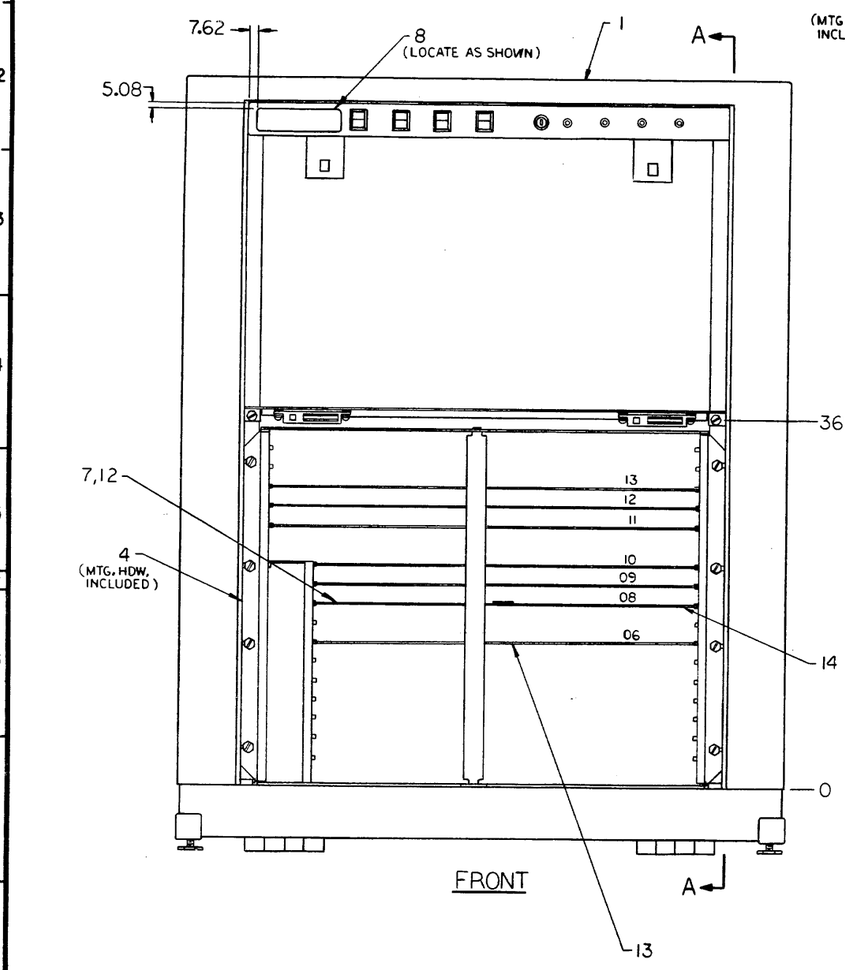
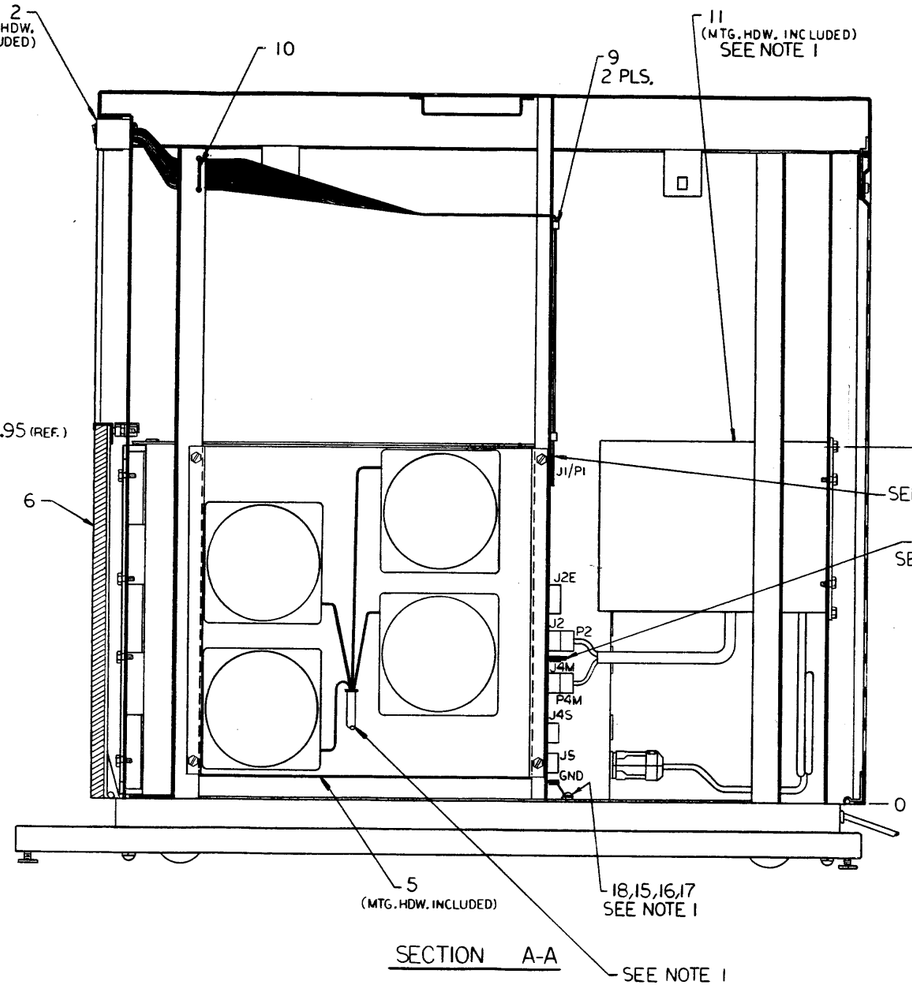
Oceanport, N.J. 07757

TITLE
SCHEMATIC
CONTROL PANEL

TASK 03131 SHT 1-1
DWG 09-148 B08

MILLIMETERS	INCHES
5.08	.20
7.62	.30
349.25	13.75
361.95	14.25





REVISIONS		
	INIT	DATE
PRE PRODUCTION APPROVAL	DEV	9-29-81
	PROD	9/25/81

IN AREA J5, FAN ASS'Y WAS PICTORIALLY SHOWN MOUNTED TO CABINET FROM INSIDE.

VT	CDF	4913	R	12-8-81	R01

RELEASED FOR PRODUCTION
MFG. ENG. MJA DATE 12/8/81

METRIC

USED IN MANUAL 47-022

UNLESS OTHERWISE SPECIFIED		
SCALE: ~	TOLERANCE:	
	MILLIMETERS	INCHES
DIMENSIONS ARE IN MILLIMETERS	.XX ± .13 .X ± .5 X. ± .8	.XXX ± .005 .XX ± .02 .X ± .03

NAME	TITLE	DATE
J. TAMUL	DES/DFT	9-5-81
R. CERO	SUPV	12-18-81
	CHK	
D. FOGGIA	ENG	12-18-81
P. ABITANTE	MGR	12-18-81
R. BARKER	QC	12-17-81

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

01-196F02	INTERNATIONAL

PART NO	DESCRIPTION
VARIATION TABLE	

NOTES 1. SEE 01-196 D12, SHT. 3 FOR TERMINATION OF CABLES.

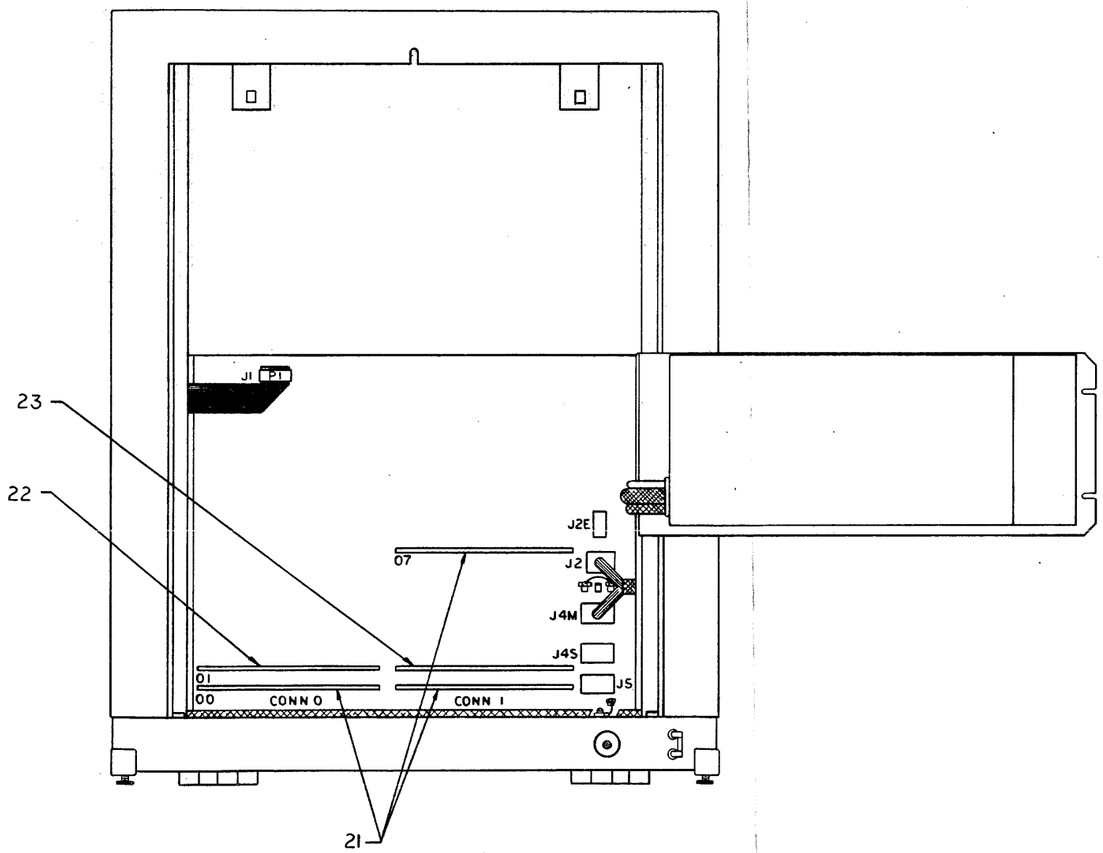
12	1	SHEET NO
00	01	REV. LEVEL
D	D	SHEET SIZE

REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT

TITLE
ASSEMBLY, BASIC
SYSTEM CABINET W/O DFU
MOD 3210, 208V

TASK 03175	SHT
DWG 01-196 R01 D03	1 - 2

REVISIONS



REAR VIEW

NOTES

DRAFTER	J TAMULEVICIUS
DATE	9-2-81

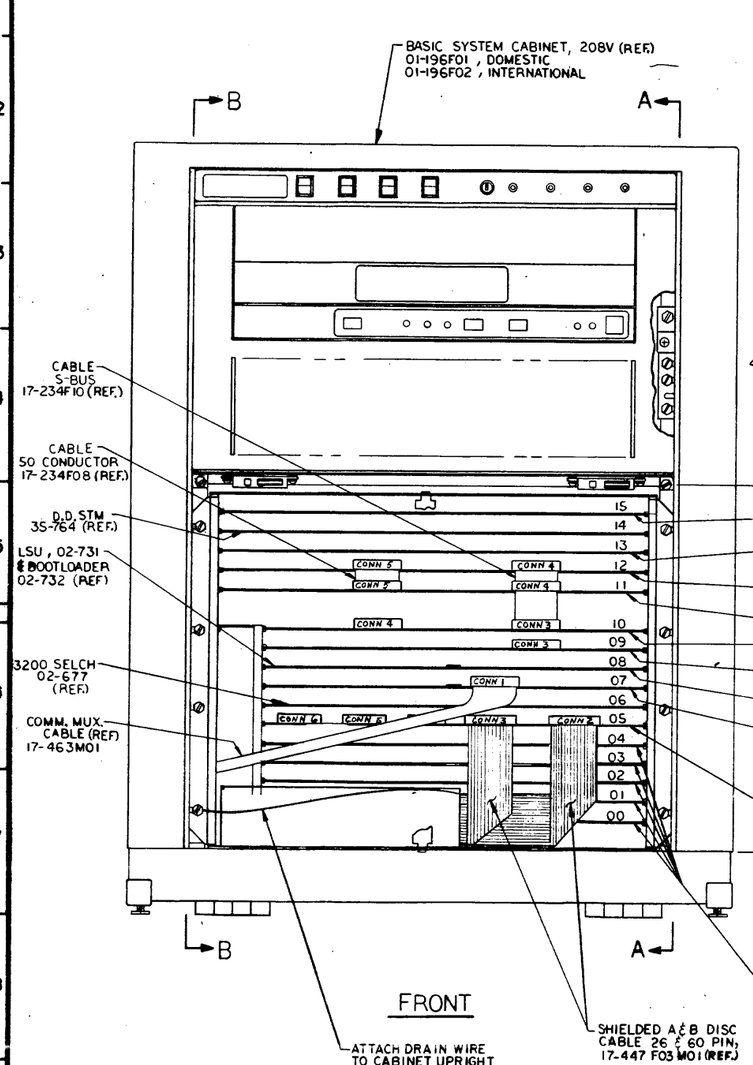
PERKIN-ELMER

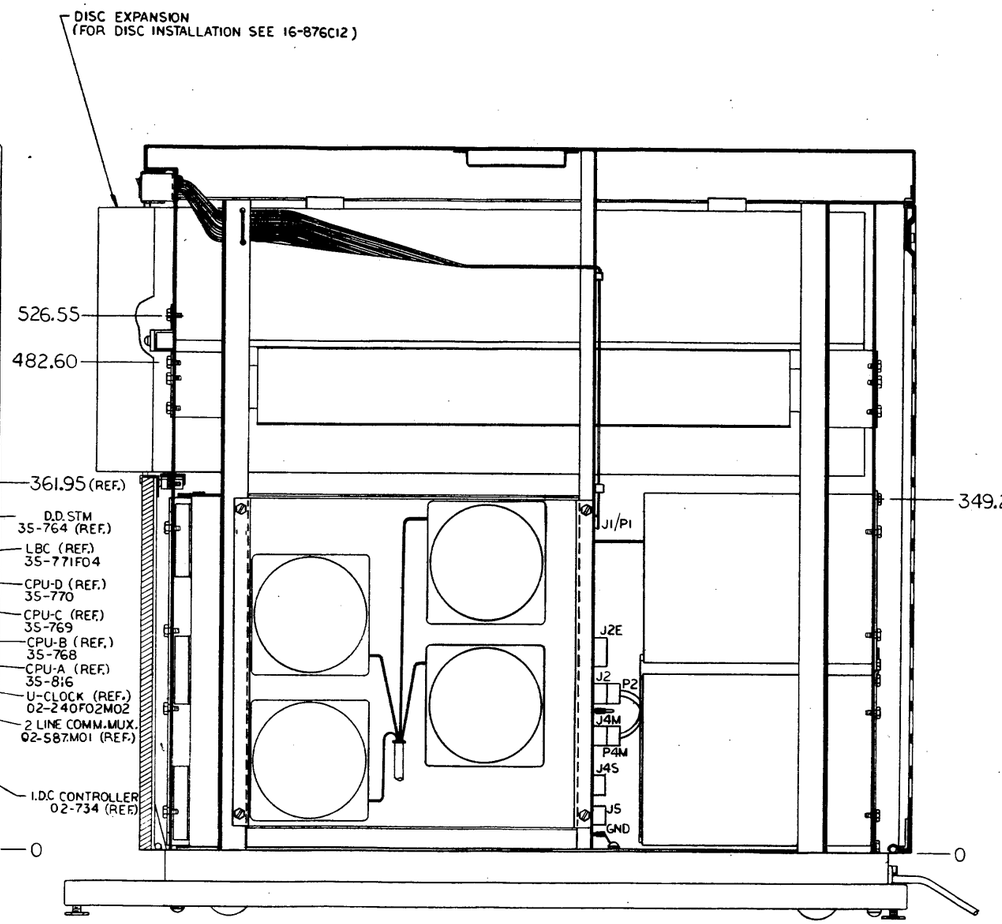
Computer Systems Division
Oceanport, N.J. 07757

TITLE ASSEMBLY , BASIC SYSTEM CABINET W/O DFU MOD 3210 , 208V

TASK 03175		SHT 2-2
DWG 01-196	D03	

MILLIMETERS	INCHES
526.55	20.75
482.60	19.00
361.95	14.25
349.25	13.75





BASIC CABINET

REVISIONS					
PRE PRODUCTION APPROVAL	INIT	DATE			
	DEV	9-25-81			
	PROD	9/25/81.			
IN AREA F6, CPU-A (REF.) WAS 35-798					
VT		4803	R	12-8-81	R01
IN AREA J5, FAN. ASS'Y WAS PICTORIALLY SHOWN MOUNTED TO CABINET FROM INSIDE, REVISED SHT. 3.					
VT	JMF	4913	R	12-8-81	R02 X
RELEASED FOR PRODUCTION MFG. ENG. MJG DATE 12/18/81					
EXTENSIVE CHANGE MADE: SEE MICRO FILM R02: REV'D SHTS 2 & 3:					
JAH	JV	5050	R	9-7-82	R03 X

METRIC

USED IN MAUNAL 47-022

UNLESS OTHERWISE SPECIFIED		
SCALE: ~	TOLERANCE:	
	MILLIMETERS	INCHES
DIMENSIONS ARE IN MILLIMETERS	.XX ±.13 .X ±.5 X. ±.8	.XXX ±.005 .XX ±.02 .X ±.03

NAME		TITLE	DATE
J. TAMUL		DES/DFT	9-10-81
R. CERO		SUPV	12-18-81
		CHK	
D. FOGGIA		ENG	12-18-81
P. ABITANTE		MGR	12-18-81
R. BARKER		QC	12-17-81

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

SHEET NO.	1	2	3
REV. LEVEL	3	1	2
SHEET SIZE	D	D	D

NOTES

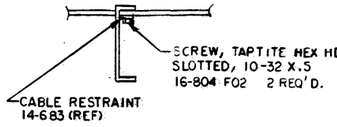
THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

TITLE
INFORMATION DWG.
W/O DFU
MOD 3210 , 208V

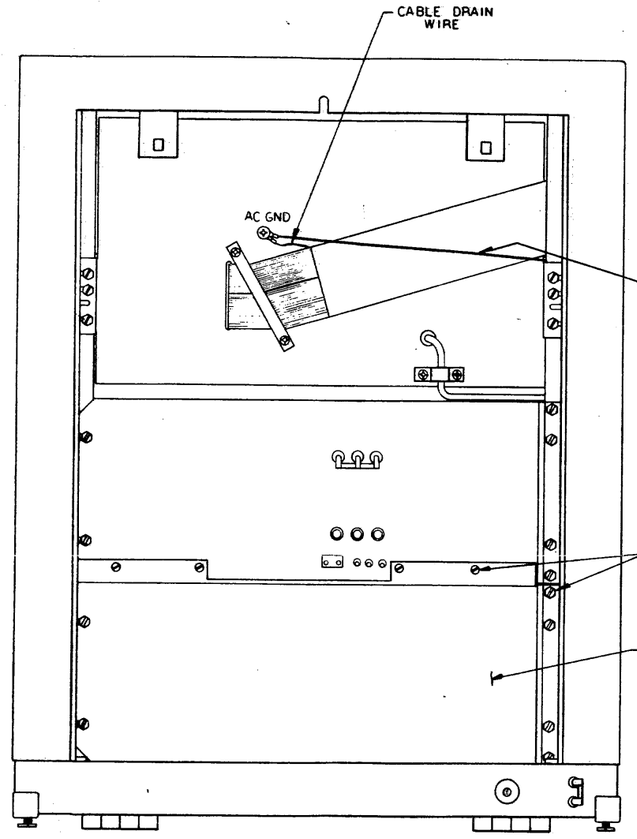
TASK	03175	SHT
DWG	01-196 R03 D12	1-3

DRAWING 44-131-4079

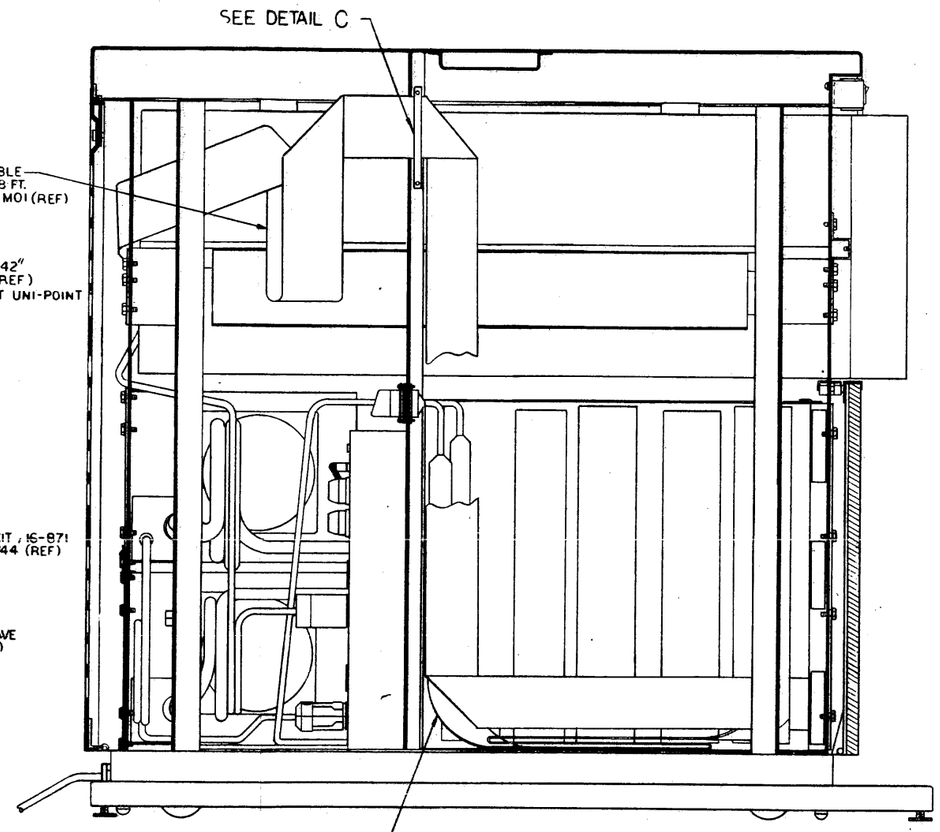
REVISIONS					
EXTENSIVE CHANGES MADE: SEE MICROFILM R00:					
JAH		5050	R	4-7-82	R01



DETAIL C



REAR



SECTION B-B

BASIC CABINET

NOTES

DRAFTER	J TAMULEVICIUS
DATE	9-11-81

PERKIN-ELMER

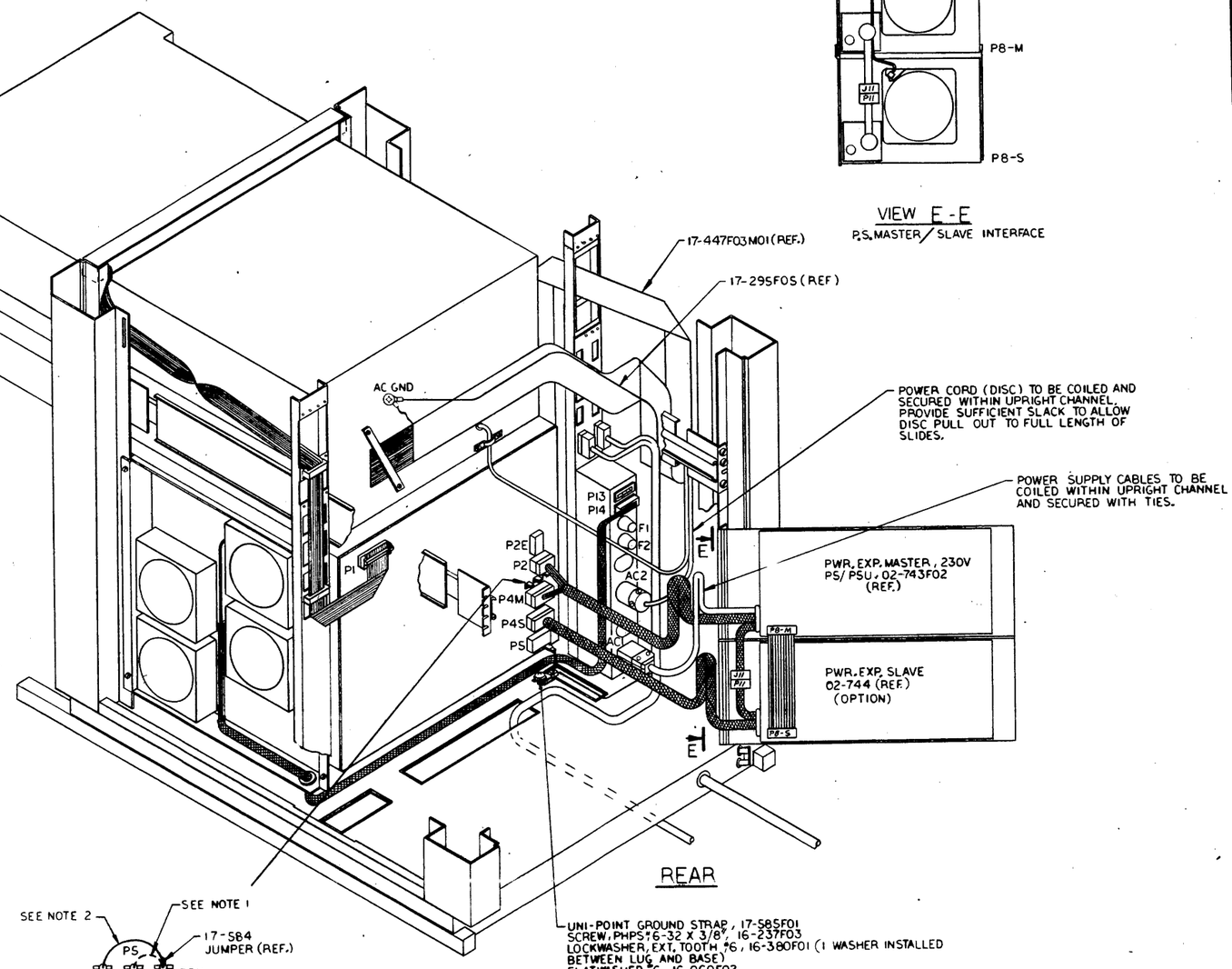
Computer Systems Division
Oceanport, N.J. 07757

TITLE INFORMATION DWG.

MOD 3210, 208V

TASK 03175		SHT 2-3
DWG 01-196 R01	D12	

REVISIONS						
AREA EG, FAN ASS'Y WAS PICTORIALLY SHOWN MOUNTED TO CABINET FROM INSIDE.						
VT	CBF	4913	R	12-8-81	R01	X
EXT. CHANGES MADE: SEE MICRO FILM R01						
JAH	JJ	5050	R	4-7-82	R02	



VIEW E-E
P.S. MASTER/SLAVE INTERFACE

BASIC CABINET

NOTES
1. CONNECT B TO C, TO POWER P5U FROM P5 IF P.S. 02-743F01 (P5 ONLY) IS USED.
2. CONNECT A TO C, WHEN P.S. 02 743F02 (P5/P5U) IS USED.

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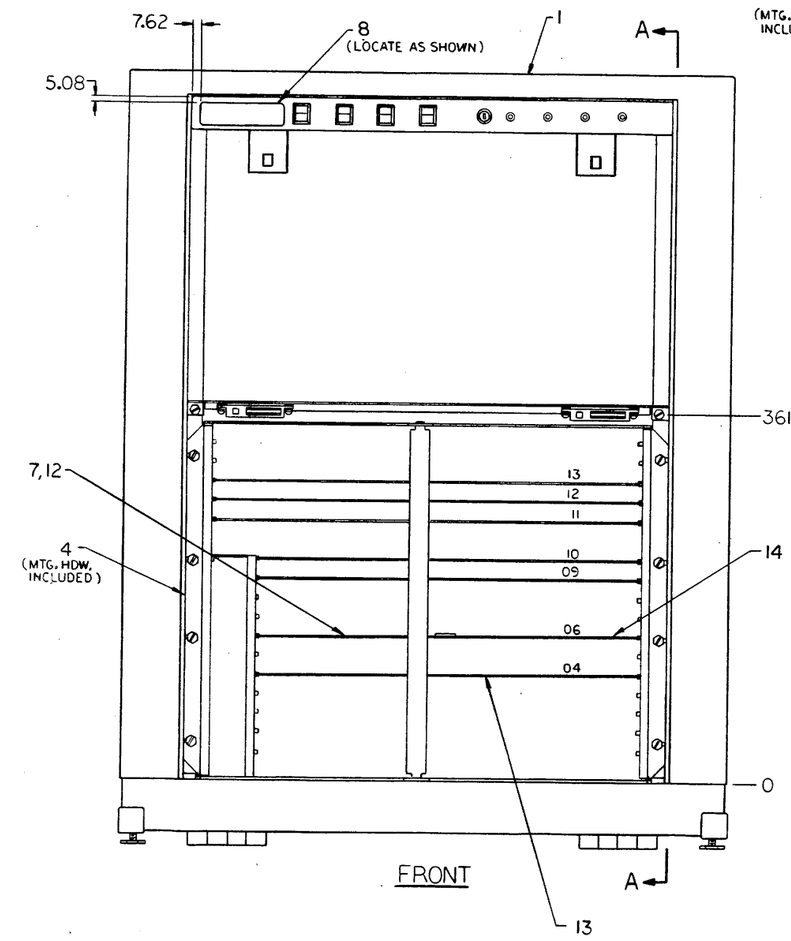
Oceanport, N.J. 07757

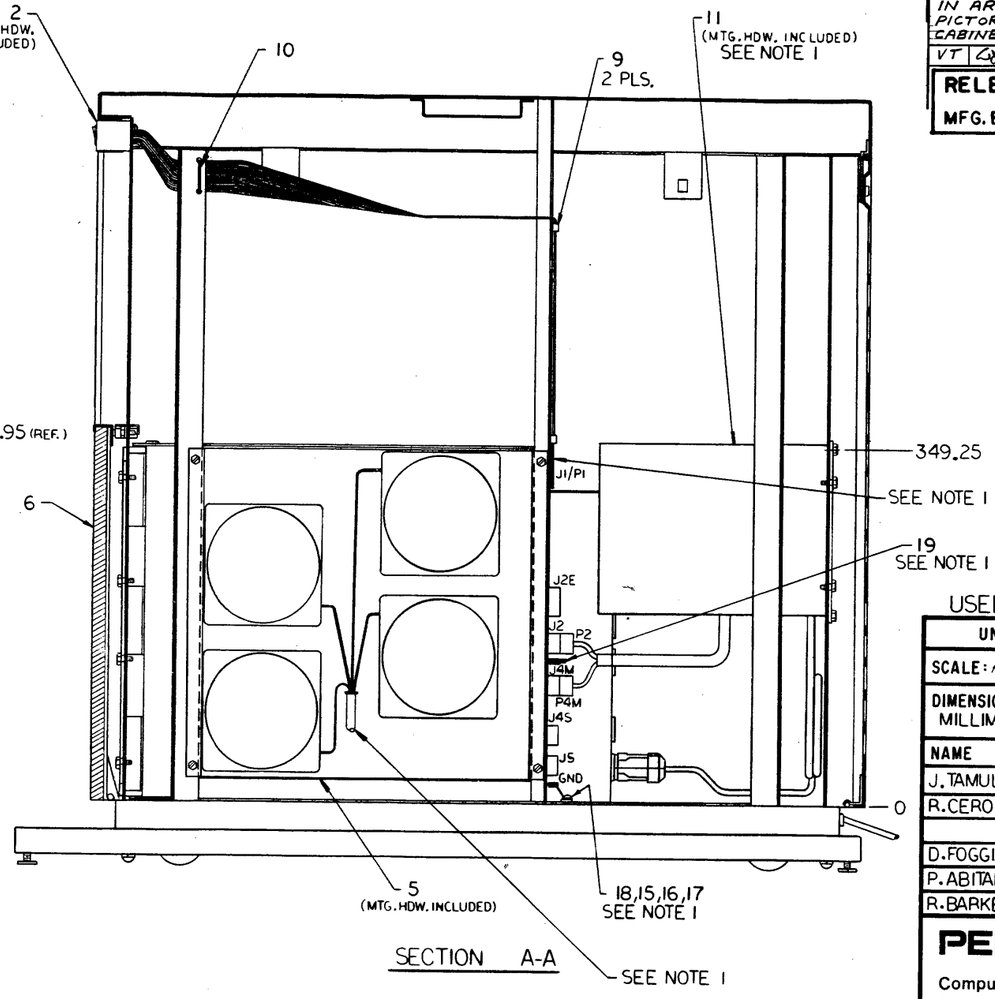
DRAFTER	J TAMULEVICIUS
DATE	9-15-81

TITLE: INFORMATION DWG.
MOD 3210, 208V

TASK	03175	SHT
DWG	01-196 R02 D12	3-3

MILLIMETERS	INCHES
5.08	.20
7.62	.30
349.25	13.75
361.95	14.25





REVISIONS		
PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	9-25-81
	PROD	9/25/81

IN AREA J5, FAN ASS'Y WAS PICTORIALLY SHOWN MOUNTED TO CABINET FROM INSIDE.

VT	GF	4913	R	12-8-81	R01

RELEASED FOR PRODUCTION
MFG. ENG. _____ DATE 12/18/81

METRIC

USED IN MANUAL 47-022

UNLESS OTHERWISE SPECIFIED		
SCALE: ~	TOLERANCE: MILLIMETERS	INCHES
DIMENSIONS ARE IN MILLIMETERS	.xx ± .13 .x ± .5 x. ± .8	.xxx ± .005 .xx ± .02 .x ± .03

NAME	TITLE	DATE
J. TAMUL	DES/DFT	9-5-81
R. CERO	SUPV	12-18-81
	CHK	
D. FOGGIA	ENG	12-18-81
P. ABITANTE	MGR	12-18-81
R. BARKER	QC	12-17-81

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

01-197F02	INTERNATIONAL

PART NO	DESCRIPTION
VARIATION TABLE	

NOTES 1. SEE 01-197 D12, SHT. 3 FOR TERMINATION OF CABLES.

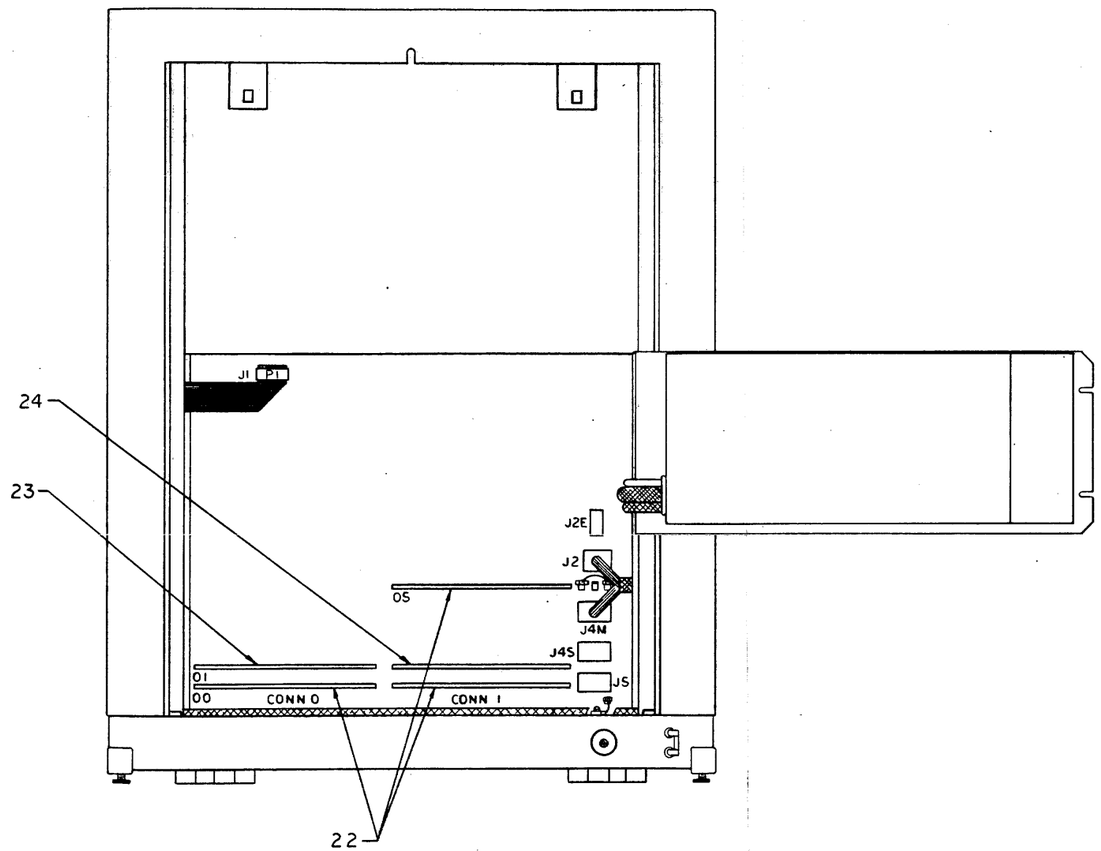
2	1	*SHEET NO
00	01	REV. LEVEL
D	D	SHEET SIZE

REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT

TITLE
ASSEMBLY, BASIC SYSTEM CABINET W/DFU
MOD 3210, 208V

TASK 03175	SHT
DWG 01-197 R01 D03	1 - 2

SHUNING 44-131 40979



REAR VIEW

REVISIONS

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

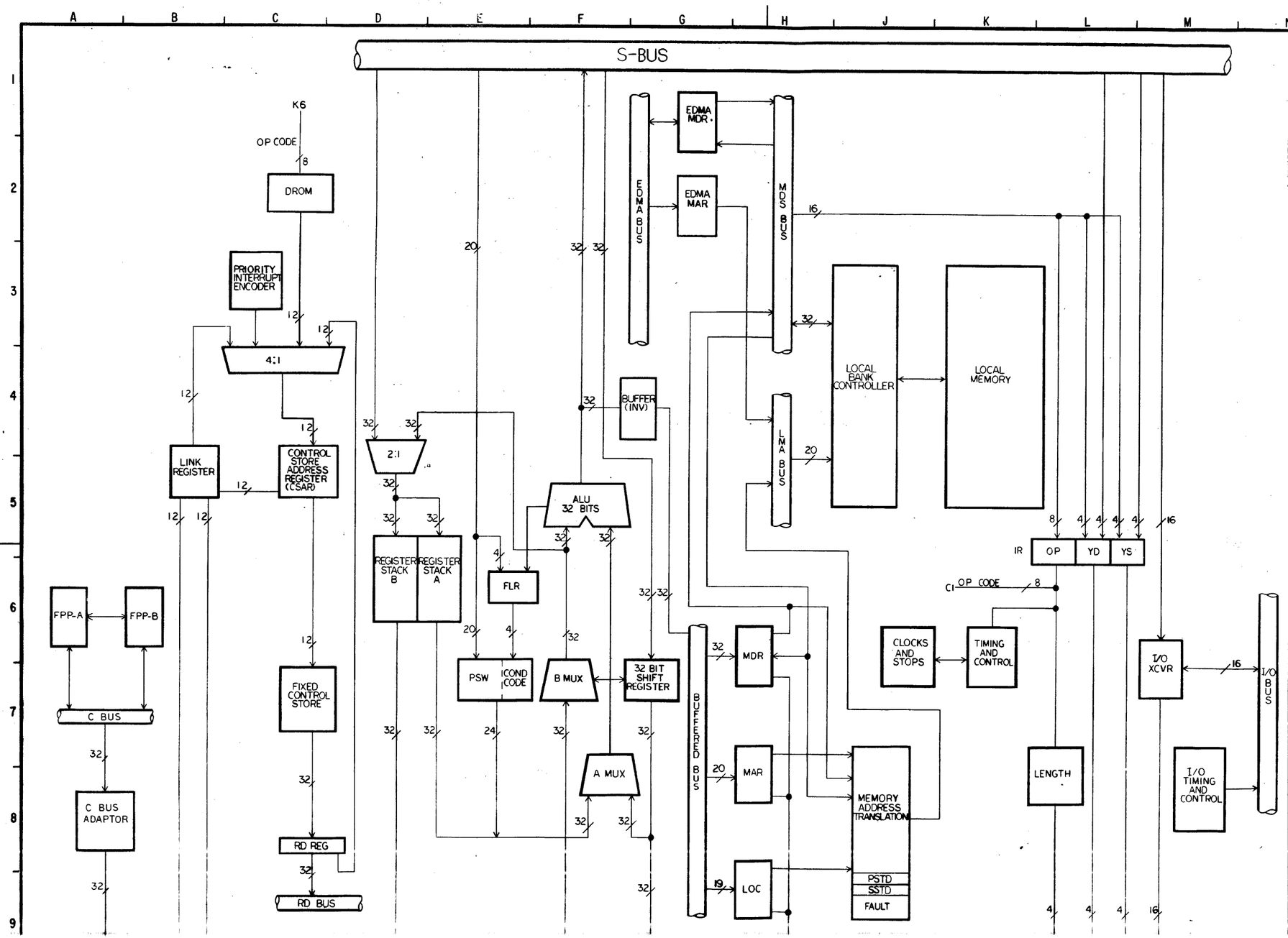
TITLE: ASSEMBLY, BASIC SYSTEM CABINET W/DFU MOD 3210, 208V

NOTES

DRAFTER	
J. TAMULEVICIUS	
DATE	
9-2-81	

TASK 03175	SHT 2-2
DWG 01-197 D03	

RRUNNING 44-131-40579-2



REVISIONS			
PRE PRODUCTION APPROVAL	INIT	DATE	
	DEV		
	ENG	mm	9-22-81
REVISED SHT 4.			
JLV	GNF	4915	M	12-10-81	R01	X

RELEASED FOR PRODUCTION
DEV. ENG. _____ DATE _____

USED IN MANUAL: 47-022

UNLESS OTHERWISE SPECIFIED	
SCALE: NONE	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME		TITLE	DATE
B. LUSK	J. VERBOSH	DES / DFT	4/6/81
R. CERO		SUPV	
E. GREENSTEIN		TEST	
M. MANGIONE		ENG	
P. OBRDA		MGR	
R.A. BARKER		QC	

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Oceanport, N.J. 07757

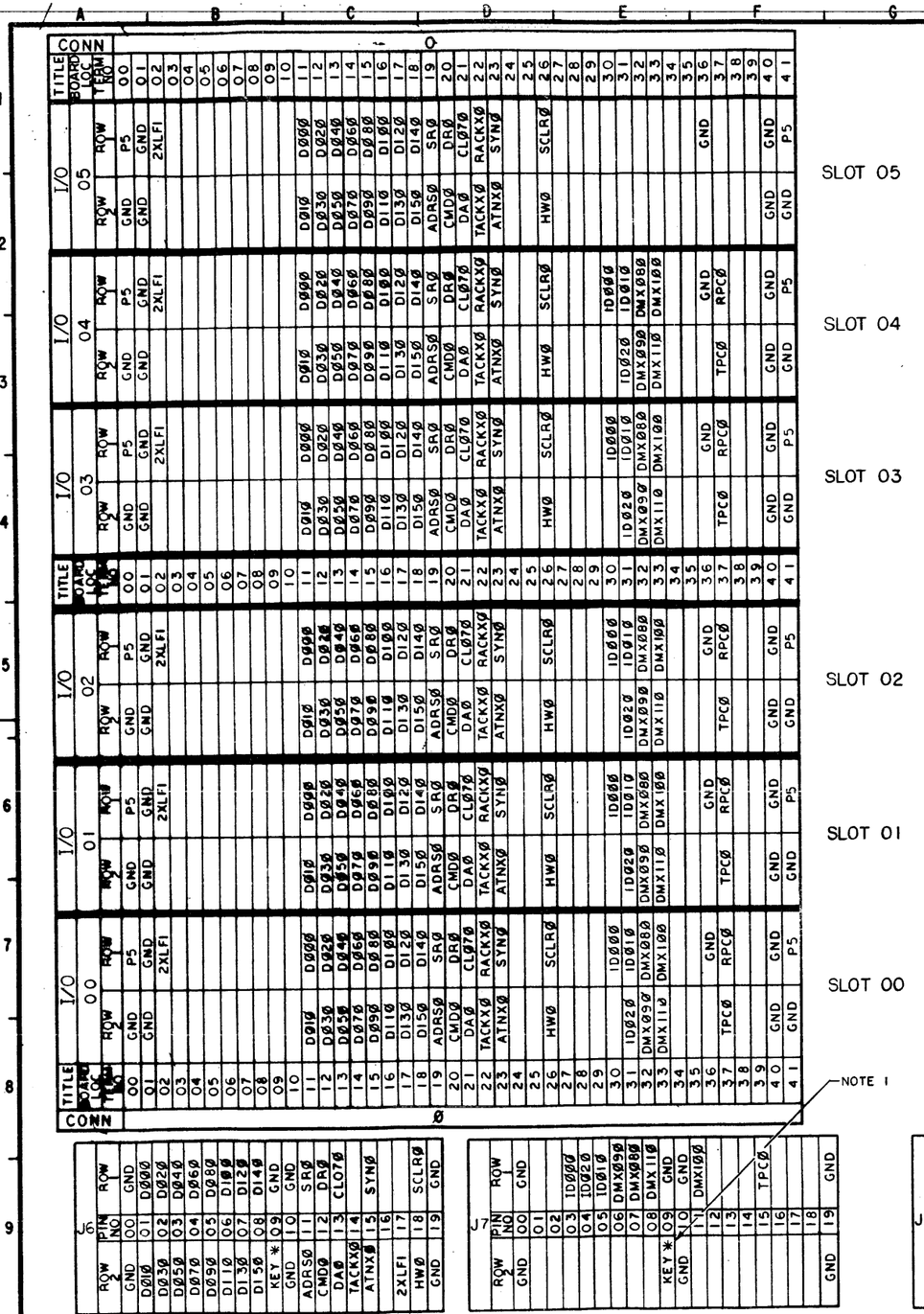
TITLE DFU
BACKPANEL MAP
W/ HPFPP

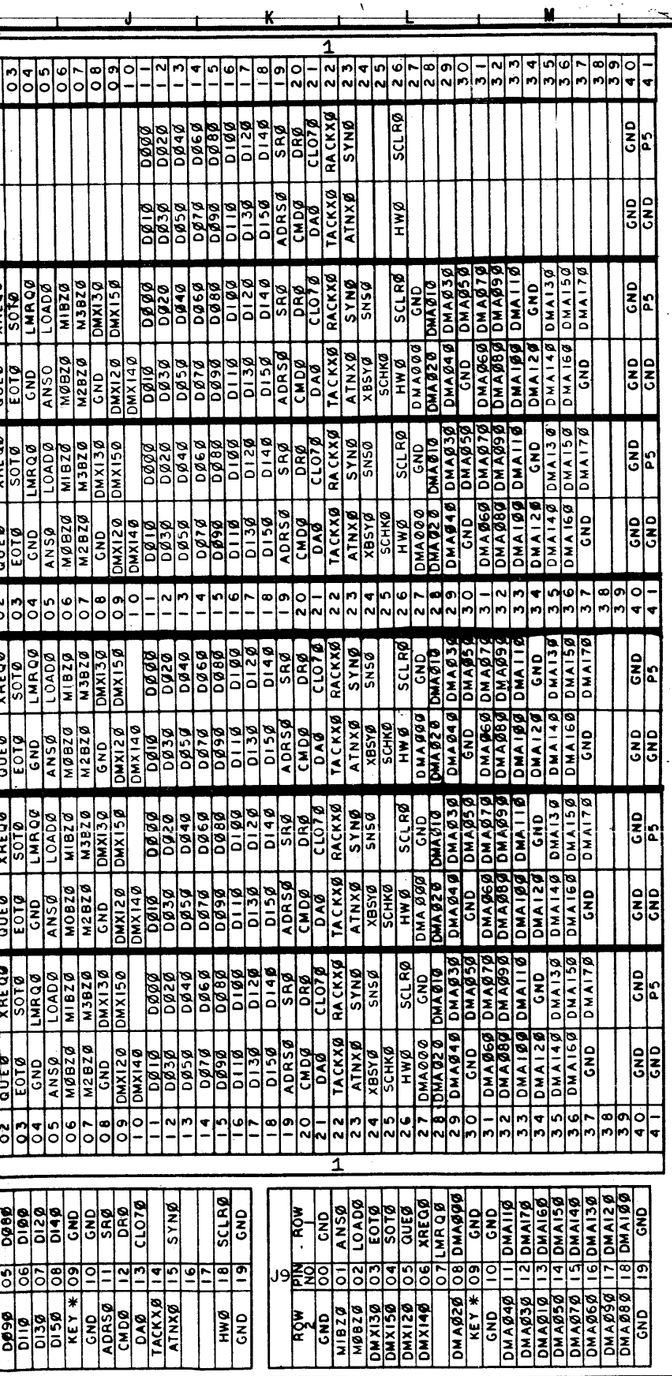
TASK 03179	SHT
DWG 01-197 R01 D08	1 - 4

NOTES: THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

REVISION	1	0	0	1
SHEET	1	2	3	4

BRUNING 44-131-40179





REVISIONS

J2E	
01	C4
02	PFDTØ
03	
04	

J2	
PIN	FUNCTION
01	C4
02	PFDTØ
03	2XLFI
04	
05	
06	
07	GND
08	GND SENSE
09	GND
10	P5U
11	P5U SENSE
12	P5U

J3		
A	B	C
SPARE	P5	P5U

J4M, J4S, J5	
PIN	FUNCTION
01	GND
02	GND
03	GND
04	GND
05	GND
06	GND
07	P5 SENSE
08	CHS. GND
09	GND SENSE
10	P5
11	P5
12	P5
13	P5
14	P5
15	P5

NOTES

1. * INDICATES KEY LOCATION ON J6, J7, J8, AND J9

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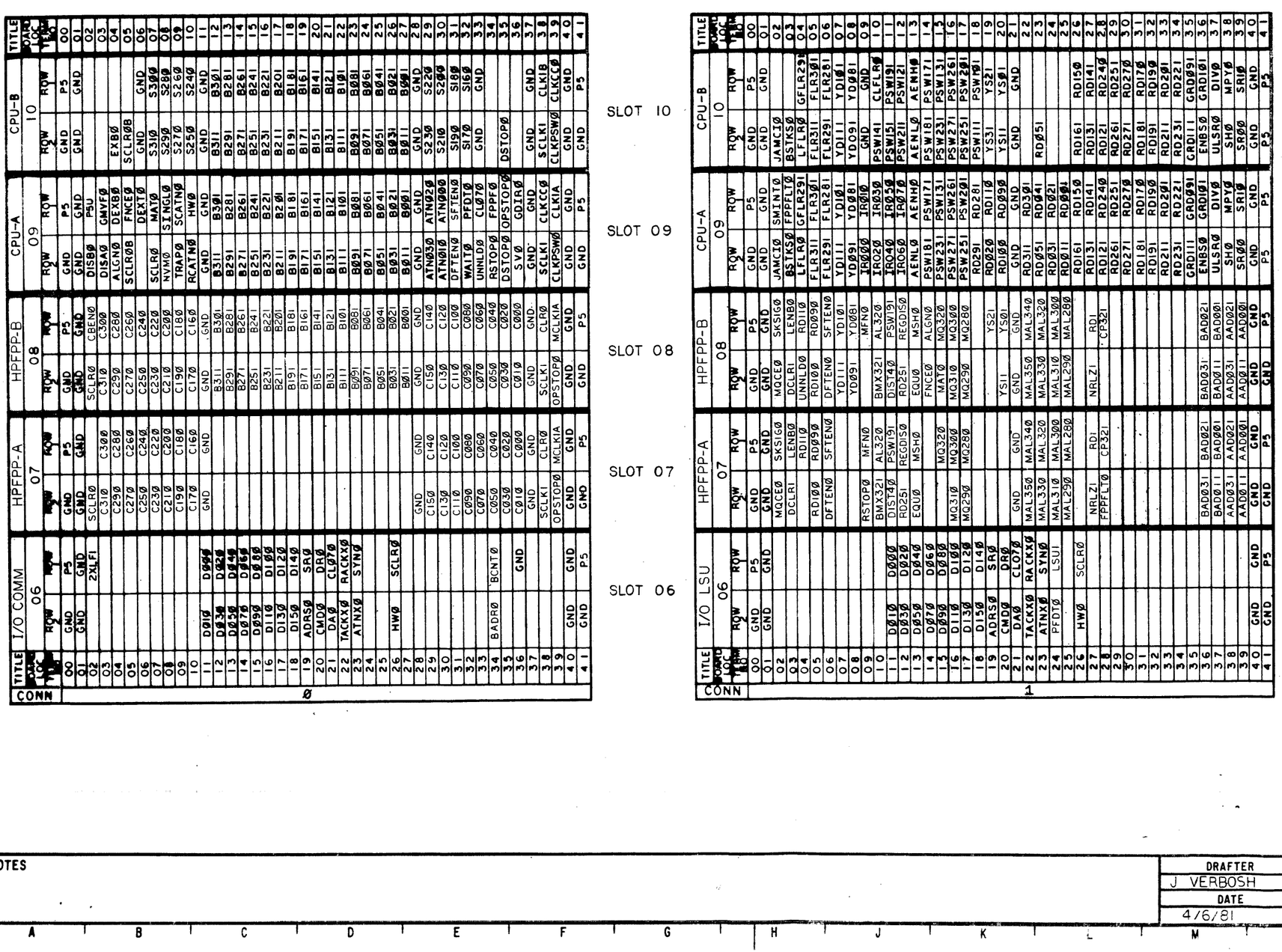
Computer Systems Division
Oceanport, N.J. 07757

TITLE BACKPANEL MAP-DFU W/HPFPP

TASK 03179 | SHT 2-4

DWG 01-197 | D08



REVISIONS

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE DFU
BACKPANEL MAP
W/HPFPP

NOTES

DRAFTER	TASK 03179	SHT
J VERBOSH	DWG 01-197 D08	3 - 4
DATE 4/6/81		

SEE NOTE 1

J1 ROW 1	PIN NO	ROW 2
LSUI	00	GND
SCATNØ	01	GND
RCATNØ	02	GND
PFDTØ	03	GND
SINGLØ	04	GND
P5	05	GND
FAULTØ	06	GND
WAITØ	07	GND
PØFFØ	08	GND
C4	09	GND
P5U	10	KEY
	11	GND
	12	GND

REVISIONS

ADDED MNEMONIC TO: CONN Ø, SLOT 14, ROW 1, PIN 26; CONN 01, SLOT 12, ROW 1, PIN 32 & 09; & SLOT 14, ROW 2, PIN 07.				
JLV	GNF	4915	M	12-10-81	R01 X

SLOT 15

SLOT 14

SLOT 13

SLOT 12

SLOT 11

NOTES

1. * INDICATES KEY LOCATION ON J1

DRAWING 44-131 40579

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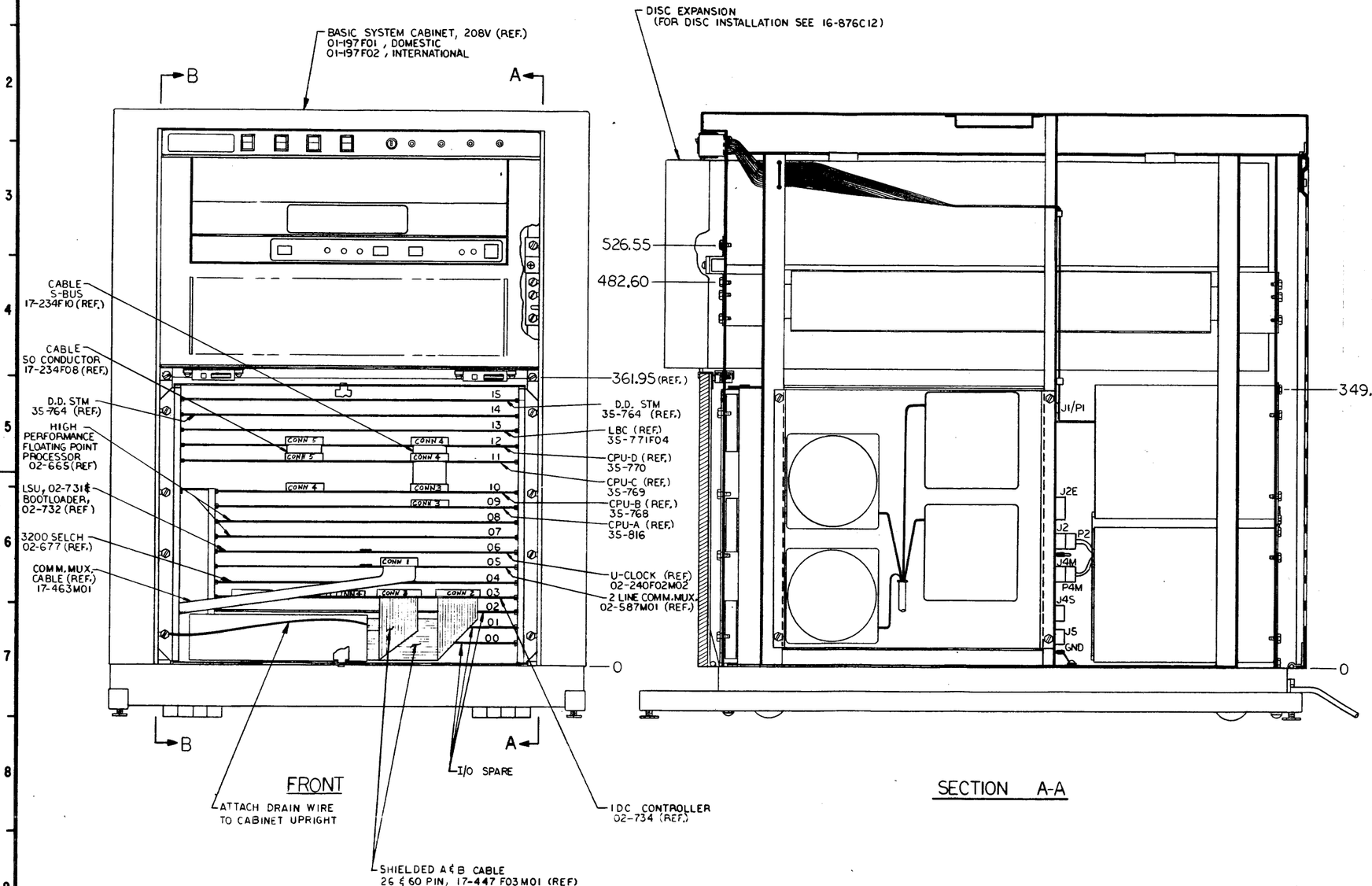
Computer Systems Division
Oceanport, N.J. 07757

TITLE BACKPANEL MAP - DFU W/HPFPP

TASK 03179 | SHT 4 - 4

DWG 01-197 R01 D08

MILLIMETERS	INCHES
526.55	20.75
482.60	19.00
361.95	14.25
349.25	13.75



BASIC CABINET

SHEET NO.	1	2	3
REV. LEVEL	3	1	2
SHEET SIZE	D	D	D

NOTES
1. 35-811BD, TO BE CONFIGURED PER 35-811E03 (CONFIGURATION TABLE)

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	8-25-81
	PROD	9/25/81

IN AREA F6, CPU-A (REF.) WAS 35-798

VT	GJF	4803	R	12-8-81	R01

IN AREA J5, FAN ASS'Y WAS PICTORIALLY SHOWN MOUNTED TO CABINET FROM INSIDE, REVISED SHT. 3

VT	GJF	4913	R	12-8-81	R02	X

RELEASED FOR PRODUCTION
MFG. ENG. MJ & DATE 12/19/81

EXTENSIVE CHANGES MADE: SEE MICROFILM R02: REVISED SHTS 2 & 3:

JAH	JH	5050	R	4-7-82	R03	X

METRIC

USED IN MANUAL 47-022

UNLESS OTHERWISE SPECIFIED

SCALE: ~

TOLERANCE:

DIMENSIONS ARE IN MILLIMETERS	MILLIMETERS	INCHES
	.XX ±.13	.XXX ±.005
	.X ±.5	.XX ±.02
	X ±.8	.X ±.03

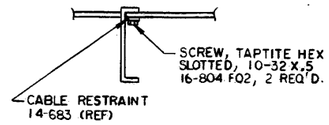
NAME	TITLE	DATE
J. TAMUL	DES/DFT	9-11-81
R. CERO	SUPV	12-18-81
	CHK	
D. FOGGIA	ENG	12-18-81
P. ABITANTE	MGR	12-18-81
R. BARKER	QC	12-17-81

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

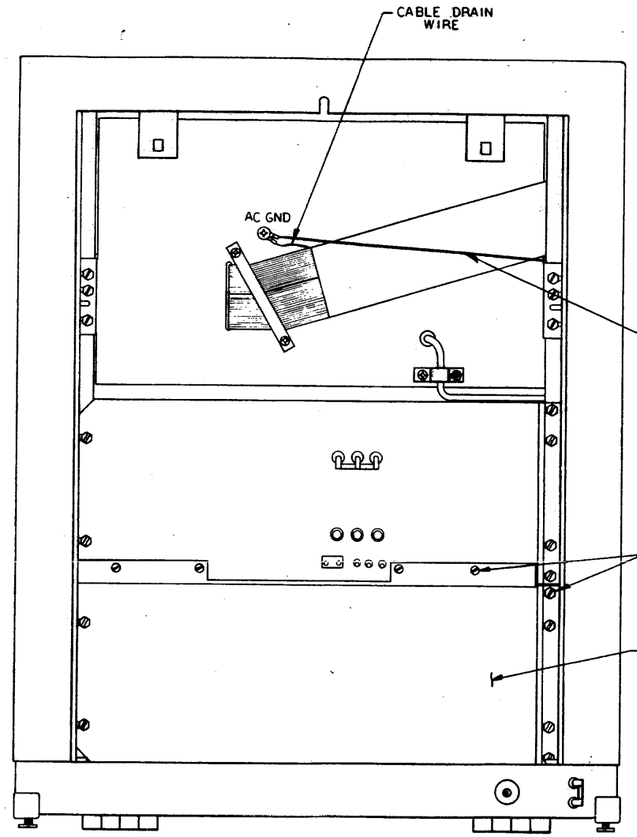
TITLE
INFORMATION DWG.
W/ DFU
MOD 3210, 208V

TASK	03175	SHT
DWG	01-197 R03 D12	1-3

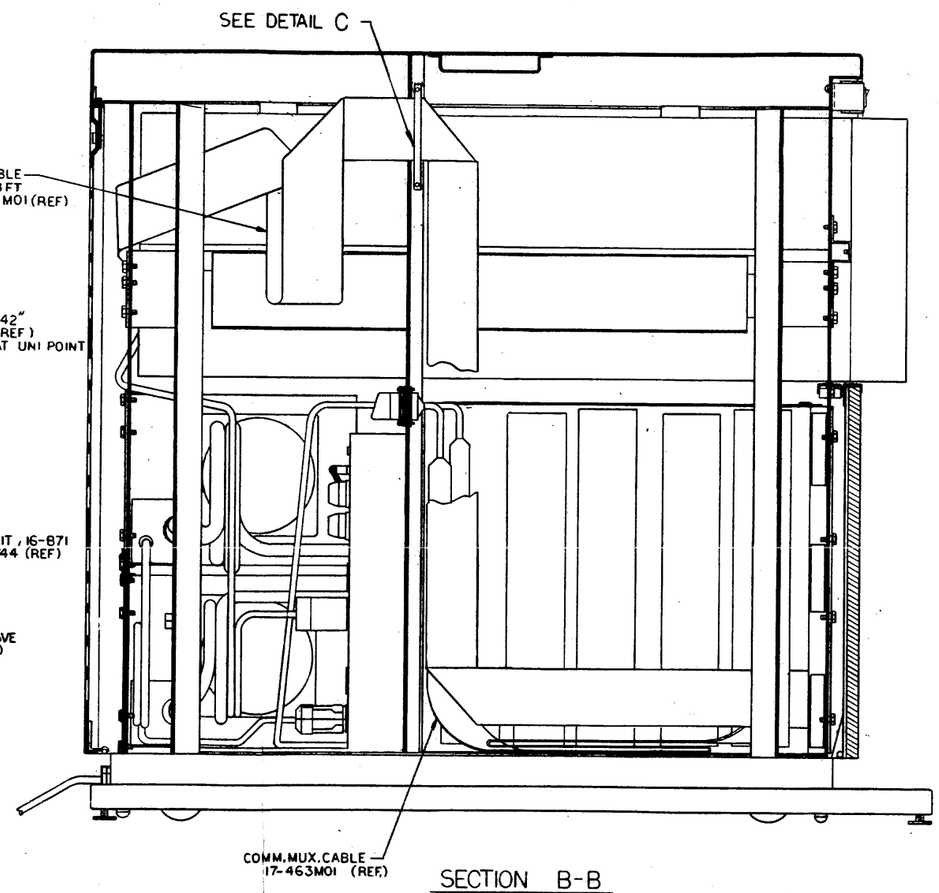
REVISIONS					
EXTENSIVE CHANGES MADE: SEE MICROFILM ROD:					
JAH	JH	5050	R	9-7-82	R01



DETAIL C



REAR



SECTION B-B

BASIC CABINET

NOTES

DRAFTER	J TAMULEVICIUS
DATE	9-11-81

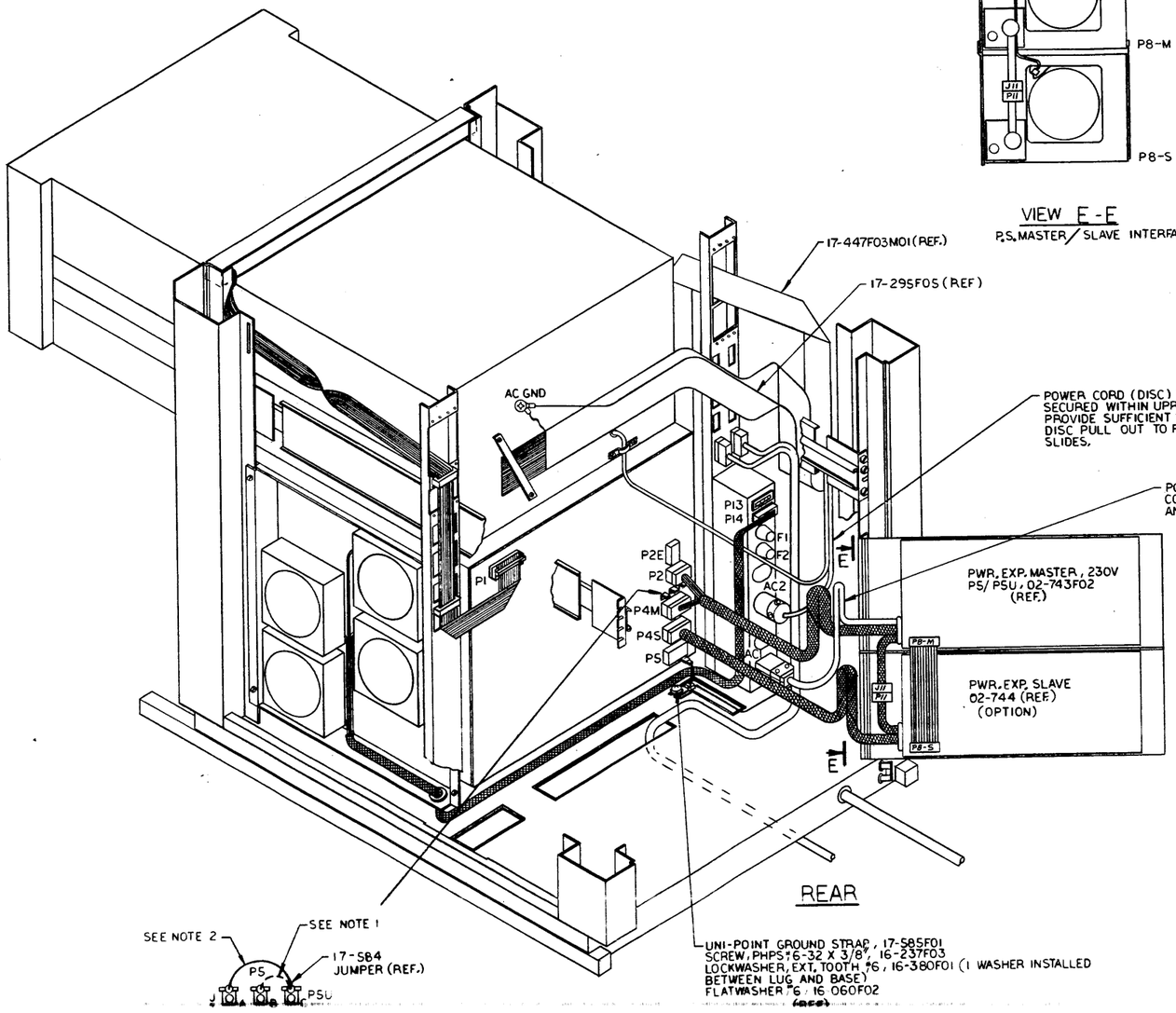
PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE: INFORMATION DWG.
MOD 3210, 208V

TASK 03175		SHT 2-3
DWG 01-197 R01	D12	

REVISIONS						
AREA E6, FAN ASSY WAS PICTORIALLY SHOWN MOUNTED TO CABINET FROM INSIDE.						
VT	CAF	4913	R	12-8-81	R01	X
EXTENSIVE CHANGES MADE: SEE MICRO FILM R01:						
JAH	JJ	5050	R	4-7-82	R02	



REAR

VIEW E-E
P.S. MASTER / SLAVE INTERFACE

BASIC CABINET

NOTES
1. CONNECT B TO C, TO POWER P5U FROM P5 IF P.S. 02-743F01 (P5 ONLY) IS USED.
2. CONNECT A TO C, WHEN P.S. 02 743F02 (P5/P5U) IS USED.

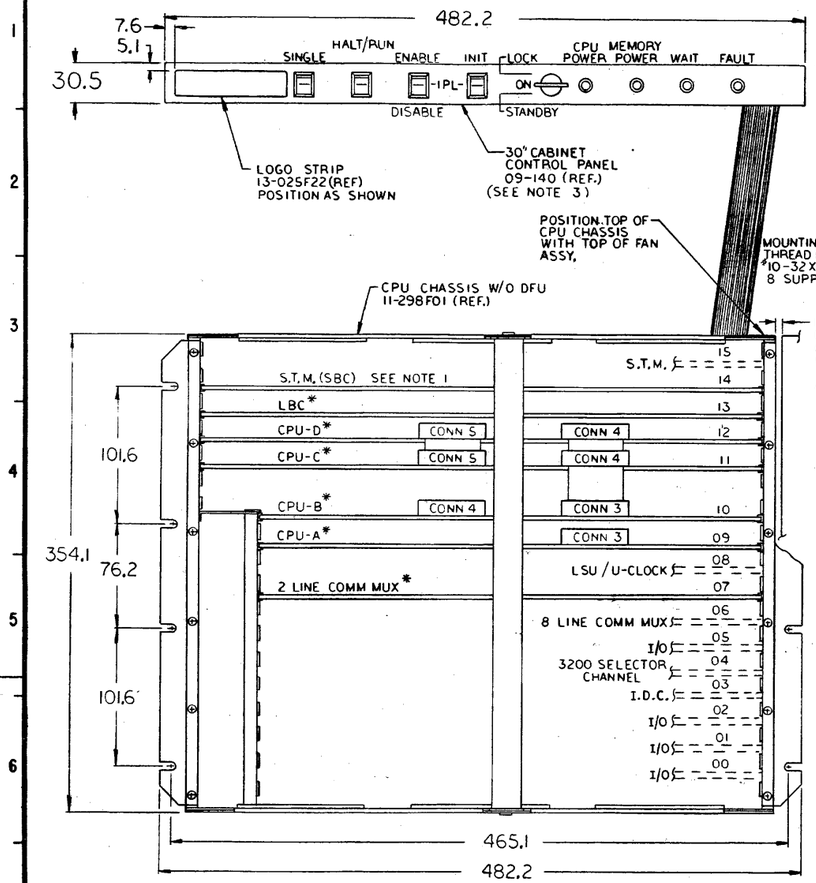
PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

DRAFTER	J TAMULEVICIUS
DATE	9-15-81

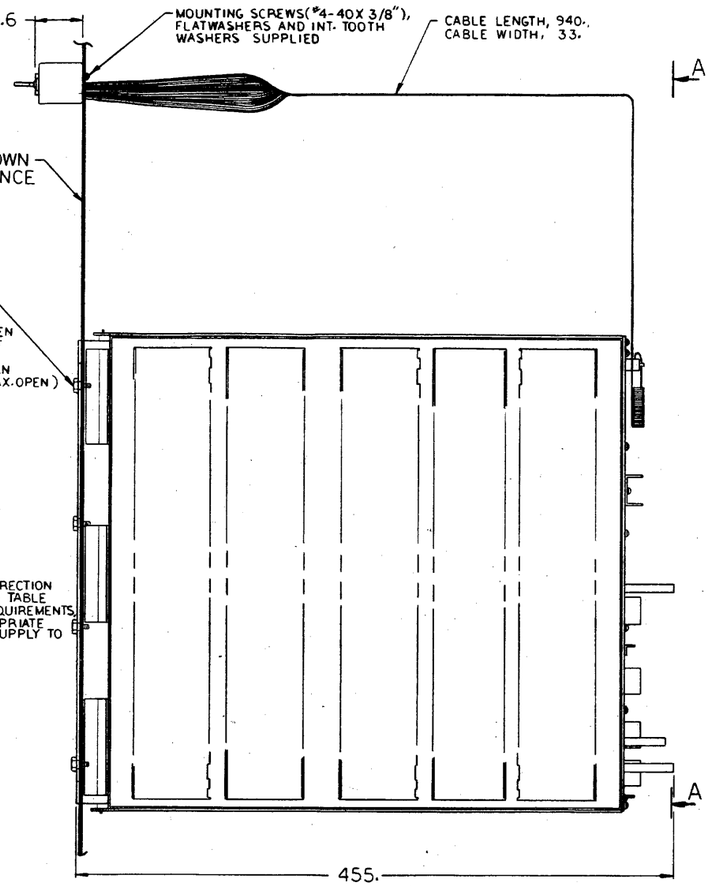
TITLE: INFORMATION DWG. MOD 3210, 208V

TASK 03175 | SHT 3-3

DWG 01-197 R02 D12



FRONT



RIGHT SIDE

33.	1.3
5.1	.20
7.6	.30
4.1	.16
8.9	.35
30.5	1.20
35.6	1.40
76.2	3.00
101.6	4.00
354.1	13.94

482.2	19.00
455.	17.9
340.	37.0
MILLIMETERS	INCHES

SLOT	CUBIC FEET PER MINUTE	CUBIC FEET PER SECOND
	COOLING REQ'D. ACROSS P.C. ASSY (SEE NOTE 2)	
15	2502	5.3
14	2502(STM) 2926(SBC)	5.3(STM) 6.2(SBC)
13	3068	6.5
12	2124	4.5
11	3304	7.0
10	2454	5.2
9	1652	3.5
8	850	1.8
7	850	1.8
6	1652	3.5
5	1652	3.5
4	1652	3.5
3	1652	3.5
2	1652	3.5
1	1652	3.5
0	1652	3.5
	CUBIC FEET PER MINUTE	CUBIC FEET PER SECOND

COOLING REQUIREMENTS

NOTES
1. P.C. ASSEMBLIES NOTED WITH (*) ARE SUPPLIED WITH BASIC CPU CHASSIS. OTHER OPTIONAL P.C. ASSEMBLIES ARE SHOWN FOR REF. LOCATION IN CHASSIS ONLY.
2. THE ABOVE COOLING REQUIREMENTS (SEE TABLE) WILL PROVIDE EXITING AIR TEMPERATURES WITHIN 15°C (59°F) OF INPUT AIR SUPPLY. (FOR PERKIN ELMER COOLING FAN ASSY. SEE 11-295M01 (M32-561)
3. THE SYSTEM CONTROL PANEL SHALL OPERATE AS DEFINED IN 3210 PROCESSOR USERS MANUAL 29-747

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

REVISIONS		
PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	12-18-81
	PROD	12/18/81

RELEASED FOR PRODUCTION
MFG. ENG. MJ DATE 2/19/82

METRIC

USED IN MANUAL 47-022

UNLESS OTHERWISE SPECIFIED		
SCALE: ~	TOLERANCE: MILLIMETERS	INCHES
DIMENSIONS ARE IN MILLIMETERS	.XX ± .13	.XXX ±.005
	.X ± .5	.XX ± .02
	X. ± .8	.X ± .03

NAME	TITLE	DATE
J.TAMUL	DES/DFT	10-2-81
R.CERO	SUPV	2-19-82
	CHK	
R.DENGEL	ENG	2-19-82
P. ABITANTE	MGR	2-19-82
R.BARKER	QC	2-19-82

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

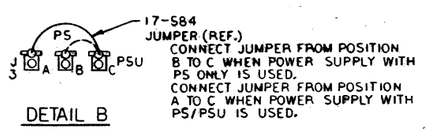
2	1	SHEET NO.
00	00	REV. LEVEL
D	D	SHEET SIZE

TITLE INFORMATION DWG.
BASIC CPU CHASSIS
(W/O DFU CAPABILITY)
(3210/A)

TASK 03131
DWG 02-783 D12
SHT 1-2

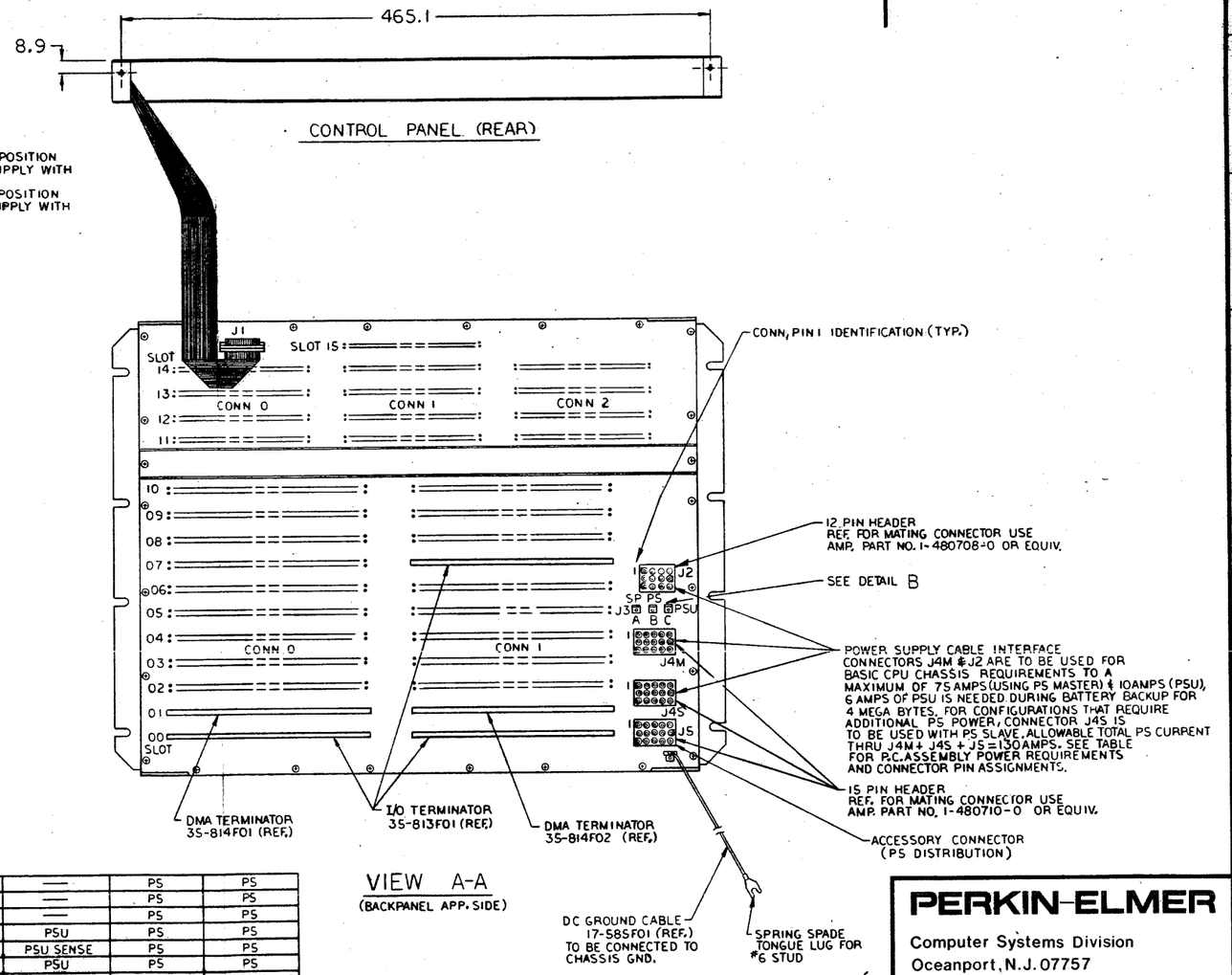
P.C. ASSY. POWER REQUIREMENTS (AMPS)

SLOT NO.	P.C. ASSEMBLY	PS	PSU 256KB	PSU 512KB	PSU 1MB	PSU 2MB	
15	STM	2.2	3.0	3.3	4.2	4.8	NOTE 2
14	STM (SBC)	2.2(15)	1.8 / .6	2.2/ .9	2.0/.9	2.5/1.4	NOTE 3/ NOTE 4
13	LBC	8.0	2.0	2.0	2.0	2.0	
12	CPU-D	7.6					
11	CPU-C	10.6					
10	CPU-B	8.8					
09	CPU-A	5.2					
08	LSU/ U-CLOCK	2.75					
07	2 LINE COMM MUX	2.0					
06	8 LINE COMM MUX	5.0					
05	I/O						
04	3200 SELECTOR CHANNEL	6.0					
03	I.D.C.	6.0					
02	I/O						
01	I/O						
00	I/O						



DETAIL B

17-584 JUMPER (REF.)
CONNECT JUMPER FROM POSITION B TO C WHEN POWER SUPPLY WITH PS ONLY IS USED.
CONNECT JUMPER FROM POSITION A TO C WHEN POWER SUPPLY WITH PS/PSU IS USED.



VIEW A-A
(BACKPANEL APP. SIDE)

PS CONTROL	ON/OFF CONTROL OF PS THROUGH THE KEY SWITCH
OVERTEMPERATURE PROTECTION	PS SHUT DOWN TEMPERATURE 105°C ± 5°C (221°F ± 41°F) PS RESET TEMPERATURE 80°C ± 6°C (176°F ± 42.8°F)
OUTPUT SIGNALS TO THE BACKPANEL FROM DPSC	PFDTØ OUTPUT POWER FAIL DETECT LOGIC LEVELS: 1... OPEN CIRCUIT WITH PULL-UP TO PSU THROUGH 860 OHMS (ON CPU A BOARD) Ø... 1.2 VOLTS MAXIMUM WITH A 10ma CURRENT SINK 2XLF1 TWICE LINE FREQUENCY CLOCK SIGNAL OUTPUT LOGIC LEVELS: 1... APPROXIMATELY 1 MILLISECOND WIDE 5VDC PULSE EVERY 8.3 MILLISECONDS WITH A SOURCE RESISTANCE OF 1 KOHMS Ø... 1 VDC MAXIMUM MAXIMUM LOADING: .. NO MORE THAN 2 STANDARD LINE FREQUENCY CLOCK MODULES OR UNIVERSAL CLOCK MODULES ATTACHED TO THE CPU BACKPANEL
PS & PSU OVERVOLTAGE LIMITING	6.0 VOLTS MAX AT SENSE POINTS
PS & PSU 120 HZ RIPPLE	60 MILLIVOLTS (DC TO 20 MHZ) PEAK TO PEAK MAX (0-50°C) (32-122°F) NO LOAD TO FULL LOAD MEASURED AT SENSE POINTS WITH DIFFERENTIAL PROBE
PS & PSU LOAD, LINE, TEMPERATURE & DYNAMIC LOADING REGULATION	± 5% AT ANY POINT ON BOARD (LOAD)
PSU SENSE POINT LOCATION ON BACKPANEL	CONNECTOR J2
PS SENSE POINT LOCATION ON BACKPANEL	CONNECTOR J4M
VOLTAGE AT SENSE POINTS	5.08 VOLTS ± 10 MILLIVOLTS
REMOTE SENSE POINTS	PROVIDED AT BACKPANEL TO OVERCOME VOLTAGE DROP FROM POWER SUPPLY TO BACKPANEL
REQUIREMENT	DESCRIPTION

CHASSIS POWER REQUIREMENTS

PIN NO	J2 (12 PIN)	J4M (15 PIN)	J4S (15 PIN)
	BACKPANEL CONNECTOR (P.C. HEADER)		
15	—	PS	PS
14	—	PS	PS
13	—	PS	PS
12	PSU	PS	PS
11	PSU SENSE	PS	PS
10	PSU	PS	PS
09	PSU GND	PS SENSE GND	PS SENSE GND
08	PSU SENSE GND	CHS GND	CHS GND
07	PSU GND	PS SENSE	PS SENSE
06		PS GND	PS GND
05		PS GND	PS GND
04	FFLTØ	PS GND	PS GND
03	2XLF1	PS GND	PS GND
02	PFDTØ	PS GND	PS GND
01	KSONØ	PS GND	PS GND

CONN. PIN ASSIGNMENT

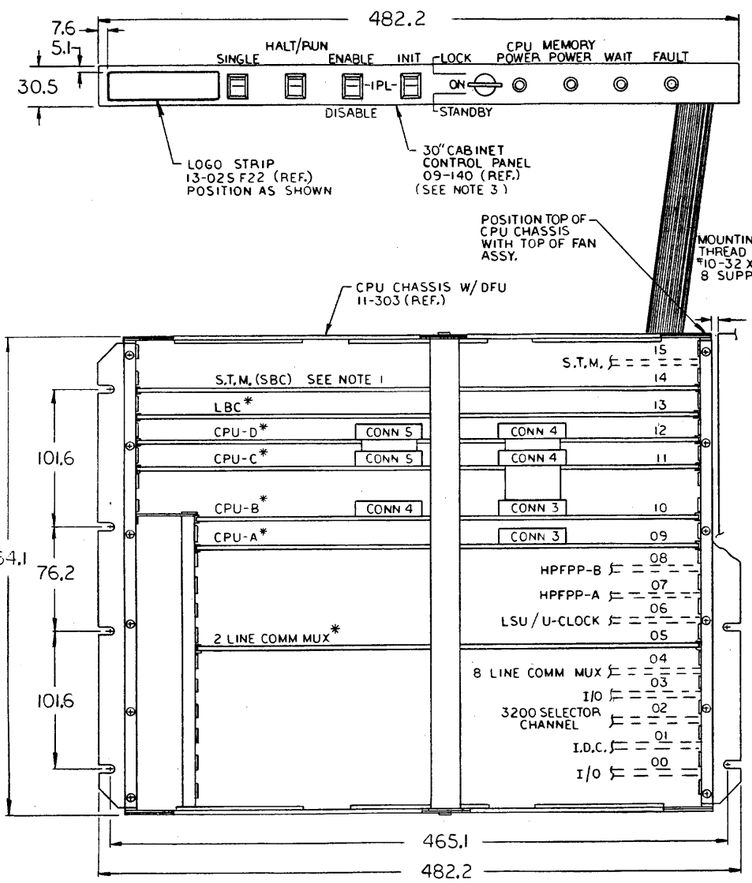
NOTES
1. FOR ADDITIONAL POWER REQUIREMENT INFORMATION SEE 47-020 (REF.) SEE 02-743F01 (M32-540) FOR PERKIN ELMER POWER CONDITIONER
2. VALUES SHOWN ARE PER ACTIVE MODE (MEMORY MODULE IS ACCESSED EVERY 1.2 μ SEC.) ONLY ONE MEMORY MODULE MAY BE ACTIVE.
3. VALUES SHOWN ARE PER STAND-BY MODE (MEMORY MODULE IS NOT ACCESSED).
4. VALUES SHOWN ARE BATTERY BACKUP DRAIN.

REVISIONS

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE INFORMATION DWG.
BASIC CPU CHASSIS

DRAFTER	TASK 03131	SHT
J TAMULEVICIUS	DWG 02-783 D12	2-2
DATE 10-2-81		



33.	1.3
5.1	.20
7.6	.30
4.1	.16
8.9	.35
30.5	1.20
35.6	1.40
76.2	3.00
101.6	4.00
~~354.1~~	~~13.94~~
465.1	18.31
482.2	19.00
455.	17.9
940.	37.0
MILLIMETERS	INCHES

SLOT	CENTIMETERS PER SECOND	FEET PER MINUTE
	COOLING REQ'D. ACROSS P.C. ASSY (SEE NOTE 2)	
15	2502	5.3
14	2502 (STM) 2926 (SBC)	5.3 (STM) 6.2 (SBC)
13	3068	6.5
12	2124	4.5
11	3304	7.0
10	2454	5.2
9	1652	3.5
8	2785	5.9
7	2785	5.9
6	850	1.8
5	850	1.8
4	1652	3.5
3	1652	3.5
2	1652	3.5
1	1652	3.5
0	1652	3.5

COOLING REQUIREMENTS

NOTES

1. P.C. ASSEMBLIES NOTED WITH (*) ARE SUPPLIED WITH BASIC CPU CHASSIS. OTHER OPTIONAL P.C. ASSEMBLIES ARE SHOWN FOR REF. LOCATION IN CHASSIS ONLY.
2. THE ABOVE COOLING REQUIREMENTS (SEE TABLE) WILL PROVIDE EXITING AIR TEMPERATURES WITHIN 15°C (59°F) OF INPUT AIR SUPPLY. (FOR PERKIN ELMER COOLING FAN ASSY. SEE 11-295 MOI (M32-561)
3. THE SYSTEM CONTROL PANEL SHALL OPERATE AS DEFINED IN 3210 PROCESSOR USERS MANUAL 29-747

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

REVISIONS		
	INIT	DATE
PRE PRODUCTION APPROVAL		
DEV	[illegible]	12-18-81
PROD	MJD	12/18/81

RELEASED FOR PRODUCTION

MFG. ENG. [illegible] DATE 2/19/82

METRIC

USED IN MANUAL 47-022

UNLESS OTHERWISE SPECIFIED		
SCALE: ~	TOLERANCE: MILLIMETERS	INCHES
DIMENSIONS ARE IN MILLIMETERS	.XX ± .13 .X ± .5 X. ± .8	.XXX ±.005 .XX ± .02 .X ± .03

NAME	TITLE	DATE
J.TAMUL	DES/DFT	10-2-81
R.CERO	SUPV	2-19-82
	CHK	
R.DENGEL	ENG	2-19-82
P.ABITANTE	MGR	2-19-82
R.BARKER	QC	2-19-82

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

12	SHEET NO.
00	REV. LEVEL
D	SHEET SIZE

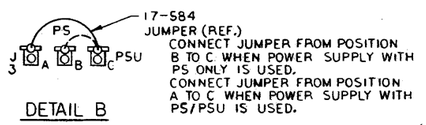
TITLE INFORMATION DWG.
BASIC CPU CHASSIS
(W/DFU CAPABILITY)
(3210/A)

TASK	SHT
03131	
DWG 02-784 D12	1-2

HRINING 44-131 40579

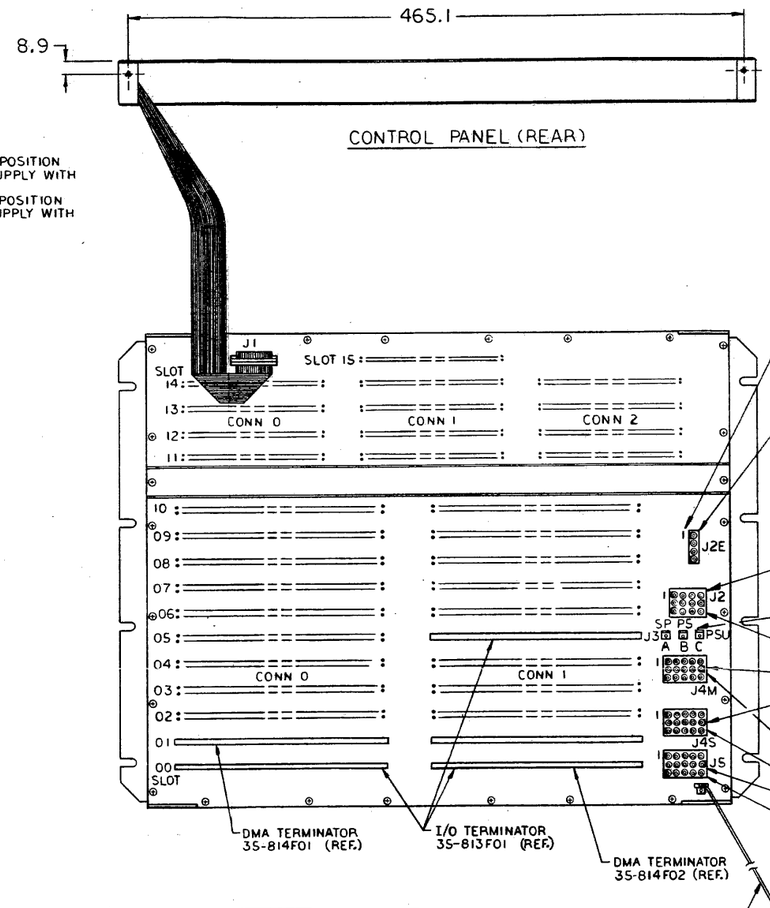
P.C. ASSY. POWER REQUIREMENTS (AMPS)

SLOT NO.	P.C. ASSEMBLY	PS	PSU 256KB	PSU 512 KB	PSU 1MB	PSU 2MB	
15	STM	2.2	3.0	3.3	4.2	4.8	NOTE 2
14	STM (SBC)	2.2(1S)	1.8/.6	2.2/.9	2.0/.9	2.5/1.4	NOTE 3 / NOTE 4
13	LBC	8.0	2.0	2.0	2.0	2.0	
12	CPU-D	7.6					
11	CPU-C	10.6					
10	CPU-B	8.8					
09	CPU-A	5.2					
08	HPFPP-B	21.0					
07	HPFPP-A						
06	LSU/U-CLOCK	2.7S					
05	2 LINE COMM MUX	2.0					
04	8 LINE COMM MUX	5.0					
03	I/O						
02	3200 SELECTOR CHANNEL	6.0					
01	I.D.C.	6.0					
00	I/O						



DETAIL B

17-584 JUMPER (REF.)
CONNECT JUMPER FROM POSITION B TO C WHEN POWER SUPPLY WITH PS ONLY IS USED.
CONNECT JUMPER FROM POSITION A TO C WHEN POWER SUPPLY WITH PS/PSU IS USED.



VIEW A-A
(BACKPANEL APP. SIDE)

PS CONTROL	ON/OFF CONTROL OF PS THROUGH THE KEY SWITCH
OVERTEMPERATURE PROTECTION	PS SHUT DOWN TEMPERATURE 105°C ± 5°C (221°F ± 41°F) PS RESET TEMPERATURE 80°C ± 6°C (176°F ± 42.8°F)
OUTPUT SIGNALS TO THE BACKPANEL FROM DPSC	PFDTØ OUTPUT POWER FAIL DETECT LOGIC LEVELS: 1... OPEN CIRCUIT WITH PULL-UP TO PSU THROUGH 860 OHMS (ON CPU A BOARD) Ø... 1.2 VOLTS MAXIMUM WITH A 10mA CURRENT SINK 2XLF1 TWICE LINE FREQUENCY CLOCK SIGNAL OUTPUT LOGIC LEVELS: 1... APPROXIMATELY 1 MILLISECOND WIDE 5VDC PULSE EVERY 8.3 MILLISECONDS WITH A SOURCE RESISTANCE OF 1 KOHMS Ø... 1VDC MAXIMUM MAXIMUM LOADING: .. NO MORE THAN 2 STANDARD LINE FREQUENCY CLOCK MODULES OR UNIVERSAL CLOCK MODULES ATTACHED TO THE CPU BACKPANEL
PS & PSU OVERVOLTAGE LIMITING	6.0 VOLTS MAX AT SENSE POINTS
PS & PSU 120 HZ RIPPLE	60 MILLIVOLTS (DC TO 20 MHZ) PEAK TO PEAK MAX (0-50°C)(32-122°F) NO LOAD TO FULL LOAD MEASURED AT SENSE POINTS WITH DIFFERENTIAL PROBE
PS & PSU LOAD, LINE, TEMPERATURE & DYNAMIC LOADING REGULATION	± 5% AT ANY POINT ON BOARD (LOAD)
PSU SENSE POINT LOCATION ON BACKPANEL	CONNECTOR J2
PS SENSE POINT LOCATION ON BACKPANEL	CENTER OF SLOT 9 ON APP. SIDE
VOLTAGE AT SENSE POINTS	5.08 VOLTS ± 10 MILLIVOLTS
REMOTE SENSE POINTS	PROVIDED AT BACKPANEL TO OVERCOME VOLTAGE DROP FROM POWER SUPPLY TO BACKPANEL
REQUIREMENT	DESCRIPTION

CHASSIS POWER REQUIREMENTS

PIN NO	J2 (12 PIN)	J4M (15 PIN)	J4S (15 PIN)
	BACKPANEL CONNECTOR (P.C. HEADER)		
15	—	PS	PS
14	—	PS	PS
13	—	PS	PS
12	PSU	PS	PS
11	PSU SENSE	PS	PS
10	PSU	PS	PS
09	PSU GND	PS SENSE GND	PS SENSE GND
08	PSU SENSE GND	CHS GND	CHS GND
07	PSU GND	PS SENSE	PS SENSE
06		PS GND	PS GND
05		PS GND	PS GND
04	FFLTØ	PS GND	PS GND
03	2XLF1	PS GND	PS GND
02	PFDTØ	PS GND	PS GND
01	KSONØ	PS GND	PS GND

CONN. PIN ASSIGNMENT

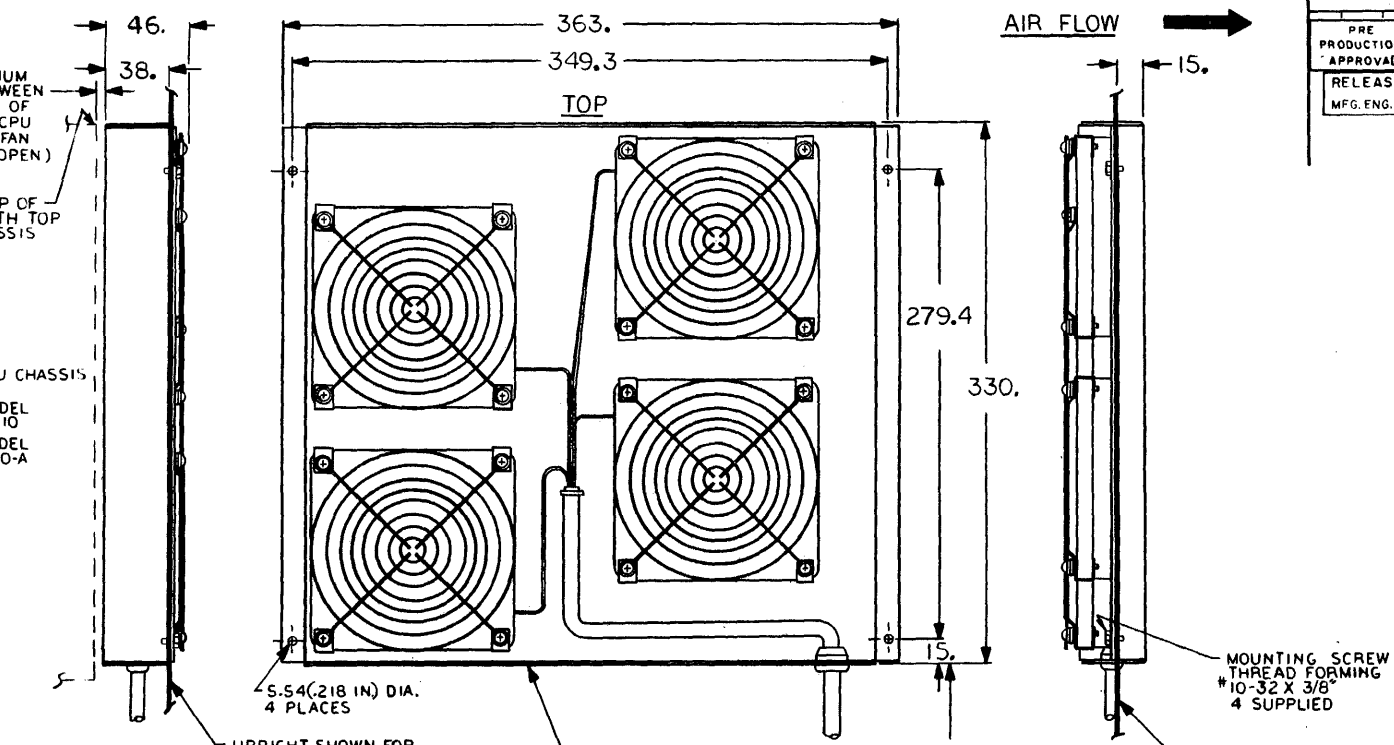
NOTES
1. FOR ADDITIONAL POWER REQUIREMENT INFORMATION SEE 47-020 (REF.) SEE 02-743F01 (M32-540) FOR PERKIN ELMER POWER CONDITIONER
2. VALUES SHOWN ARE PER ACTIVE MODE (MEMORY MODULE IS ACCESSED EVERY 1.2 μSEC). ONLY ONE MEMORY MODULE MAY BE ACTIVE.
3. VALUES SHOWN ARE PER STAND-BY MODE (MEMORY MODULE IS NOT ACCESSED).
4. VALUES SHOWN ARE BATTERY BACKUP DRAIN.

REVISIONS

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE INFORMATION DWG.
BASIC CPU CHASSIS

DRAFTER: J TAMULEVICIUS
DATE: 10-2-81
TASK 03131
DWG 02-784 D12
SHT 2-2



4.1	16
15.	.6
38.	1.5
46.	1.8
279.4	11.00
330.	13.0
349.3	13.75
363.	14.3
MILLIMETERS	INCHES

CURRENT	.24A/FAN
SPEED	2600 RPM / 2950 RPM
AIR FLOW	SEE PERF. CURVE
FREQUENCY	50/60 HZ
VOLTAGE	117 VOLTS
FAN SPECIFICATIONS	

NOTES

REVISIONS			
		INIT	DATE
PRE PRODUCTION APPROVAL	DEV	[illegible]	12-18-81
	PROD	[illegible]	12/18/81
RELEASED FOR PRODUCTION MFG. ENG. [illegible] INIT DATE 1/27/82			

USED IN MANUAL 47-022

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

UNLESS OTHERWISE SPECIFIED			
SCALE: ~	MILLIMETERS	TOL	INCHES
DIMENSIONS ARE IN MILLIMETERS	.XX ± .13 .X ± .5 .X ± .8		.XXX ± .005 .XX ± .02 .X ± .03

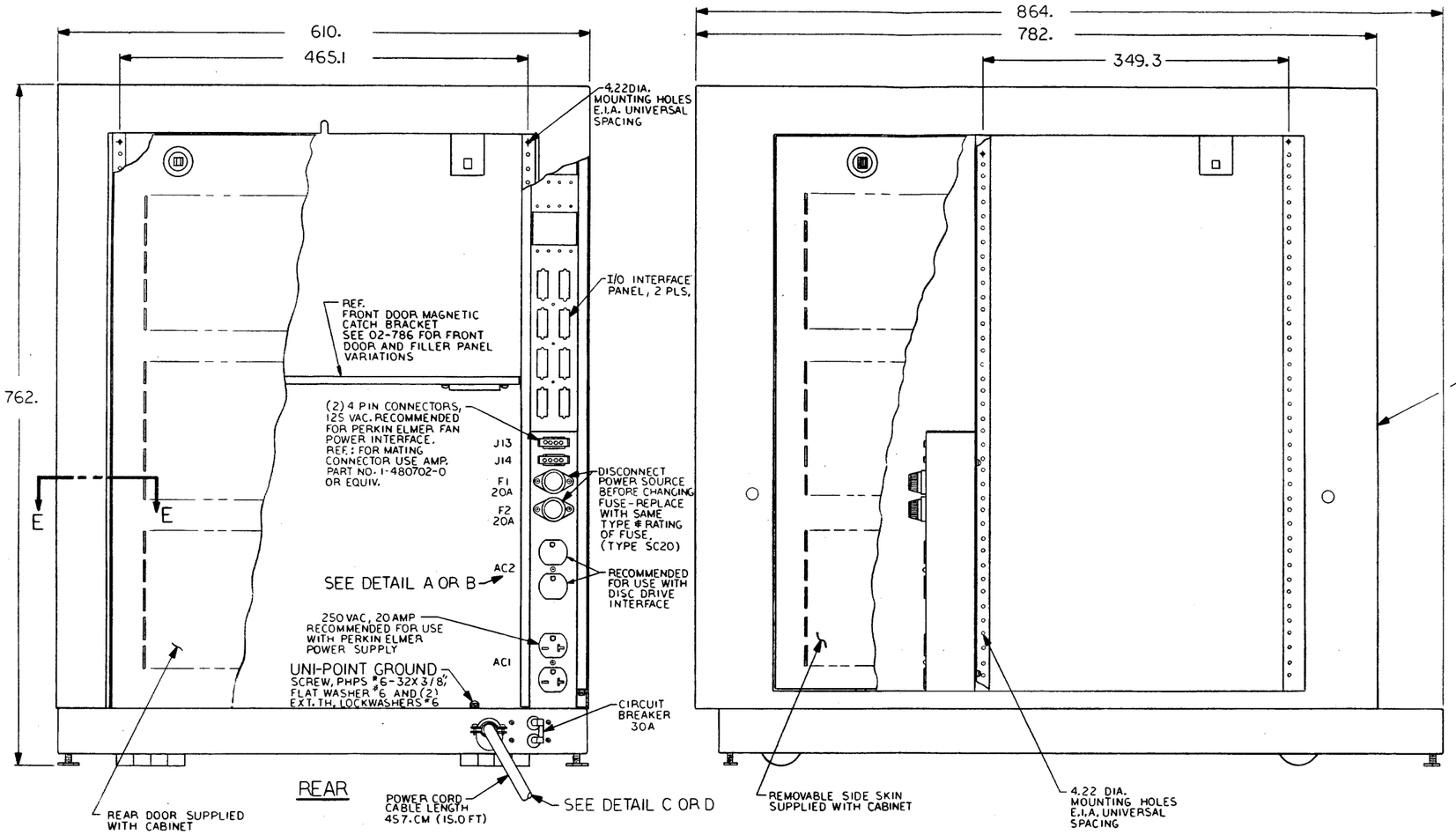
NAME	TITLE	DATE
J TAMUL	DES / DFT	10-8-81
R CERO	SUPV	1-27-82
	CHK	
R DENGEL	ENG	1-27-82
P ABITANTE	MGR	1-27-82
R BARKER	QC	1-27-82

TITLE 3210, 3210/A INFORMATION DWG. FAN ASSEMBLY

TASK 03131 SHT 1-1

DWG 11-295M01 C12

BRUNING 44-131 40579



DETAIL A
(DOMESTIC)
125VAC
20AMP

DETAIL B
(INTERNATIONAL)
250VAC
20AMP

DETAIL C
(DOMESTIC)
PLUG EQUIPPED IS HUBBEL #2711 OR EQUIV. (REF.) FOR APPLICATIONS POWERED BY A 120/208VAC, 60 HZ 3 POLE 4 WIRE GROUNDING SOURCE

DETAIL D
(INTERNATIONAL)
PLUG EQUIPPED IS HUBBEL #4511S OR EQUIV. (REF.) FOR APPLICATIONS POWERED BY A 200 TO 240 VAC, 50 HZ 2 POLE 3 WIRE GROUNDING SOURCE

SECTION E-E

WHEN BOLTING CABINETS TOGETHER; REMOVE APPROPRIATE HOLE PLUGS AND SIDE SKINS, BOLT TOGETHER WITH:
1 EA, 5/16-18 X 3/4" HEX HEAD BOLT, 16-410F01
2 EA, 5/16 EXTERNAL TOOTH LOCKWASHER, 16-380F05
1 EA, 5/16-18 HEX NUT, 16-058F05

4.22	.174
349.3	13.75
465.1	18.31
~~610~~	~~24.0~~
762.	30.0
782.	30.8
864.	34.0
MILLIMETERS	INCHES

02-788 F01	DOMESTIC, 208V, 60 Hz (DETAILS A & C)
PART NO	DESCRIPTION
VARIATION TABLE	

NOTES 1 FOR SCHEMATIC INFO SEE DWG. 11-296C08

REVISIONS		
PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	
	PROD MJS	12/18/81

RELEASED FOR PRODUCTION
MFG. ENG. MJS DATE 2/9/82

METRIC

USED IN MANUAL 47-022

UNLESS OTHERWISE SPECIFIED		
SCALE: 3/8	TOLERANCE: MILLIMETERS	INCHES
DIMENSIONS ARE IN MILLIMETERS	.XX ± .13 .X ± .5 X ± .8	.XXX ± .005 .XX ± .02 .X ± .03

NAME	TITLE	DATE
J. TAMUL	DES/DFT	10-14-81
R. CERO	SUPV	2-19-82
	CHK	
R. DENGEL	ENG	2-19-82
P. ABITANTE	MGR	2-19-82
R. BARKER	QC	2-19-82

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

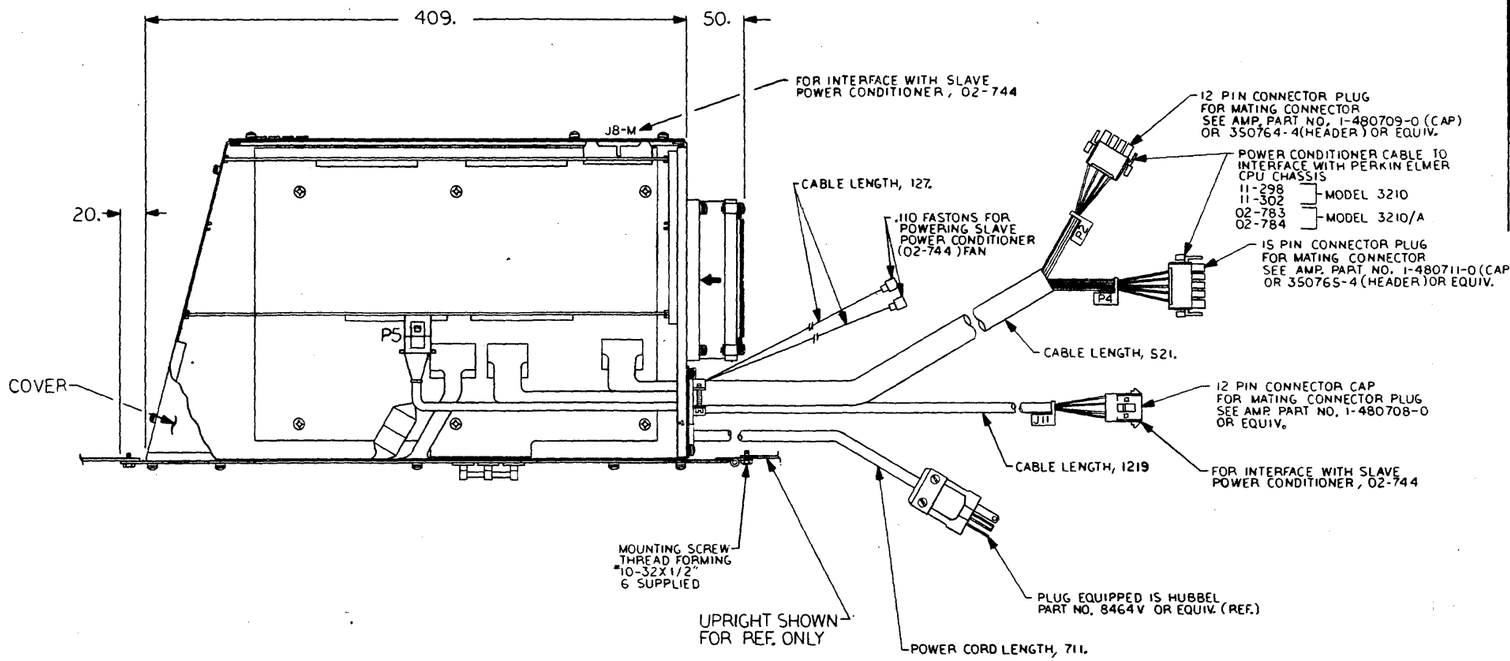
TITLE INFORMATION DWG. 30" CABINET (W/O FRONT DOOR AND FILLER PANEL) (3210/A)

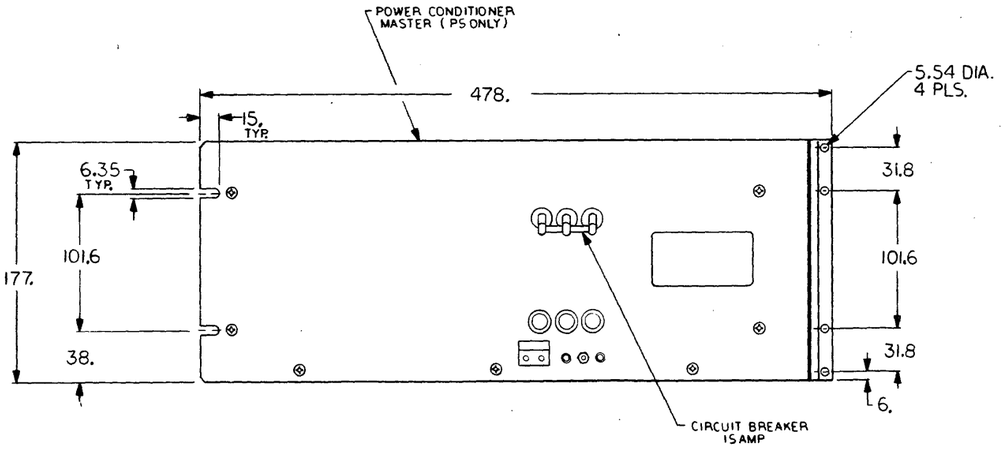
TASK 03131 | SHT 1-1

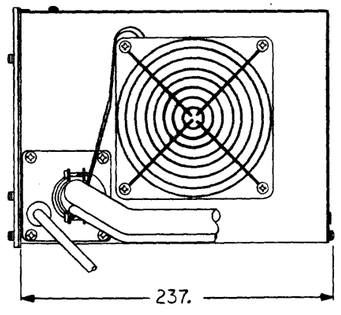
DWG 02-788 D12

I/RUNING 44-131 4579

MILLIMETERS	INCHES
478.	18.8
409.	16.1
237.	9.3
177.	7.0
101.6	4.00
50.	1.7
38.	1.5
31.8	1.25
20.	.8
15.	.6
6.35	.250
6.	.2
5.54	.218
1219	48.0
521.	20.5
127.	5.0
114.	4.5







02-743F01
SEE NOTE 1

NOTES 1. FOR PSU EXPANSION (BATT. BACKUP) SEE DWG. 02-745D12

REVISIONS

RELEASED FOR PRODUCTION
MFG. ENG. JMJ DATE 12/18/81
IN MILLIMETER CHART, 1219. WAS 711.; 48.0 WAS 28.0:
JAH | AJ | 4985 | R | 4-28-82 | R01 | X

USED IN MANUAL 47-020

UNLESS OTHERWISE SPECIFIED		
SCALE: ~	TOLERANCE: MILLIMETERS	INCHES
DIMENSIONS ARE IN MILLIMETERS	.XX ± .13	.XXX ± .005
	.X ± .5	.XX ± .02
	X. ± .8	.X ± .03

NAME		TITLE	DATE
J. TAMUL		DES / DFT	10-20-81
R. CERO		SUPV	12-8-81
		CHK	
R. DENGEL		ENG	12-8-81
P. ABITANTE		MGR	12-8-81
R. BARKER		QC	12-7-81

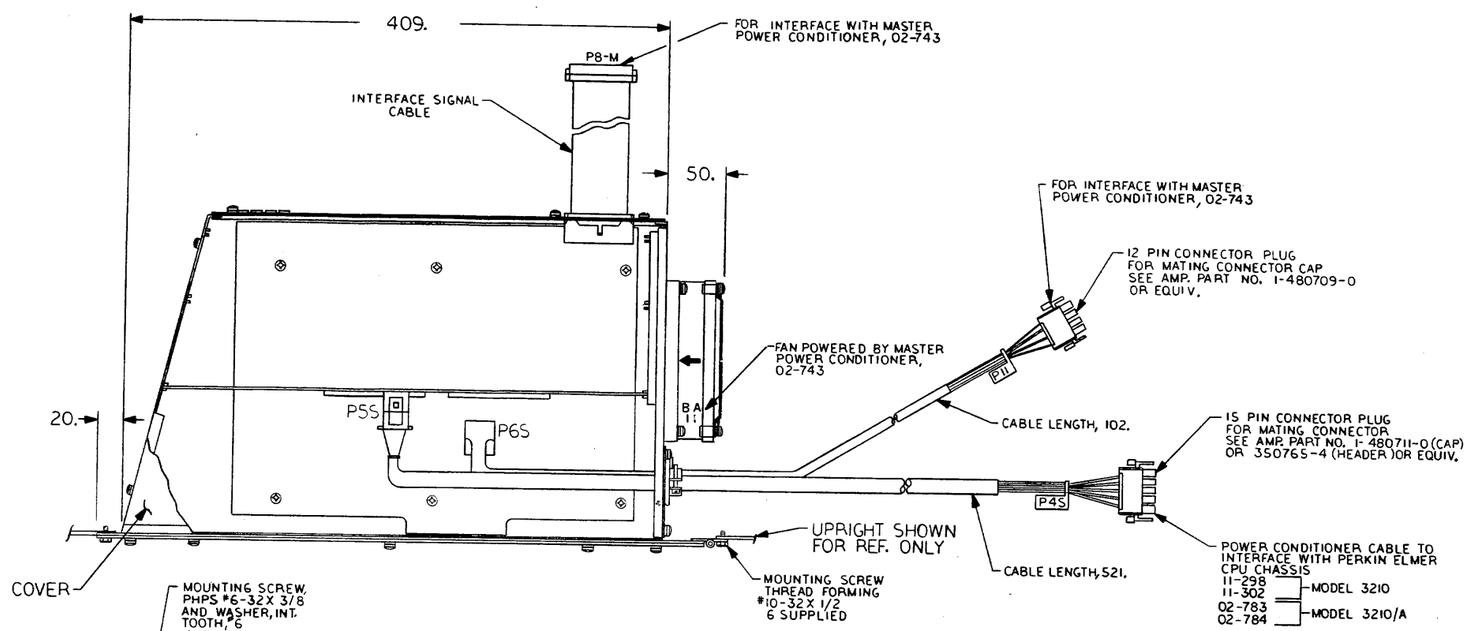
PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

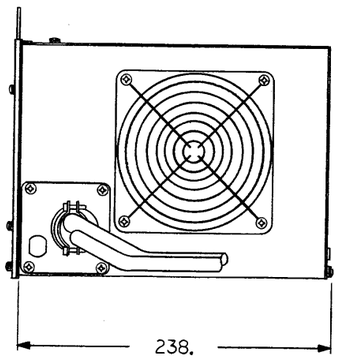
METRIC

TITLE INFORMATION DWG. POWER CONDITIONER, MASTER (P5 ONLY.) (3210, 3210/A)

TASK 03131 | SHT 1-1
DWG 02-743 R01 D12

MILLIMETERS	INCHES
478.	18.0
409.	16.1
238.	9.3
201.	7.9
101.6	4.00
50.	1.7
38.	1.5
31.8	1.25
20.	.8
15.	.6
6.35	.250
.6	.2
5.54	.218
521.	20.5
102.	4.0





REVISIONS

RELEASED FOR PRODUCTION
MFG. ENG. _____ DATE 12/18/81

METRIC

USED IN MANUAL 47-020

UNLESS OTHERWISE SPECIFIED

SCALE: 1/2

TOLERANCE:

DIMENSIONS ARE IN MILLIMETERS	MILLIMETERS	INCHES
	.XX ± .13	.XXX ± .005
	.X ± .5	.XX ± .02
	X. ± .8	.X ± .03

NAME	TITLE	DATE
J.TAMUL	DES/DFT	10-21-81
R.CERO	SUPV	12-8-81
	CHK	
R.DENGEL	ENG	12-8-81
P.ABITANTE	MGR	12-8-81
R.BARKER	QC	12-7-81

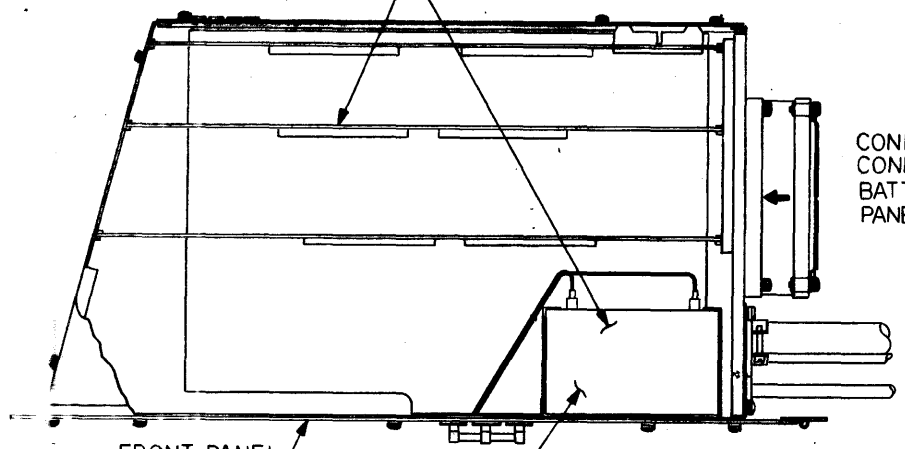
PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

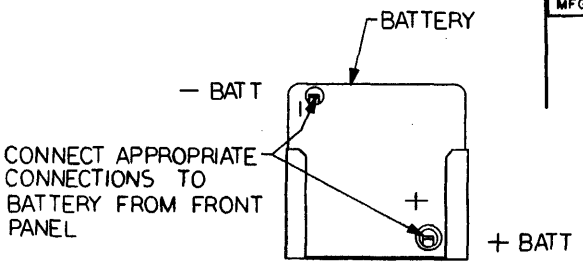
TITLE: INFORMATION DWG. POWER CONDITIONER SLAVE (3210, 3210/A)

TASK 03131 | SHT 1-1
DWG 02-744 D12

NOTES

BUSHING 44131-40579





DETAIL "A"
INSTALL BATTERY AS SHOWN

REVISIONS
RELEASED FOR PRODUCTION MFG. ENG. MJQ DATE 12/18/81

USED IN MANUAL 47-020

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

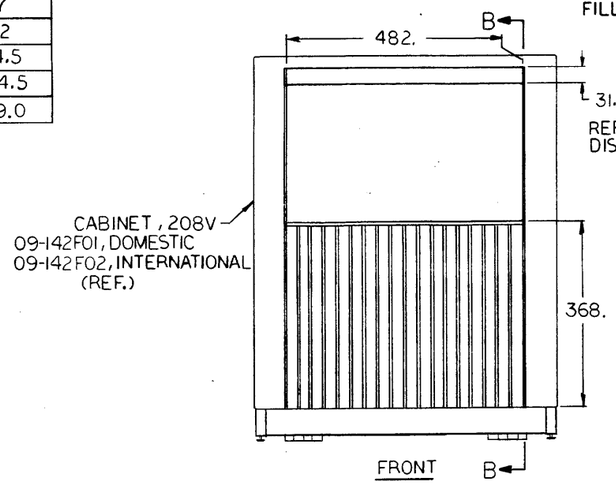
UNLESS OTHERWISE SPECIFIED			
SCALE: 1/2	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ± .005 .X ± .03 .XX ± .02 ANGLES ± 1°		
NAME		TITLE	DATE
J TAMUL		DES / DFT	10-21-81
R CERO		SUPV	12-8-81
		CHK	
R DENGEL		ENG	12-8-81
P ABITANTE		MGR	12-8-81
R BARKER		QC	12-7-81

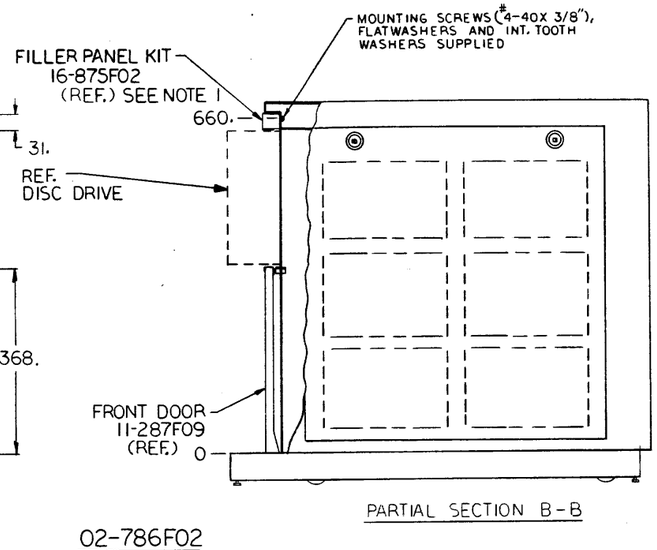
TITLE 3210/A
INFORMATION DWG.
P5U EXPANSION

TASK 03131 SHT 1-1
DWG 02-745 C12

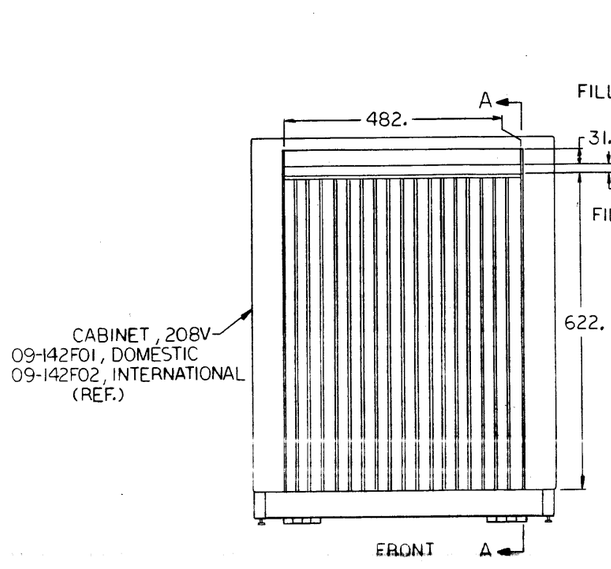
NOTES
1. FOR MEMORY MODULE INFO SEE CPU CHASSIS DWG. 02-783[illegible]12 AND 02-784D12.

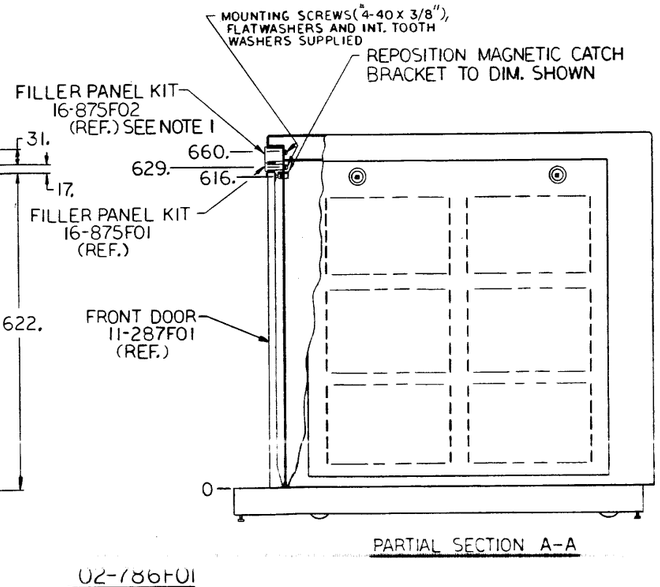
MILLIMETERS	INCHES
616.	24.3
629.	24.8
660.	26.0
17.	.7
31.	1.2
368.	14.5
622.	24.5
482.	19.0





02-786F02
FRONT DOOR & FILLER PANEL
(FOR SINGLE DISC)





02-786F01
FULL FRONT DOOR & FILLER PANELS
(FOR CPU CHASSIS &/OR I/O CHASSIS)

NOTES 1. WHEN PROCESSOR (CPU) CHASSIS IS INSTALLED IN CABINET, FILLER PANEL KIT 16-875F02 IS REPLACED BY CONTROL PANEL SUPPLIED WITH CHASSIS (SEE 02-783 & 02-784)

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

REVISIONS		
PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	
	PROD	12/18/81

RELEASED FOR PRODUCTION
MFG. ENG. _____ DATE 2/19/82

METRIC

USED IN MANUAL 47-022

UNLESS OTHERWISE SPECIFIED		
SCALE: ~	TOLERANCE: MILLIMETERS	INCHES
DIMENSIONS ARE IN MILLIMETERS	.XX ± .13	.XXX ± .005
	.X ± .5	.XX ± .02
	X. ± .8	.X ± .03

NAME		TITLE	DATE
J. TAMUL		DES/DFT	10-14-81
R. CERO		SUPV	2-19-82
		CHK	
R. DENGEL		ENG	2-19-82
P. ABITANTE		MGR	2-19-82
R. BARKER		QC	2-19-82

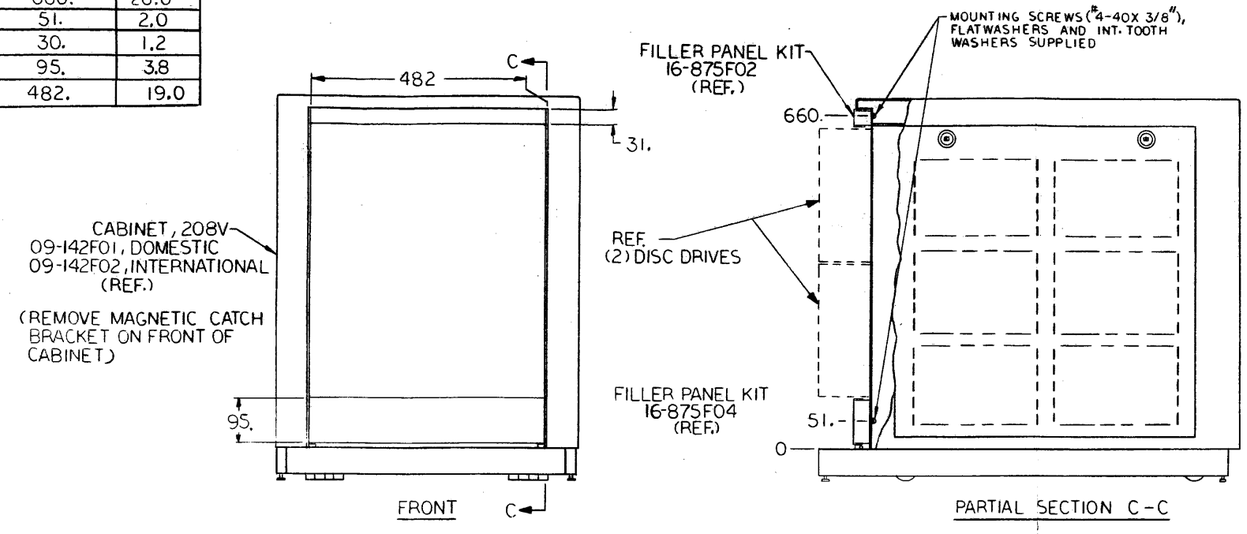
PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

12	SHEET NO
00 00	REV LEVEL
D D	SHEET SIZE

TITLE INFORMATION DWG.
FRONT DOOR AND FILLER PANEL
OR FILLER PANELS
30" CABINET (3210/A)

TASK 03131	SHT 1-2
DWG 02-786 D12	

MILLIMETERS	INCHES
660.	26.0
51.	2.0
30.	1.2
95.	3.8
482.	19.0



02-786F03
FILLER PANELS
(FOR DOUBLE DISC)

REVISIONS

NOTES

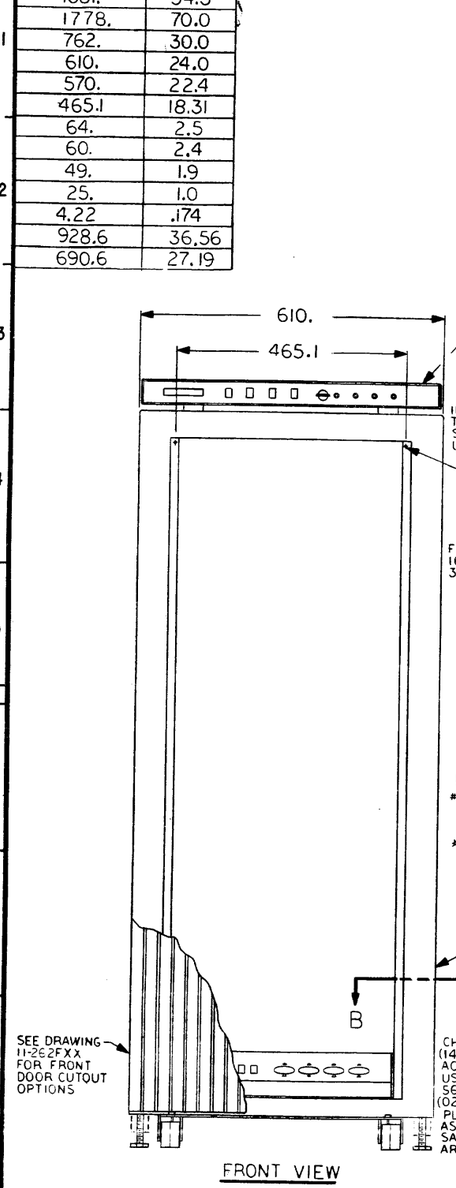
DRAFTER	J TAMULEVICIUS
DATE	10-14-81

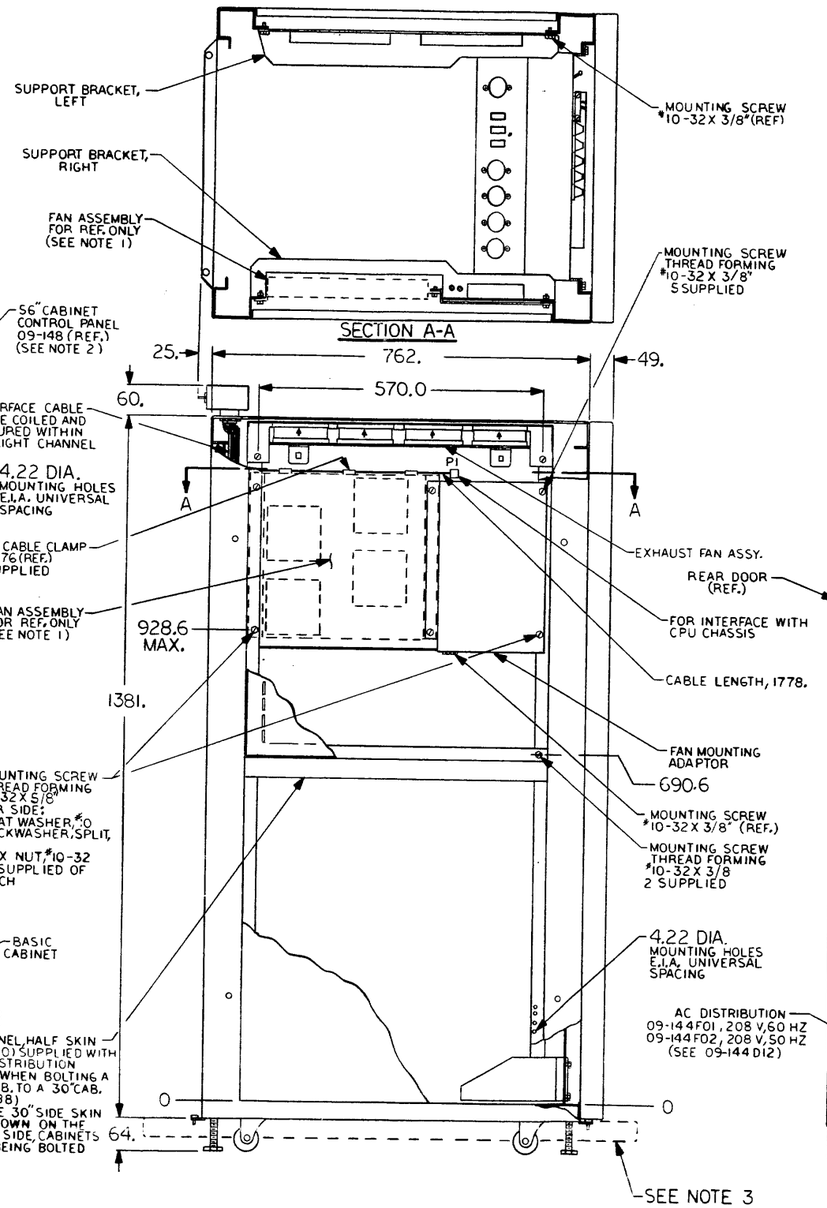
PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

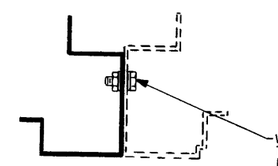
TITLE
INFORMATION DWG.
FRONT DOOR AND FILLER PANEL
OR FILLER PANELS
30" CABINET

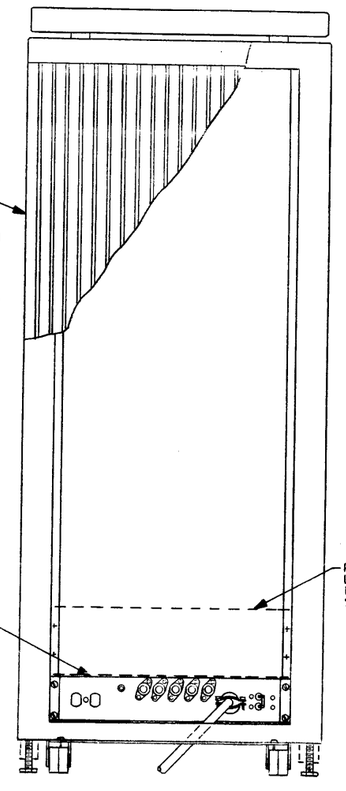
TASK	03131	SHT
DWG	02-786 D12	2-2

MILLIMETERS	INCHES
1381.	54.3
1778.	70.0
762.	30.0
610.	24.0
570.	22.4
465.1	18.31
64.	2.5
60.	2.4
49.	1.9
25.	1.0
4.22	.174
928.6	36.56
690.6	27.19









REVISIONS		
PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	12/23/81
	PROD	12/28/81

RELEASED FOR PRODUCTION
MFG. ENG. _____ DATE 2/19/82

METRIC

USED IN MANUAL 47-022

UNLESS OTHERWISE SPECIFIED		
SCALE: ~	TOLERANCE:	
	MILLIMETERS	INCHES
DIMENSIONS ARE IN MILLIMETERS	.XX ± .13 .X ± .5 X. ± .8	.XXX ± .005 .XX ± .02 .X ± .03

NAME	TITLE	DATE
J.TAMUL	DES/DFT	11-9-81
R.CERO	SUPV	2-19-82
	CHK	
R.DENGEL	ENG	2-19-82
P. ABITANTE	MGR	2-19-82
R.BARKER	QC	2-19-82

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE INFORMATION DWG.
56" CABINET
(3210/A)

TASK	03131	SHT
DWG	09-147 DI2	1-1

PART NO.	DESCRIPTION
09-147F02	INTERNATIONAL, 208V, 50Hz
09-147F01	DOMESTIC, 208V, 60Hz

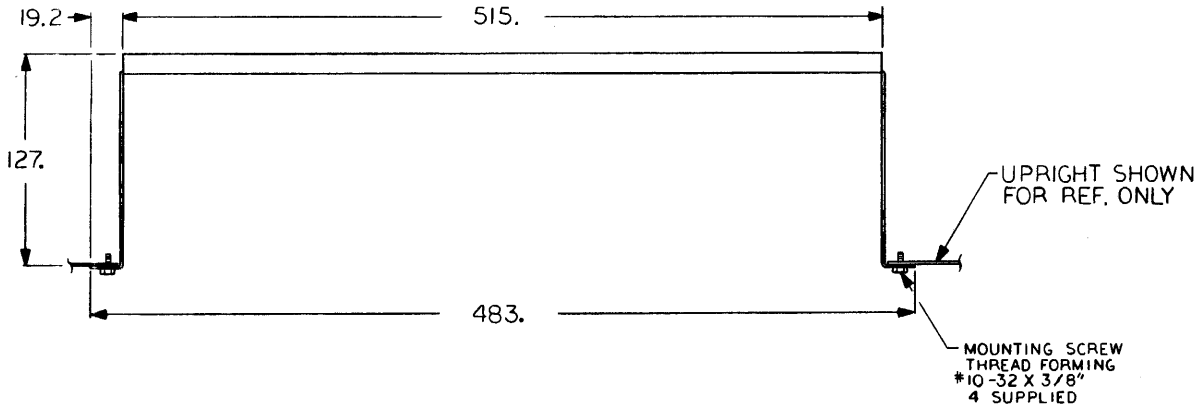
VARIATION TABLE

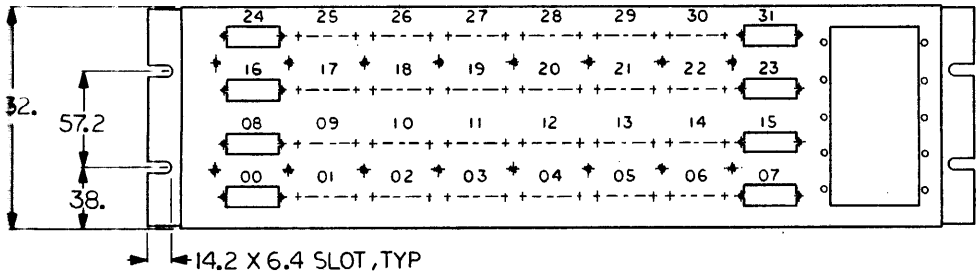
NOTES
1. FOR MOUNTING OF FAN ASSEMBLY (11-295M01 (M32-561)) SEE DWG. 11-295M01CI2
2. THE SYSTEM CONTROL PANEL SHALL OPERATE AS DEFINED IN 3210 PROCESSOR USERS MANUAL 29-747
3. STABILIZER LEGS ARE REQUIRED FOR ALL DISC EXPANSION 56" CABINETS. SEE INSTALLATION DRAWING 16-832.

RRUNNING 44-131 40/79

REVISIONS		
PRE PRODUCTION APPROVAL		INIT DATE
	DEV	12/3+31
	PROD	12/18/81

RELEASED FOR PRODUCTION
MFG. ENG. MJA DATE 2/19/82





METRIC

USED IN MANUAL 47-022

19.2	.75
515.	20.25
6.4	.25
14.2	.56
38.	1.5
57.2	2.25
127.	5.00
132.	5.2
483.	19.00
MILLIMETERS	INCHES

NOTES 1. FOR USE IN 56" CABINET (SEE 09-147D12)

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

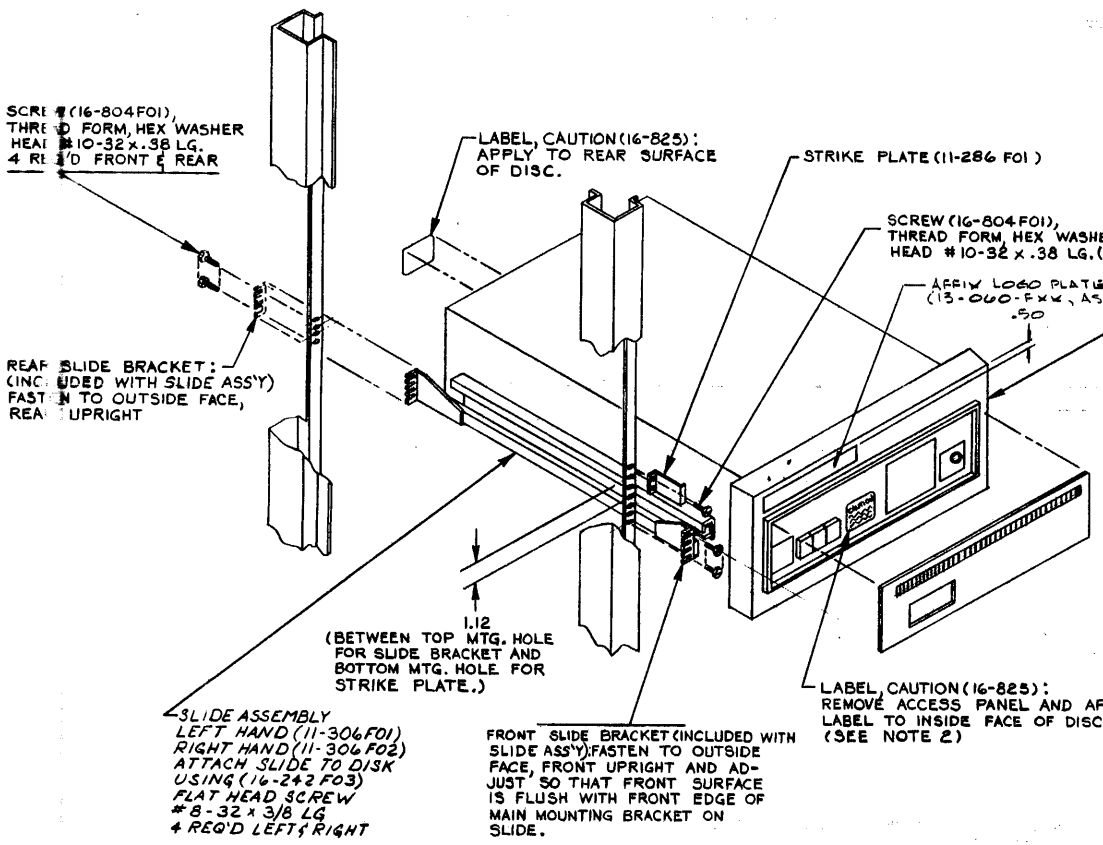
UNLESS OTHERWISE SPECIFIED				
SCALE: 1/2	MILLIMETERS		TOL	INCHES
DIMENSIONS ARE IN MILLIMETERS	.XX	± .13	.XXX ± .005	
	.X	± .5	.XX ± .02	
	X.	± .8	.X ± .03	

NAME	TITLE	DATE
J TAMUL	DES / DFT	10-14-81
R CERO	SUPV	2-19-82
	CHK	
R DENGEL	ENG	2-19-82
P ABITANTE	MGR	2-19-82
R BARKER	QC	2-19-82

TITLE 3210/A
INFORMATION DWG.
I/O INTERFACE PANEL

TASK 03131 | SHT 1-1
DWG 02-787 C12

REVISIONS				
PRE PRODUCTION APPROVAL	INIT	DATE		
	DEV			
	PROD			
IN AREA H3, (02-681) OR (02-682) WAS (02-682)				
VT		4588	R	2-27-81 R01
AREA C6 ADDED SLIDE ASS'Y INFORMATION. AREA E6 "(INCLUDED W/ SLIDE ASS'Y)" WAS "(INCLUDED WITH DISK)".				
KR		4970	R	3-29-82 R02



NOTES

1. INSTALLATION PROCEDURE TYPICAL BOTH SIDES.
2. ALL CABINETS REQUIRING 80 MB DISK MUST BE FITTED WITH STABILIZER LEGS (PER 16-832) PRIOR TO INSTALLATION.

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

UNLESS OTHERWISE SPECIFIED			
SCALE: ~	TOLERANCE: .XXX ± .005 .X ± .03 .XX ± .02 ANGLES ± 1°		
DIMENSIONS ARE IN INCHES			
NAME		TITLE	DATE
	A. WILLIAMS	DES / DFT	7-2-80
R. CERO		SUPV	
		CHK	
D. FOGGIA		ENG	
P. ABITANTE		MGR	
R. BARKER		QC	

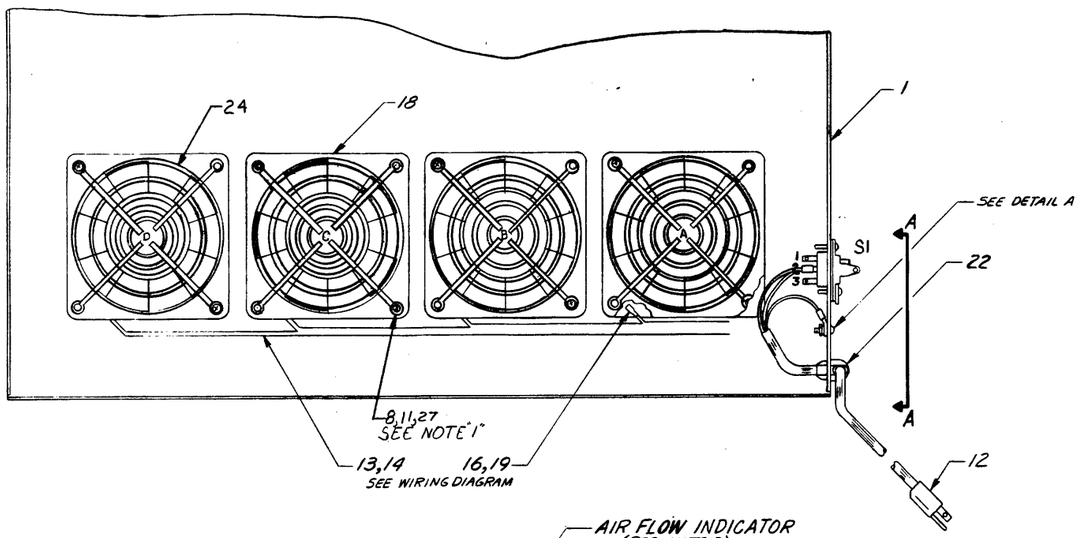
TITLE
INFORMATION DRAWING
80 MB DISK INSTALLATION
(56" CABINET)

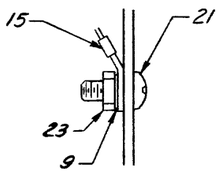
TASK 03039	SHT
DWG 16-824 R02 C12	1 - 1

BRUNING 44-131 40579

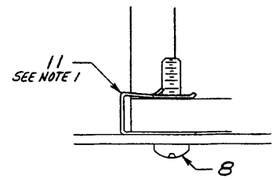
PERKIN-ELMER
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS
RELEASED FOR PRODUCTION MFG. ENG. NB DATE 7-13-76
EXTENSIVE CHANGES MADE, TO SHT, FOR R00 SEE MIRCO FILM COPY. ADDED SHT 2.
KR | JT | 3965 | R | 8-20-79 | R01
EXTENSIVE CHGS MADE TO SHTS 1 & 2; FOR R01 SEE MICRO FILM COPY.
JWH | JT | 9279 | R | 6-23-80 | R02
AREA K-7, ADDED "F03" TO VIEW; AREA L-7, ADDED "F00" TO VIEW; AREA G-9, ADDED "-- (115VAC & 09-056 F03/M02 (230VAC)" ADDED REV LEVEL TABLE.
JWH | JT | 4919 | R | 1-11-82 | R03 | X

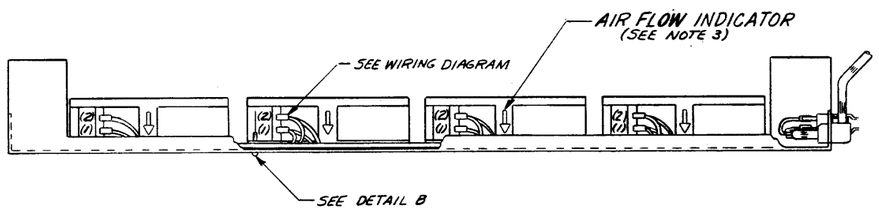


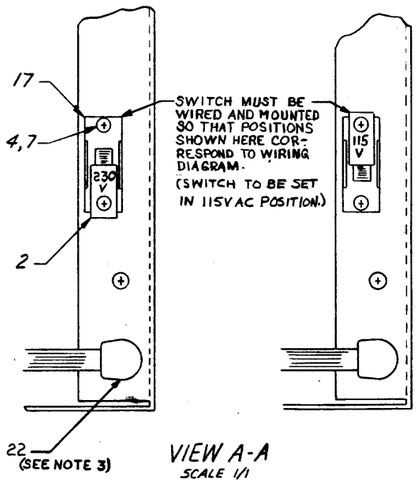


DETAIL A
SCALE 2/1



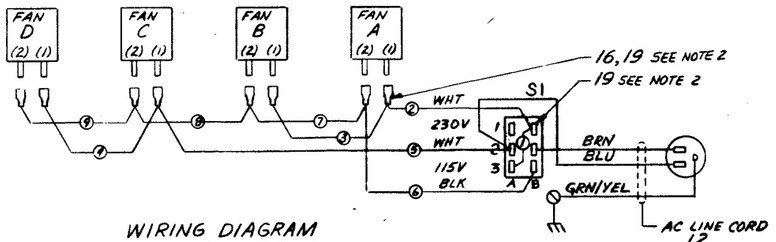
DETAIL B
SCALE 2/1





VIEW A-A
SCALE 1/1

F03 F00

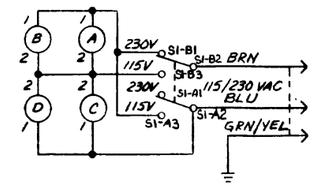


WIRING DIAGRAM
SEE TABLE A FOR COLOR AND WIRE LENGTHS

TABLE A

NO	COLOR	LENGTH
1	WHITE ITEM 13	21/2
2		8
3		7
4		7
5		18
6		8
7	BLACK ITEM 14	7
8		7
9		7

ALL WIRE 20 AWG



SCHEMATIC

09-056 F00 M02 (115VAC) 09-056 F03 M02 (230VAC)

REV LEVEL	3	2
SHT. SIZE	D	D
SHT NO.	1	2

NOTES:
1. INSTALL SPRING CLIP WITH FORMED THREAD ON INNER SIDE OF FAN FLANGE.
2. COVER ENTIRE TERMINAL WITH ITEM 19.
3. POSITION AS SHOWN.

NAME	TITLE	DATE
J. CONWAY	DRAFT	4-5-76
R.F. CERO JRB	CHK	4-12-76
F.M. MINAR	ENGR	4-12-76
R. BARKER	QC	4-12-76
P. ABITANTE	MGR	4-12-76

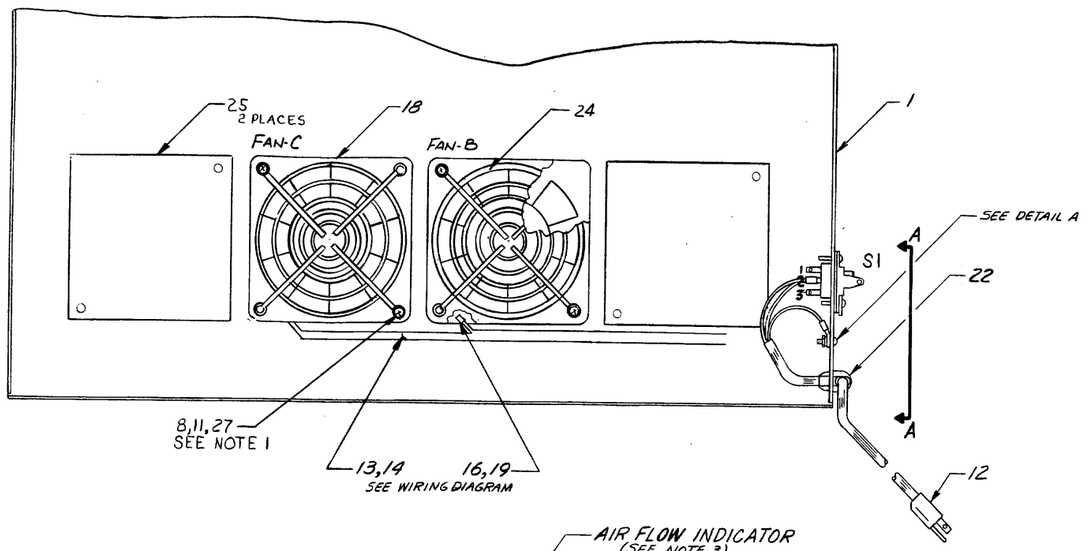
SCALE –
TOLERANCE
XXX ± .005
XX ± .03
X ± .09
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

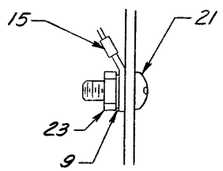
TITLE
EXHAUST FAN ASSEMBLY

ECN 2710
DWG NO. 09-056 M02 R03 R03
SHEET OF 1 — 2

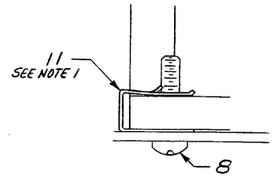
PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

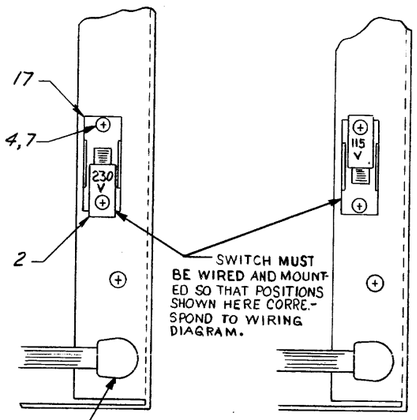




DETAIL A
SCALE 2/1



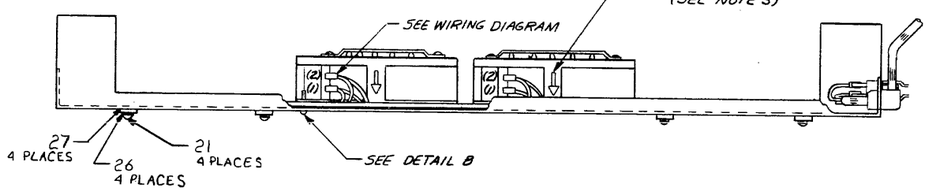
DETAIL B
SCALE 2/1

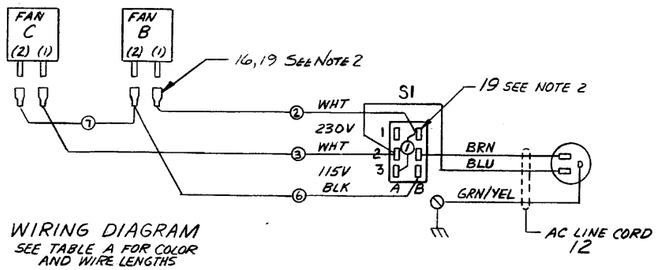


VIEW A-A
SCALE 1/1

F02

F01



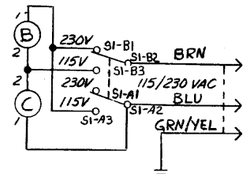


WIRING DIAGRAM
SEE TABLE A FOR COLOR AND WIRE LENGTHS

TABLE A

NO	COLOR	LENGTH
1		2 1/2
2		15
3	WHITE ITEM 13	18
6		15
7	BLACK ITEM 14	7

ALL WIRE 20 AWG
ALL LENGTHS IN INCHES



SCHEMATIC

09-056 F01 (115V AC) & F02 (230V AC) M02

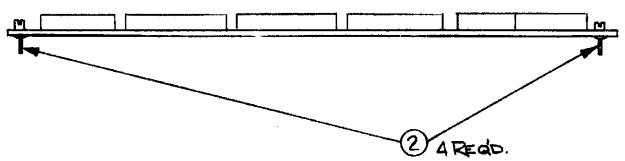
NOTES:
1. INSTALL SPRING CLIP WITH FORMED THREAD ON INNER SIDE OF FAN FLANGE.
2. COVER ENTIRE TERMINAL WITH ITEM 19.
3. POSITION AS SHOWN.

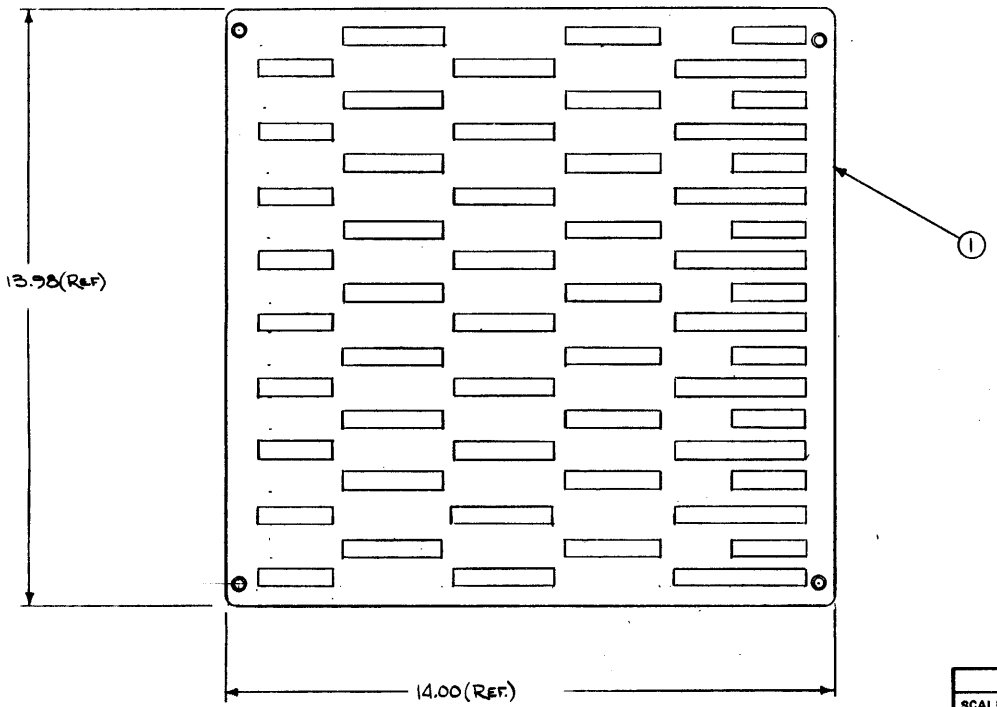
	NAME	TITLE	DATE
SCALE —	T.P.GAVIN	DRAFT	3-12-79
TOLERANCE XXX ± .005, XX ± .02, X ± .01, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	R.F. CERO JR	CHK	3-12-79
	S. SOLOMON/B.SALAMARY	ENGR	3-12-79
	R. BARKER	QC	3-12-79
	P. ABITANTE	MGR	3-12-79

TITLE: EXHAUST FAN (2) ASSEMBLY
TASK NO. 03039
DWG NO. 09-056M02 F02005
SHEET OF 2 — 2

BRUNING 44-231 24558

REVISIONS					
RELEASED FOR PRODUCTION MFG. ENG. C. Tolla DATE 8/24/79					
REVISED AREA C2 & F2 TO REFLECT NEW RIVETS. (ITEM 2)					
KR	JW	4970	R	3-29-82	201





NOTES

UNLESS OTHERWISE SPECIFIED			
SCALE: 1/2	TOLERANCE: .XXX ± .003 .X ± .05 .XX ± .02 ANGLES ± 1°		
DIMENSIONS ARE IN INCHES			
NAME		TITLE	DATE
T. GAVIN		DES / DFT	3-21-79
R. CERO		SUPV	8.28.79
		CHK	
S. SOLOMON		ENG	8.28.79
P. ABITANTE		MGR	8.28.79
R. BARKER		QC	8.28.79

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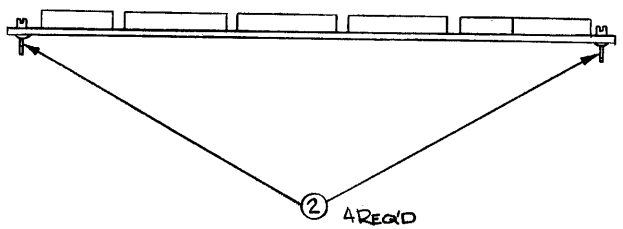
Computer Systems Division
Oceanport, N.J. 07757

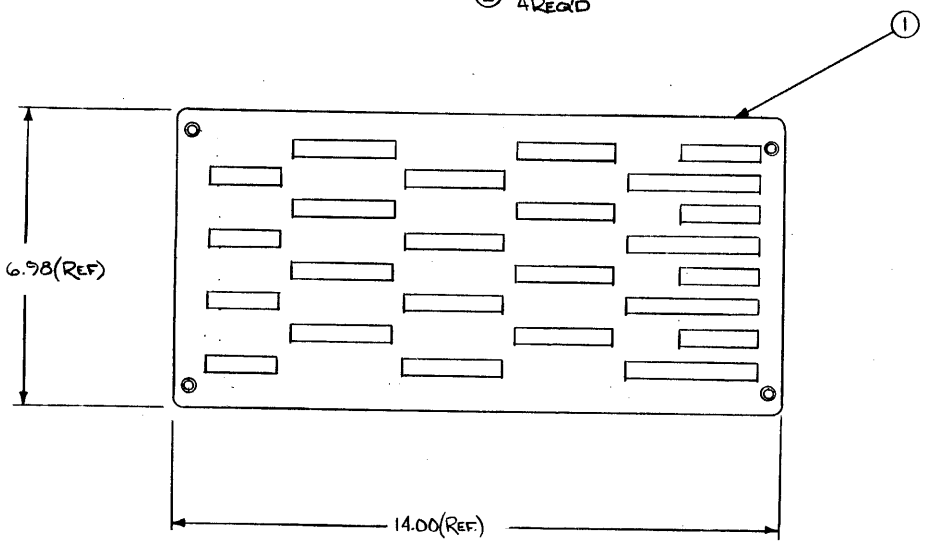
TITLE
ASSEMBLY
PERFORATED COVER (14 INCH)

TASK 03913 SHT 1 - 1

DWG 11-271 R01 C03

REVISIONS					
RELEASED FOR PRODUCTION MFG. ENG C Talen DATE 8/30/79					
AREA C3, F3, REVISE TO REFLECT NEW RIVET. (ITEM 2)					
KR	W	4970	R	3-29-82	R01





NOTES

UNLESS OTHERWISE SPECIFIED			
SCALE: 1/2	TOLERANCE: .XXX ± .005 .X ± .03 .XX ± .02 ANGLES ± 1°		
DIMENSIONS ARE IN INCHES			
NAME		TITLE	DATE
T. GAVIN		DES / DFT	3-21-79
R. CERO		SUPV	8 28 79
		CHK	
S. SOLOMON		ENG	8 28 79
P. ABITANTE		MGR	8 28 79
R. BARKER		QC	8 28 79

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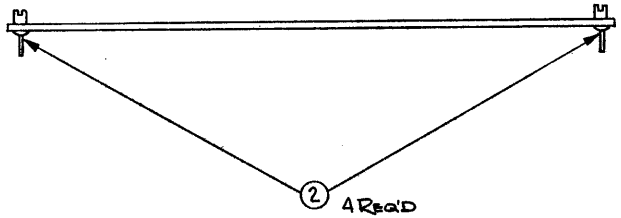
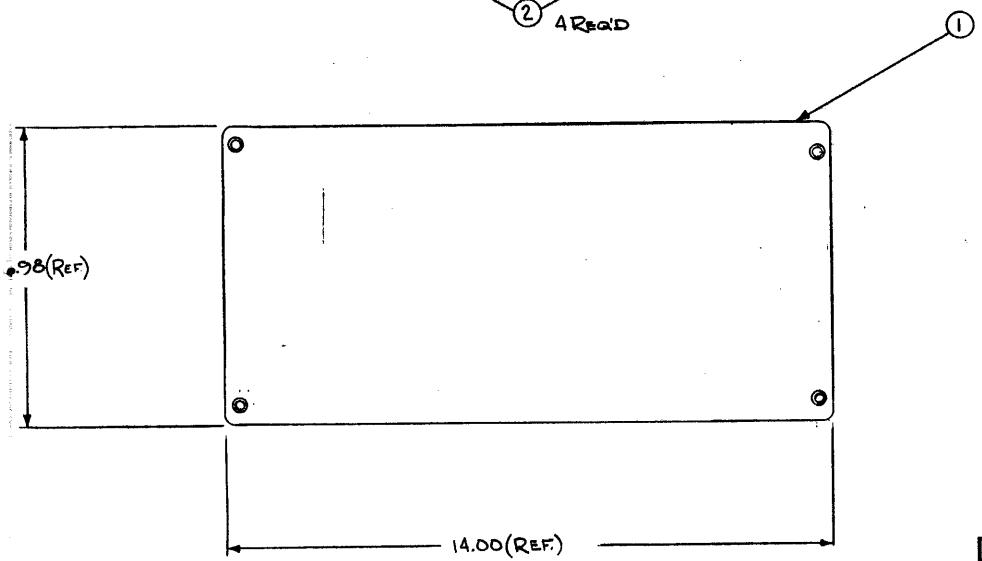
Computer Systems Division
Oceanport, N.J. 07757

TITLE
ASSEMBLY
PERFORATED COVER (7 INCH)

TASK 05913	SHT
DWG 11-272.R01 C03	1 - 1

REVISIONS				
RELEASED FOR PRODUCTION MFG. ENG. [signature] DATE 8/30/79				
AREA C3 & F3, REVISED TO REFLECT NEW RIVETS (ITEM 2)				
XR 4970	R	3-29-82	R01	X





NOTES

UNLESS OTHERWISE SPECIFIED			
SCALE: 1/2	TOLERANCE: .XXX ± .005 .X ± .03 .XX ± .02 ANGLES ± 1°		
DIMENSIONS ARE IN INCHES			
NAME		TITLE	DATE
	T. GAVIN	DES / DFT	3-21-79
R. CERO		SUPV	8.28.79
		CHK	
S. SOLOMON		ENG	8.28.79
P. ABITANTE		MGR	8.28.79
R. BARKER		QC	8.28.79

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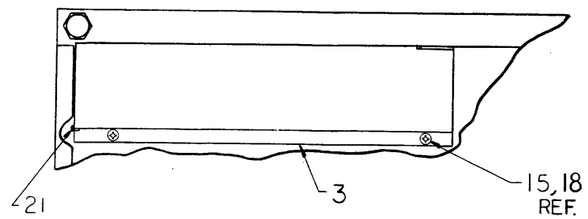
Computer Systems Division
Oceanport, N.J. 07757

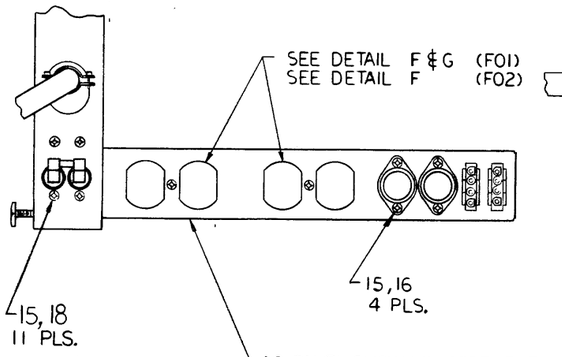
TITLE: ASSEMBLY SOLID COVER

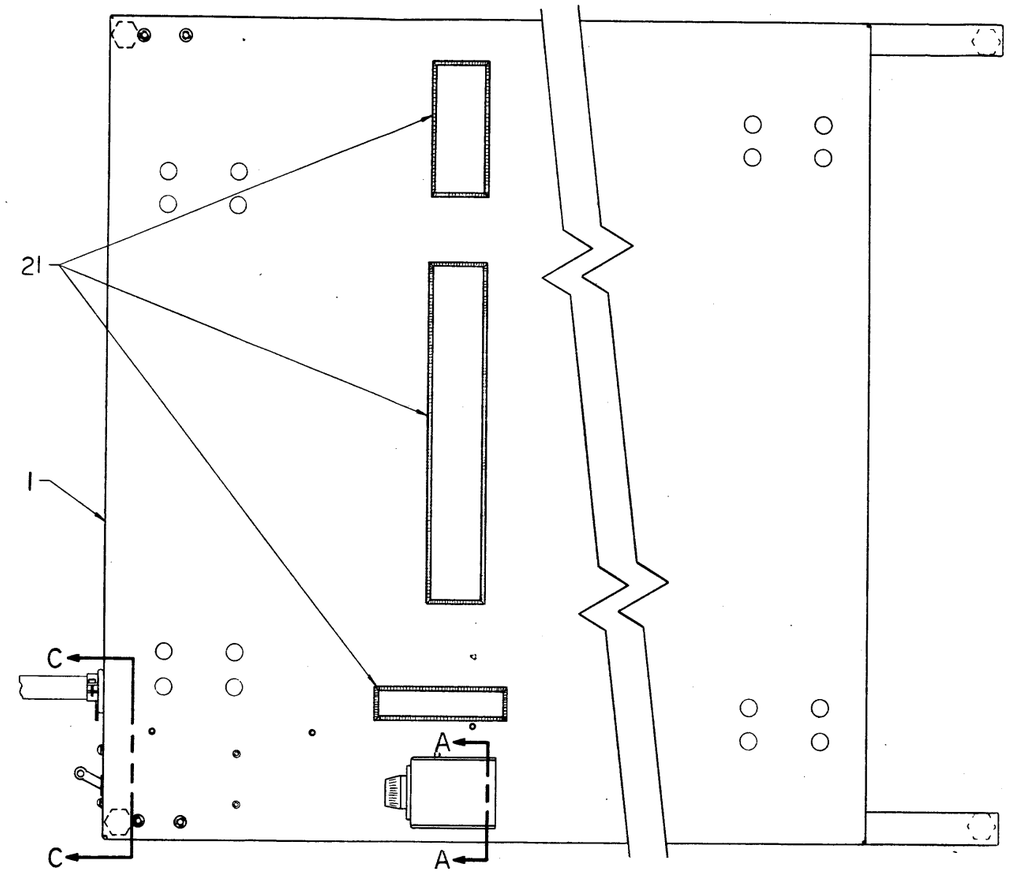
TASK 03913 | SHT 1 - 1

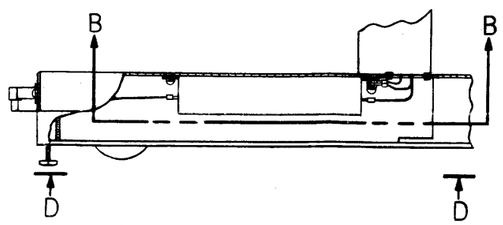
DWG 11-273801C03



PARTIAL VIEW D-D







REVISIONS					
RELEASED FOR PRODUCTION MFG. ENG. MJR DATE 8/19/82					
REVISED SHTS 1 & 3					
JLV	AV	5061	R	8-31-82	R01

USED IN MANUAL 47-022

UNLESS OTHERWISE SPECIFIED			
SCALE: ~	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°		
NAME		TITLE	DATE
K REED		DES/DFT	4-28-82
G. MILLER		SUPV	
J. VIGILANTE		CHK	
D. FOGGIA		ENG	
P. ABITANTE		MGR	
R. BARKER		QC	

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Oceanport, N.J. 07757

NO.	DESCRIPTION
11-296F01M01	AS SHOWN PER SHTS. 1 & 3 , INTERNATIONAL 208 V
11-296F02M01	AS SHOWN PER SHTS 1 & 2 , DOMESTIC 208V

VARIATION TABLE

NOTES

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

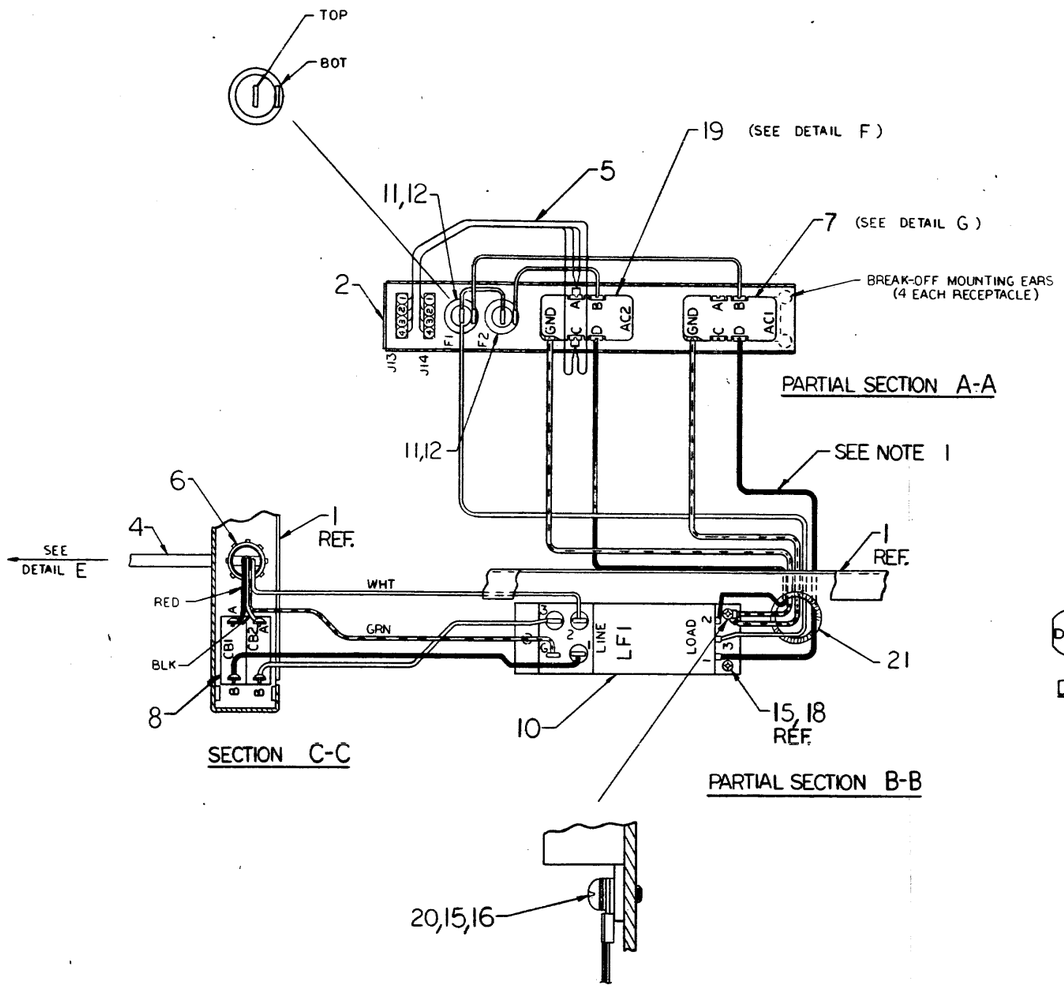
3	2	1	- SHEET NO.
D	D	D	SHEET SIZE

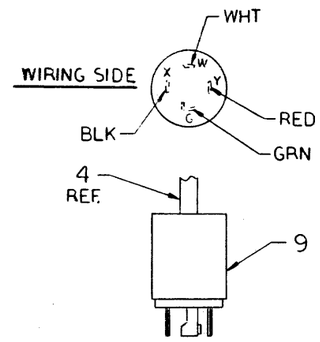
REV. LEVEL

TITLE
ASSEMBLY, BASE PAN

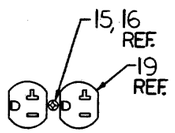
TASK 03039
DWG 11-296M01 R01 D03
SHT 1-3

DRAWING 44-131-40579

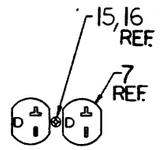




DETAIL E



DETAIL F
(115 VAC)



DETAIL G
(250 VAC)

208V (DOMESTIC)
11-296F01M01

NOTES
1. ALL WIRES SHOWN ARE PART OF ITEM 4, UNLESS OTHERWISE SPECIFIED.

DRAFTER	J TAMULEVICIUS
DATE	12-30-80

REVISIONS

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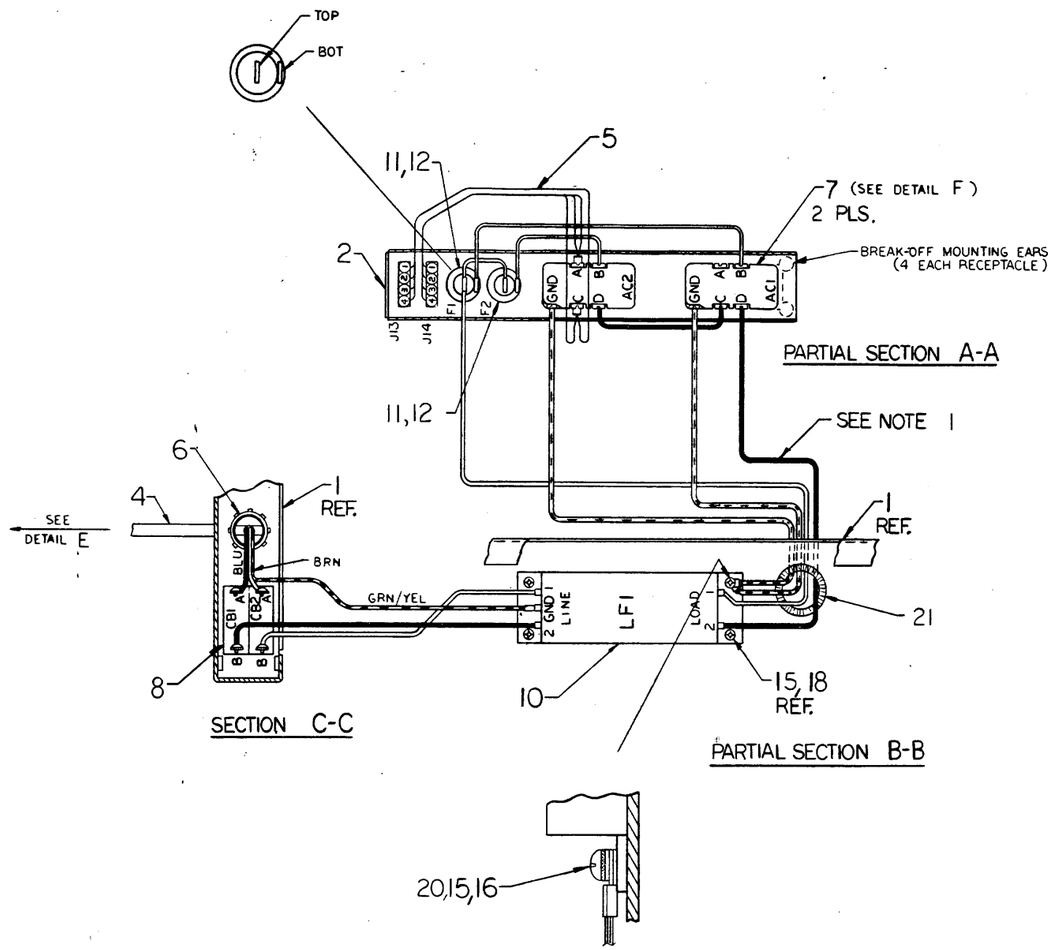
Computer Systems Division
Oceanport, N.J. 07757

TITLE
ASSEMBLY, BASE PAN

TASK 03039		SHT
DWG 11-296 M01	D03	2 - 3

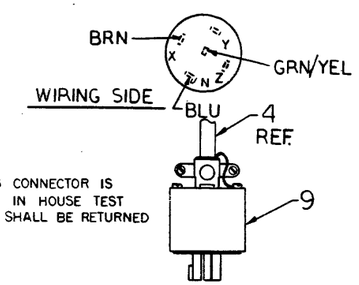
REVISIONS					
AREA K2 ADDED NOTE					
JLV	[illegible]	5061	R	8-31-82	R01



PARTIAL SECTION A-A

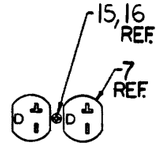
SECTION C-C

PARTIAL SECTION B-B



NOTE: THIS CONNECTOR IS REQ'D FOR IN HOUSE TEST ONLY AND SHALL BE RETURNED TO STOCK

DETAIL E



DETAIL F
(250 VAC)

208V (INTERNATIONAL)
11-296F02M01

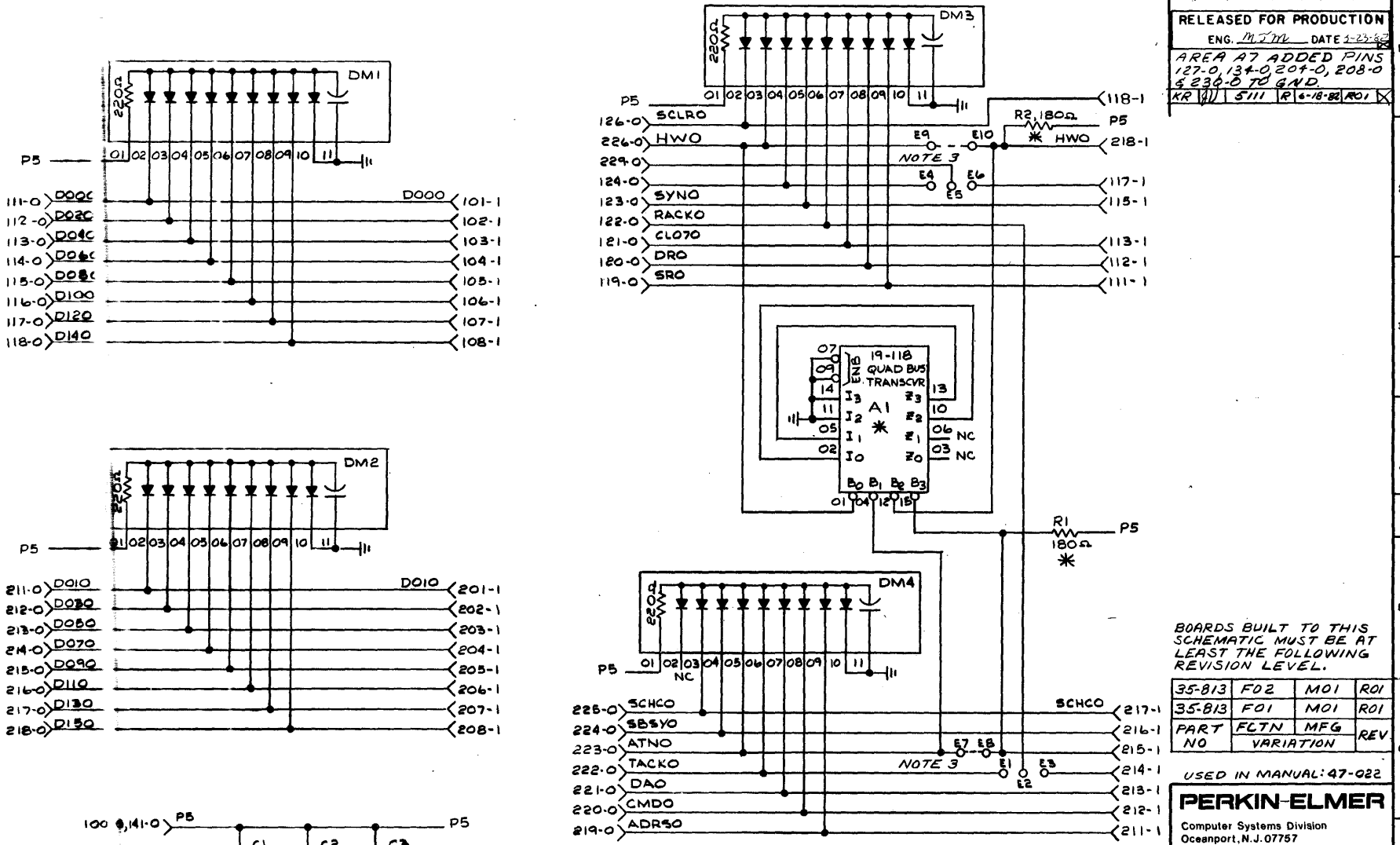
PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

NOTES
1. ALL WIRES SHOWN ARE PART OF ITEM 4, UNLESS OTHERWISE SPECIFIED.

DRAFTER	K REED
DATE	

TITLE: ASSEMBLY, BASE PAN

TASK 03039		SHT
DWG 11-296M01 R01	D03	3 - 3



REVISIONS				
RELEASED FOR PRODUCTION ENG. M.J.M. DATE 3-23-82				
AREA A7 ADDED PINS 127-0, 134-0 204-0, 208-0 & 230-0 TO GND.				
KR		5111	R	6-18-82 A01

BOARDS BUILT TO THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL.

PART NO	FCTN VARIATION	MFG	REV
35-813	F02	M01	R01
35-813	F01	M01	R01

USED IN MANUAL: 47-022

STRAPPING TABLE	
F02	STRAP E1-E3 ONLY
F01	STRAP E7-E8, E9-E10 ONLY

NOTES
1. DIODE MODULES ARE 23-062 F01
2. * DENOTES COMPONENTS USED ON F02 ONLY.
3. STRAPPING FOR F01 ONLY

UNLESS OTHERWISE SPECIFIED			
SCALE: —	TOLERANCE: .XXX ± .003 .X ± .03 .XX ± .02 ANGLES ± 1°		
DIMENSIONS ARE IN INCHES			
NAME		TITLE	DATE
B. GRAY		DES / DFT	3-24-82
R. CERO		SUPV	3-24-82
		CHK	
M. MANGIONE		ENG	3-24-82
P. OBRDA		MGR	3-24-82
R. BARKER		QC	3-24-82

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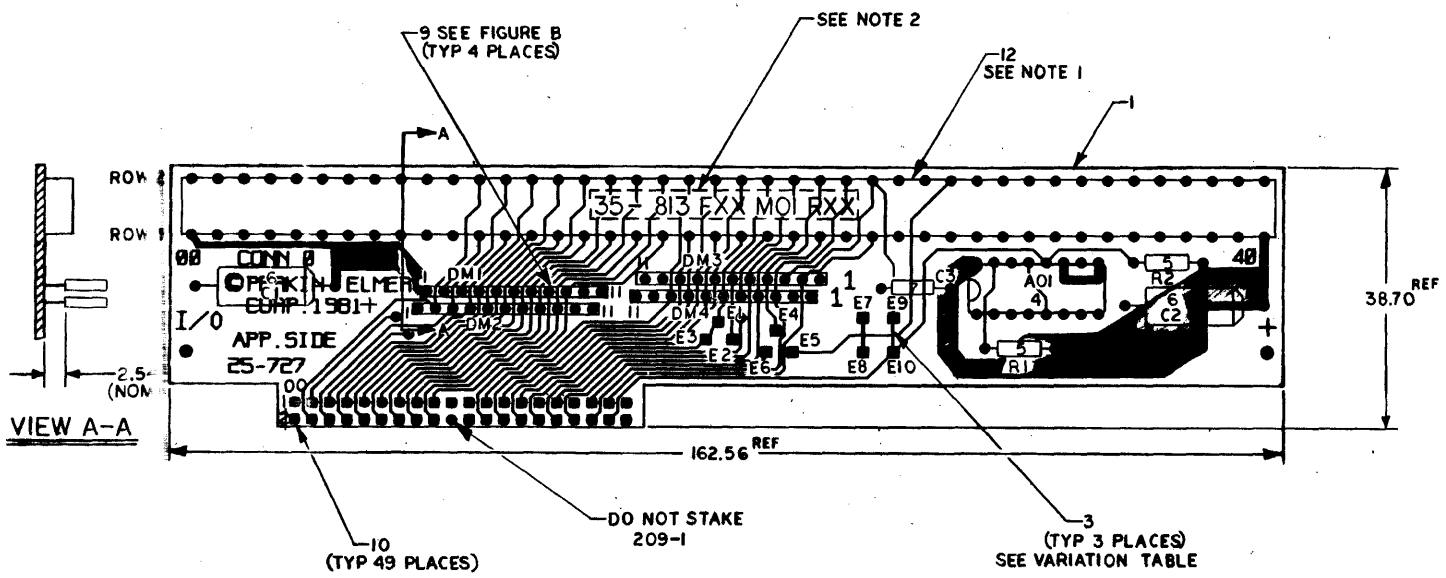
Oceanport, N.J. 07757

TITLE SCHEMATIC
I/O TERM BOARD

TASK 03179 SHT 1-1
DWG 35-813 M01 R01 C08

MILLIMETER	INCHES
38.70	52
162.56	40
2.54	10

REVISIONS				
RELEASED FOR PRODUCTION MFG. ENG. MJQ DATE 3/24/82				
REVISE TO REFLECT R01 COPPER. RELOCATED C3				
KR	80	5111	R	6-18-82 R01 X



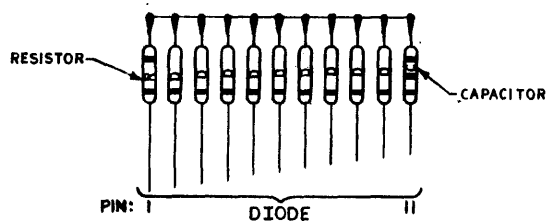


FIGURE B

METRIC

USED IN MANUAL: 47-022

F02	AS SHOWN, STRAP E1-E3 ONLY
F01	AS SHOWN, LESS ITEMS 4&5, STRAP 7-E8, E9-E10 ONLY

VARIATION TABLE

NOTES
1. BEND PINS CLOSEST TO EDGE OF BOARD INWARD PRIOR TO SOLDERING
2. FOR BOARD IDENTIFICATION SEE SSP 002-0D

TOLERANCE IN MILLIMETERS	
X	± .8
.X	± .5
.XX	± .13
UNLESS OTHERWISE SPECIFIED	

UNLESS OTHERWISE SPECIFIED			
SCALE: 2/1	TOLERANCE IN INCHES		
DIMENSIONS ARE IN MILLIMETERS	.XXX ± .005	.X ± .03	ANGLES ± 1°
	.XX ± .02		

NAME	TITLE	DATE
B.GRAY	DES/DFT	3-24-82
R.CERO	SUPV	3-24-82
	CHK	
M.MANGIONE	ENG	3-24-82
P.OBRDA	MGR	3-24-82
R.BARKER	QC	3-24-82

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE ASSEMBLY
PRINTED CIRCUIT BOARD
I/O
TERM. BOARD

TASK 03179 SHT 1-1
DWG 35-813 MOI REV C03

BRUNING 44-131 40879

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☐ Addition Page No. _____ Drawing No. _____

☐ Other Page No. _____ Drawing No. _____

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Computer Systems Division
2 Crescent Place
Oceanport, NJ 07757

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